Gate Length Scaling Effects in ESD Protection Ultrathin Body SOI Devices

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ABSTRACT

In this paper we experimentally explore the gate length scaling effects that related to the abrupt degradation of electrostatic discharge (ESD) robustness for ultra-thin body silicon on insulator (SOI) devices and integrated circuits (ICs). It is found that, for the ultra-thin body SOI, the ESD protection devices fail when the gate length of protection devices is smaller than the 0.18 micron meter (um). Taking the effects into consideration, it is believed that optimizations among the device profiles, geometries, and the protection efficiency should be done simultaneously for high performance VLSI circuit design, in particular for modern system-on-chip (SoC). This observation is very useful in both the nano-scale CMOS fabrication technology and VLSI circuit design.

Keywords: SOI, ESD, SoC, VLSI, optimization, Ultrathin body SOI, short channel

1 INTRODUCTION

ESD protection for device and circuit has been of important reliability concerns with the rapid progress in the miniaturization and process technology recently [1-4]. It is known that ESD robustness reveals the major demerit for the SOI technology and application [2]. Diverse works have been reported in the investigation of ESD robustness for SOI devices recently [3]; the improvement is very limited, especially for the ultrathin body film SOI devices. Therefore, a constructive investigation of ESD robustness for ultra-thin body SOI devices should at the same time take the SOI circuit into consideration.

In this paper, we investgate the ESD robustness of devices which fabricated on two kinds of SOI wafers. The first wafer has its silicon thickness 140 nm and the other one is 90 nm. For all gate lengths, without considering the turn on voltage and turn on resistance, the thicker body film has a stable robustness (~ 3 mA/μm). On the other hand, an abruptly decreasing of ESD robustness is found in the thinner one. The abrupt robustness reduction in short gate-length devices (gate length < 0.18 μm) with thin silicon film is examined that a narrow conduction path occurs when devices turn on. The narrow path is caused from a lower doping concentration regime near the interface of silicon/buried oxide [4]. For thin silicon film devices, the high n-type concentration regime of source/drain extensions are extending all over the silicon thin film that connecting to the low boron-doping region. Therefore, a punch-through path is generated and burn out this narrow trace. Our investigation demonstrates that the optimization is necessary and has to be achieved by considering the device profiles, geometries, and efficiency.

2 DEVICE FABRICATION AND MEASUREMENT

Two kinds of SOI wafers are used in fabrication test devices. The first one has its silicon thickness of 140 nm and the other one is 90 nm. Figure 1 shows the test structure of all devices that a 90 nm CMOS technology with the gate oxide thickness of 1.2 nm is used. ESD robustness is characterized by transmission line pulse (TLP) with its diagram shown in figure. 2, moreover, in well agreement with the ESD robustness measurement from HBM, the pulse width is setup to 100 nsec.

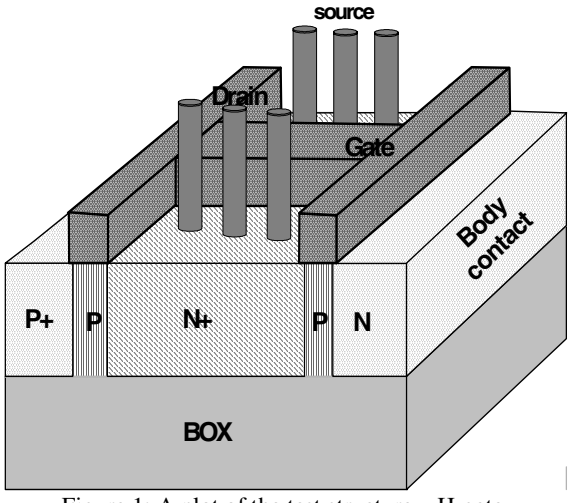

Figure 1: A plot of the test structure – H-gate.

One loop of the TLP measurement includes following steps; firstly the switch will be turned to node 1, at the meanwhile, transmission line will be charged to a designed voltage by a high voltage source. Secondly, the charged transmission line will discharge to the device under test (DUT) whenever the switch closes on the node 2. During the discharge process, a digital waveform scope is used to automatically calculate transient IV characteristics of the DUT.

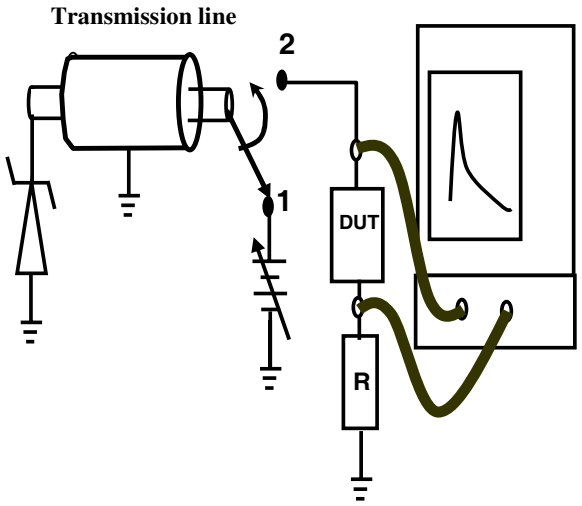

Figure 2: An illustration of the TLP measurement configuration in the study.

Soon after the discharge step finished, a quasi-static IV measurement is done to evaluate the health of DUT. If a healthy status is decided, a new TLP loop will be taken to a higher charge voltage. Otherwise, the measurement will be ended that the TLP IV measurement is finished. The quasi-static IV characteristics are measured by using the HP4156B semiconductor analyzer.

3 RESULTS AND DISCUSSION

Figure 3 shows the TLP IV characteristics of the thicker silicon film devices. It could be easily found that a longer gate length will result in a higher turn voltage, moreover, a snap back Phenomena is also observed in the longer channel device. Those results indicate different turn on mechanisms existed in the thick body devices. A more detail mechanism could be drawn that turn on behaviors of parasitic bipolar junction transistor (BJT) dominates IV characteristics of longer channel devices. Consequently the drain junction breakdown initiated parasitic BJT turn on and thus got a higher turn on voltage and a snap back behavior. On the other hand, drain induced barrier height lowering (DIBL) at drain side plays the major role in short devices; therefore we can have a lower turn on voltage IV curve without having a snap back characteristic.

Though the turn on characteristics is strongly related to the channel length of the SOI devices; the ESD robustness keeps almost the same for all the thick body devices. The result is mainly caused from the fact that the narrow silicon film allows very limited current flows. Owing to the very finite current path, a slight higher current flow can melt silicon thin film. This is the major challenge in design the SOI circuits.

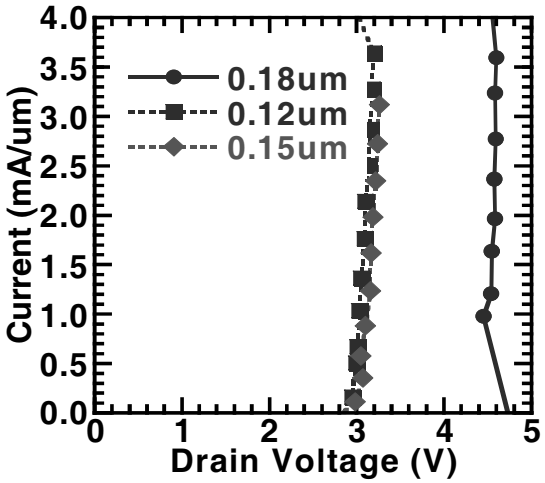

Figure 3: TLP IV characteristics of thick silicon sample with various gate lengths.

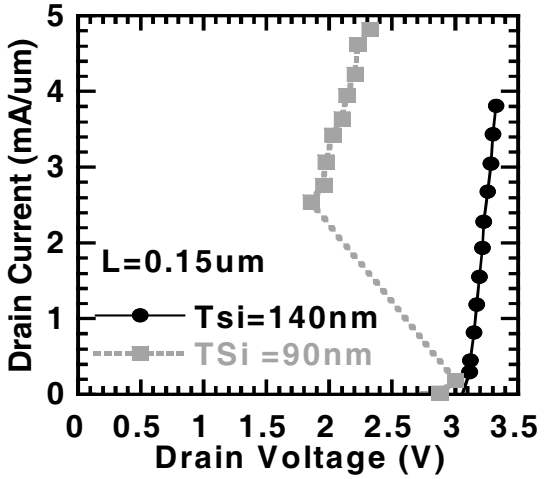

Figure 4: TLP IV characteristics of both thin and thick silicon samples

Figure 4 compares TLP IV characteristics difference between the thin and thick body SOI devices. It could be clearly explored that the thin body device will be burned out whenever the device turned on. This observation is not only true for 0.15 um lengthen device, but also real for any thin body device with its channel length shorter than 0.15 um. More details could be investigated form the Figure 5

that ESD robustness sustains constant when the channel length larger than 0.15um. On the other hand, the ESD robustness is abruptly degrading to nearly zero while the channel length of device is scaled down to less than 0.15um. This result is very important in designing the ESD protections on the SOI circuits. Moreover, mechanisms that dominate the ESD characteristic must be also discussed to have a better achievement in SOI circuit.

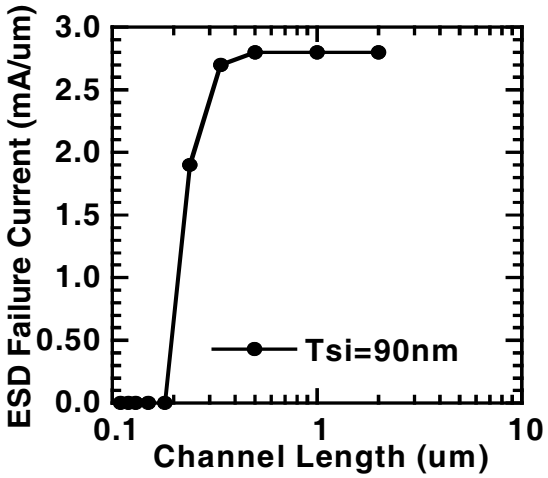

Figure 5: ESD failure current vs. gate length of the thin silicon sample

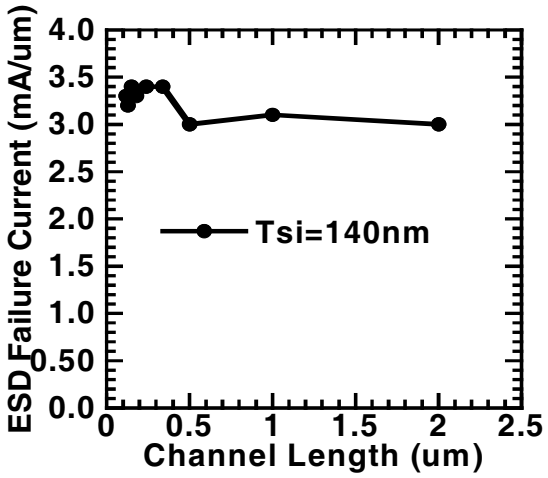

Figure 6: ESD failure current vs. gate length of the thick silicon sample

Unlike the thin body SOI device, the thick body device has a nearly channel length independent ESD robustness. This result could be referred to Figure 6 that thick body SOI device has ESD robustness about 3mA/um. In comparing with the long channel (Lg > 0.15) thin body SOI devices, the thick body device has a better ESD robustness. The result is very reasonable that a wider current path will be existed in the thicker body device; therefore, sustains a high current flow. The abruptly degradation phenomena occurred in the thin body SOI device could be explained by the following two figures.

Figure 7 shows the cross section view of the thick body SOI device. Owing to the segregation effects, the boron doping near the buried oxide (BOX) will greatly diffuse into the BOX; therefore, boron-doping concentration near the BOX will be largely lowered. It could be simplified that owing to the segregation effect, there exists a low boron doping concentration region as shown in the figure 7. The low boron doping concentration region is a relatively lower barrier height area, thus existing an easier punch through path. Fortunately, the easier punch-through region dose not connect to the source/drain extensions directly; the device would not turn on through this low boron concentration. The turn on path of the thick body device would flow through the source/drain extensions instead of the narrow low boron-doping path.

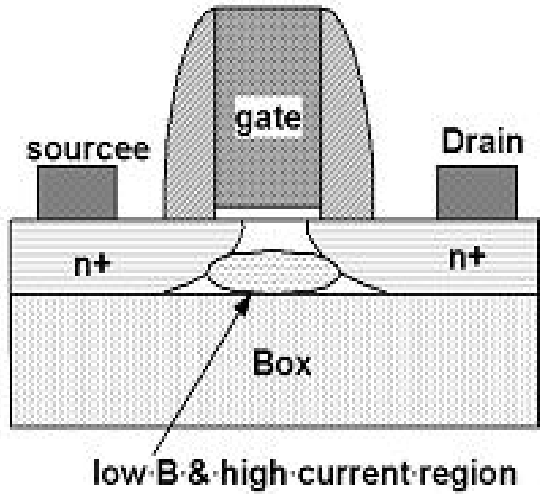

Figure 7: Cross section view of the current path in the thick silicon devices

On the contrary, thinning the thickness of the silicon film will make the low boron-doping region distributed much nearer to the source drain extensions. Therefore, as the channel length becoming shorter and shorter, the punch through path will take place of the normally turn on path.

Owing to the very limited punch through path, the path will be burned out soon after the device turned on. This effect will greatly limit the scaling ability of the SOI device. The effect will also limit the fabrication ability of fully depleted SOI devices. It is worse that the newly developed FinFET structure, the silicon film is thinning down to lower than 50nm. In those fully depleted thin silicon films, a similar phenomenon could be occurred. Accordingly, this result explores a serious challenge for the future proposed FinFET liked devices.

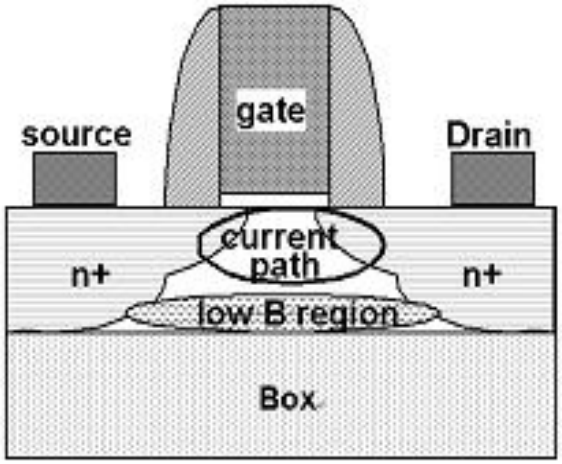

Figure 8: Cross section view of the current path in the thick silicon devices

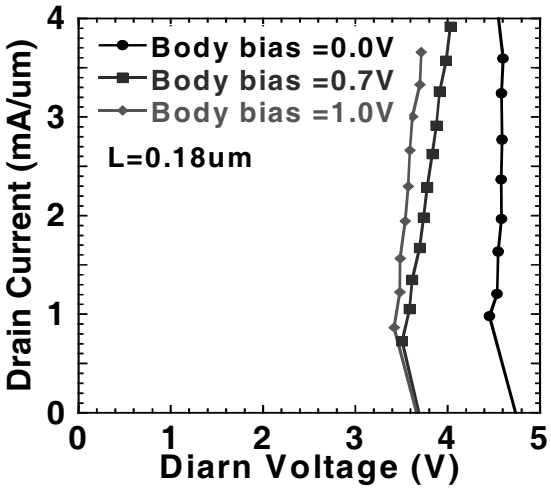

Figure 9: TLP IV characteristics of thick silicon sample with various body bias, where L = 0.18 um.

Substrate biased (body biased) technology is also performed on the thick body SOI device. Figure 9 and Figure 10 demonstrate that body bias did lower the turn on voltage of the long channel thick SOI device, but do not affect turn characteristic of the short channel devices. Those results are greatly consisted with our previous ratiocination that parasitic BJT dominates turn on behavior of the long channel thick body SOI device. Though a lower turn on voltage, the ESD robustness does not be affected by body bias (owing to a limited current path).

4 CONCLUSIONS

We have studied an abruptly degradation of ESD robustness owing to gate length reduction. Two kinds of SOI wafers have been used in the fabrication of test devices. The first one is with its silicon thickness 140 nm and the other is with 90 nm. We have observed that the robustness abruptly decreasing in the thinner one when the gate length is smaller than 0.18 um. For all gate lengths, the SOI with thicker body films has a stable robustness (~ 3 mA/um). Our investigation demonstrates that the optimization is necessary and has to be achieved by considering the device profiles, geometries, and efficiency.

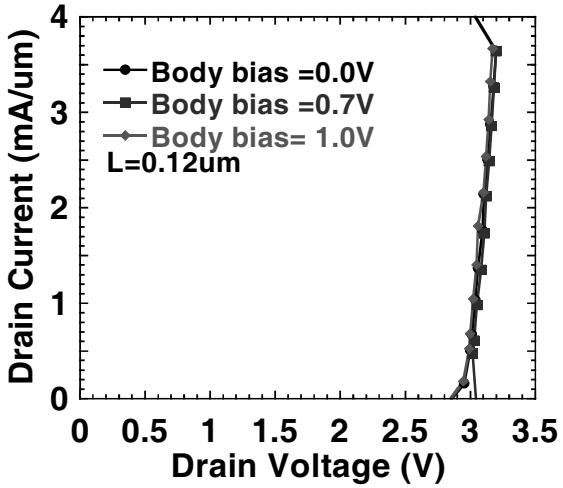

Figure 10: TLP IV characteristics of thick silicon sample with various body bias, where L = 0.18 um.

5 ACKNOWLEDGEMENTS

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