Compact, Physics-Based Modeling of Nanoscale Limits of Double-Gate MOSFETs

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ABSTRACT

Compact, physics-based models of subthreshold swing and threshold voltage are presented for double-gate (DG) MOSFETs in symmetric, asymmetric, and ground-plane modes. Applying these device models, threshold voltage variations in DG MOSFETs are comprehensively and exhaustively investigated using a unique, scale-length based methodology. Quantum mechanical effects and fringe-induced barrier lowering effect on threshold voltage, caused by ultra-thin silicon film and potential use of high-permittivity gate dielectrics, respectively, have been analytically modeled giving close agreement to numerical simulations. Scaling limits projections indicate that individual DG MOSFETs with good turn-off behavior are feasible at 10 nm scale; however, practical exploitation of these devices toward gigascale integrated systems requires development of novel technologies for significant improvement in process control.

Keywords: double-gate, scaling, threshold voltage, subthreshold swing, MOSFET.

1 INTRODUCTION

The double-gate (DG) MOSFET, illustrated in Figure 1, has been considered as the most promising device structure to extend CMOS scaling into the nanometer regime [1]. The ultra-thin silicon channel is undoped (i.e., lightly doped with the background doping concentration less than 10^{16} cm^{-3}) to avoid random dopant placement effect and mobility degradation associated with high doping. Depending upon gate work functions and gate-bias conditions, a DG MOSFET can operate in symmetric (SDG), asymmetric (ADG), or ground-plane (GP) modes. Two key characteristics of a MOSFET, namely, subthreshold swing (S) and threshold voltage (V_{TH}), and their dependences on device parameters are usually exploited to gauge its immunity to short-channel effects (SCE), i.e., its scalability. In this paper, compact, physical models of subthreshold swing and threshold voltage for symmetric, asymmetric, and ground-plane DG MOSFETs are described, including quantum mechanical effects and fringe-induced barrier lowering (FIBL) effect. These new device models are applied to comprehensively analyze parameter variations, reveal device design insights, and project scaling limits and opportunities of DG MOSFETs.

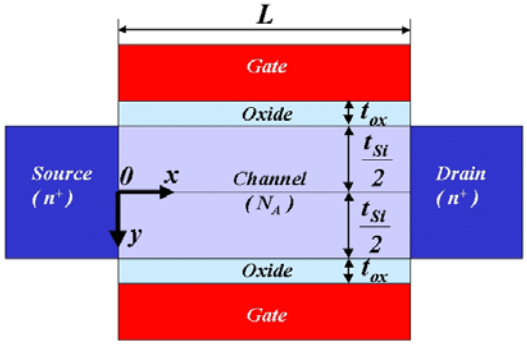

Figure 1: Cross-section schematic of a DG MOSFET.

2 SUBTHRESHOLD SWING MODELS

A two-dimensional (2-D) Poisson equation with the dopant term only is solved using the evanescent-mode analysis in the channel region to obtain the channel potential distribution [2]. To eliminate the uncertainty of choosing the most representative leakage path (channel surface versus channel center [3, 4]), it is assumed that the drain current is proportional to the *sheet* density of inversion carriers at the virtual cathode (i.e., the minimum potential point between the source and drain). Subthreshold swing, defined as the gate voltage (V_{GS}) change required for an order-of-magnitude change of the subthreshold current, is then obtained as [5],

$$S = \left[\int_{y=-t_{Si}/2}^{t_{Si}/2} n_m(y) \frac{\partial \varphi_{\min}(y)}{\partial V_{GS}} dy \Big/ \int_{y=-t_{Si}/2}^{t_{Si}/2} n_m(y) dy \right]^{-1} \frac{kT}{q} \ln 10, \quad (1)$$

where $n_m(y)=n_i \exp[\varphi_{\min}(y)q/kT]$, n_i is the intrinsic electron concentration, $\varphi_{\min}(y)$ is the potential profile at the virtual cathode.

2.1 Symmetric DG MOSFETs

Exploiting (1), a detailed study on subthreshold swing's dependence on the channel doping concentration [2] reveals that subthreshold swing in short-channel DG MOSFETs can be closely described by a concept of effective conducting path, i.e., its location with respect to the gate. In undoped symmetric DG devices, the effective conducting path is found in-between the channel surface and the channel center because of symmetry and the

minuscule amount of ionized dopant atoms [2]. As a result, (1) can be greatly simplified without comprising much accuracy [2],

$$S = \left(1 - 2\Gamma_1 \cos\frac{t_{Si}}{4\lambda_1} e^{-\frac{L}{2\lambda_1}}\right)^{-1} \frac{kT}{q}\ln 10 \cdot \quad (2)$$

The new S model is compared to previous models and Medici numerical simulations with improved agreement (Figure 2). Ideal subthreshold swing is achieved at large channel lengths, which is explained by ideal gate-to-gate coupling through the dielectric-like undoped channel [6]. The parameter λ_1 is a scale length and can be approximated as [2],

$$\lambda_1 = \frac{t_{Si} + \varepsilon_{Si} t_{ox} / \varepsilon_{ox}}{1 + \pi/2} \quad or \quad \lambda_1 = \frac{t_{Si} + \sqrt{2}\varepsilon_{Si} t_{ox} / \varepsilon_{ox}}{\sqrt{2} + \pi/2}, \quad (3)$$

for $(\varepsilon_{Si} t_{ox}/\varepsilon_{ox} t_{Si}) \leq \pi/2$ and $> \pi/2$, respectively. It provides an efficient guideline in selecting appropriate t_{ox} and t_{Si} values for device designs (Figure 3).

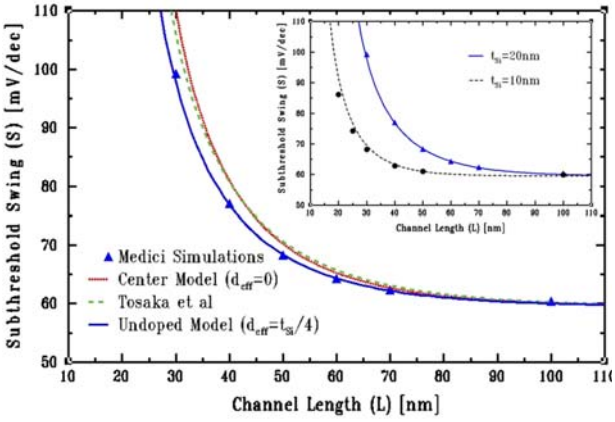

Figure 2: S roll-up in undoped SDG MOSFETs [2].

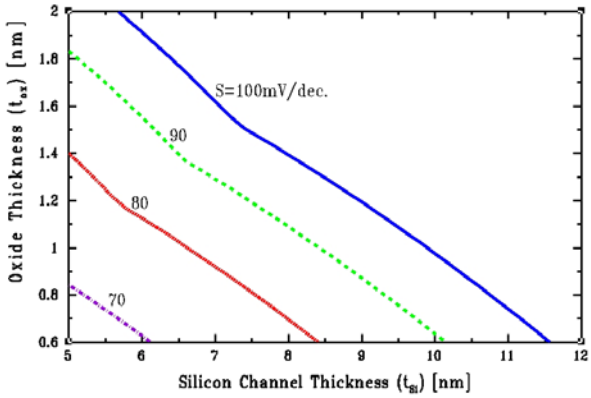

Figure 3: Design contours of a 15 nm undoped symmetric DG MOSFETs for different S requirements [**2**].

2.2 Asymmetric DG MOSFETs

Based on the concept of effective conducting path, (1) can be similarly simplified for asymmetric devices [5],

$$S = \left[1 - 2\Gamma_1 \frac{(V_1 + V_{DS}/2)}{\sqrt{V_1(V_1 + V_{DS})}} \cos\frac{d_{eff}}{\lambda_1} e^{-\frac{L}{2\lambda_1}}\right]^{-1} \frac{kT}{q}\ln 10, \quad (4)$$

where d_{eff} is the location of effective conducting path, and is a more complex and sensitive function of gate work-functions and device geometry than in SDG devices [5]. In general, because of asymmetry of the channel potential profile, the effective conducting path is found to be closer to the gate in ADG MOSFETs than in symmetric ones of the same geometry, resulting in a stronger gate control over the channel, and consequently, a slightly smaller S (Figure 4). The slightly improved subthreshold swing of ADG devices may translate into a higher drive current than in SDG ones for a normalized off-current.

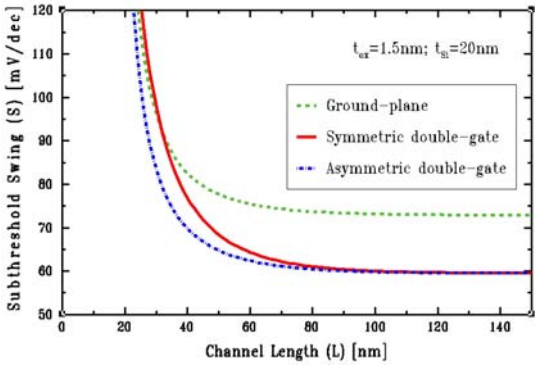

Figure 4: Comparison of subthreshold swing in SDG, ADG, and GP MOSFETs [5].

2.3 Ground-plane MOSFETs

The subthreshold swing of GP MOSFETs is obtained from (1) as,

$$S = \frac{kT}{q}\ln 10\left[\frac{1}{2} - \frac{r}{r+2}\frac{d_{eff,linear}}{t_{Si}} - \Gamma_1 e^{-\frac{L}{2\lambda_1}} \frac{V_1 + V_{DS}/2}{\sqrt{V_1(V_1 + V_{DS})}} \cos\frac{d_{eff}}{\lambda_1}\right]^{-1}, \quad (5)$$

and can be comprehended by a combination of capacitor divider model and effective conducting path [5]. For long-channel and moderately short-channel designs, GP MOSFETs demonstrate a significantly larger subthreshold swing than both SDG and ADG devices (Figure 4).

3 THRESHOLD VOLTAGE MODELS

It has been observed that the concentration of inversion carriers can exceed that of ionized dopant atoms under the threshold condition in undoped devices [7, 8, 9, 10]. Inversion carriers, thus, need to be included for threshold

voltage calculations. Moreover, the conventional way of using the surface band bending equal to $2q\phi_B$, where $\phi_B=\ln(N_A/n_i)kT/q$, to define the threshold condition becomes irrelevant. An alternative is to define the threshold voltage as the gate voltage at which the sheet density of inversion carriers reaches a value of Q_{TH} adequate to identify the turn-on condition [11]. Such a definition is equivalent to the constant-current V_{TH} measurement widely used both in experiments and simulations.

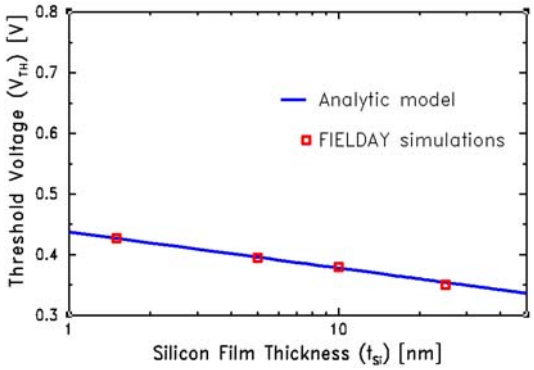

Figure 5: Long-channel V_{TH} vs. t_{Si} in SDG MOSFETs. Mid-gap gates are assumed [11].

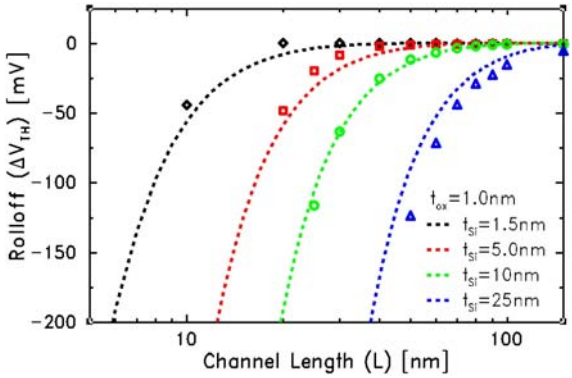

Figure 6: V_{TH} rolloff in mid-gap SDG MOSFETs [11].

3.1 Symmetric DG MOSFETs

A 2-D Poisson equation with only the mobile charge term included is analytically solved in the near-threshold region for SDG MOSFETs [11]. The potential profile at the virtual cathode is then determined, which, through the sheet density of inversion carriers, leads to a general short-channel threshold voltage model [11],

$$V_{TH}=\Phi_{MS,i}+\eta\frac{kT}{q}\frac{\cosh(\theta)}{\cosh(\theta/2)}\ln\left(\frac{Q_{TH}}{n_i t_{Si}}\right)-\left[\frac{\cosh(\theta)}{\cosh(\theta/2)}\eta-1\right]\varphi_{0m}, \quad (6)$$

where $\Phi_{MS,i}$ is the gate work-function referenced to the intrinsic silicon. At large channel lengths, (6) readily reduces into a long-channel V_{TH} model,

$$V_{TH,long}=\Phi_{MS,i}+\frac{kT}{q}\ln\left(\frac{Q_{TH}}{n_i t_{Si}}\right). \quad (7)$$

Models (7) and (6) are compared with published FIELDAY numerical simulations [12] with close agreement (Figure 5 and Figure 6). The slight dependence of long-channel V_{TH} on t_{Si} is caused by the volume inversion effect [11].

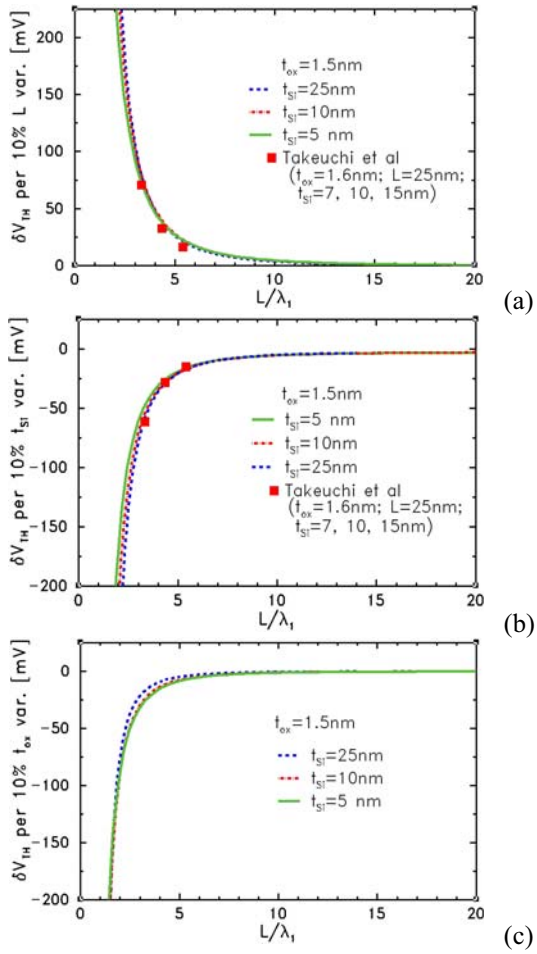

Figure 7: V_{TH} change versus the ratio of L/λ_1 caused by 10% increase of (a) L, (b) t_{Si}, and (c) t_{ox} [11].

An interesting application of the analytical *short*-channel V_{TH} model is to perform *quantitative* threshold voltage sensitivity analyses of DG MOSFETs in a more thorough and easier way than from numerical simulations, and so the effects of process variation can be assessed relatively easily. It was discovered [11] that the normalized V_{TH} sensitivities, $\delta V_{TH}/(\delta X/X)$, where X stands for L, t_{Si}, or t_{ox}, and $\delta X/X$ is its process tolerance expressed in percentage, can be represented, with reasonably good accuracy, by three unified, unique functional dependences on L/λ_1 for virtually all (L, t_{Si}, t_{ox}) designs (Figure 7). It enables a convenient and exhaustive study of the impact of process variations across technology nodes. For practical device designs (with L/λ_1 around ~4.5 to ~7) L causes 30%

to 50% more V_{TH} variation than does t_{Si} for the same process tolerance, while t_{ox} causes the least, relatively insignificant amount of V_{TH} variation.

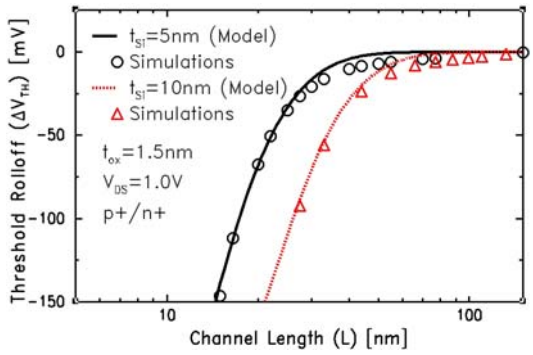

Figure 8: Threshold voltage rolloff in ADG devices [13].

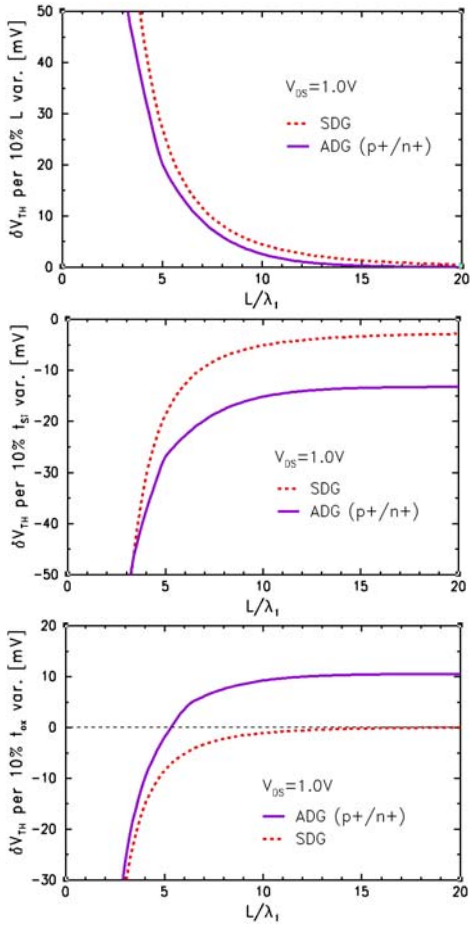

Figure 9: V_{TH} variations per 10% increase of L, t_{Si}, and t_{ox}: symmetric versus asymmetric devices [13].

3.2 Asymmetric DG MOSFETs

The effect of inversion carriers on threshold voltage calculations in asymmetric devices is included by a bi-sectional approach to computing the potential profile at the virtual cathode [5], which leads to a simple, although explicit, short-channel V_{TH} model [13],

$$V_{TH} = \Phi_{MS,i,F} + \phi_{MAX} + (kT/q) n_i t_{Si} \exp(q\phi_{MAX}/kT) / Q_{TH} r \cdot \quad (8)$$

Model (8) is compared to Medici simulations with close agreement (Figure 8).

Applying the new V_{TH} variation analysis technique, V_{TH} sensitivities in ADG MOSFETs are investigated and compared to those in SDG devices (Figure 9). For practical designs of p+/n+ ADG devices, t_{Si} causes 35% to 100% more V_{TH} variation than L does for the same process tolerance. While ADG devices show a slightly smaller sensitivity to L than SDG devices, they may be more prone to t_{Si} and t_{ox} variations, particularly, in relatively long-channel designs.

3.3 Ground-plane MOSFETs

In ground-plane MOSFETs, the threshold voltage essentially represents a pair of signal-gate voltage and constant-bias voltage [5]. Depending upon the gate voltage combinations, the potential profile under the threshold condition can be strongly asymmetric, moderately asymmetric, or symmetric. Therefore, the threshold voltage model for GP MOSFETs is developed as a hybrid of V_{TH} models for symmetric and asymmetric devices (Figure 10). Region I seen in Figure 10 is undesirable because of very weak control of the signal gate over the channel, which is explained by the fact that strong inversion is found along the channel surface near the constant-bias gate. The moderate dependence of V_{TH} on constant-bias voltage found in Region II may be exploited to compensate for process induced V_{TH} variations.

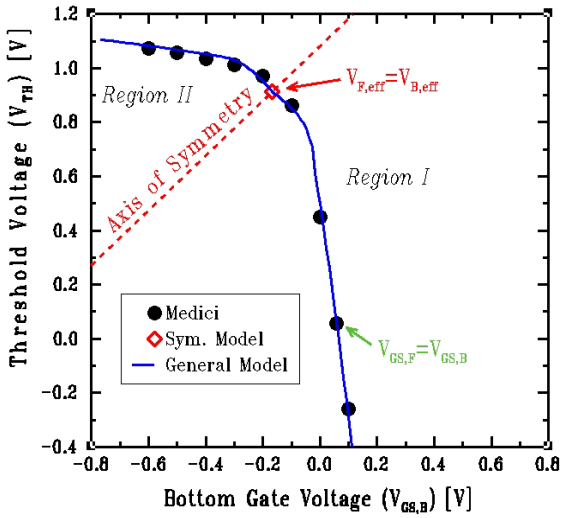

Figure 10: V_{TH} versus constant-bias gate voltage. t_{Si}=20 nm, t_{ox}=1.5 nm, and L=30 nm with p^+/n^+ polysilicon as front and bottom gates, respectively [5].

4 SCALING LIMITS PROJECTIONS

Scaling limits of DG MOSFETs are projected on the example of symmetric devices based on three scaling criteria: 1) an excellent turn-off behavior of S=70 mV/dec, 2) a moderate turn-off behavior of S=100 mV/dec, and 3) 70 mV maximum V_{TH} change caused by 30% L-equivalent process tolerance (to which all process variations are converted) [11]. As seen in Figure 11, individual DG MOSFETs with satisfactory turn-off characteristics are feasible with L as short as ~10 nm (~12 nm for S=70 mV/dec and ~7 nm for S=100 mV/dec). However, V_{TH} control, which is needed for gigascale integration of these devices, presents the biggest challenge for scaling, allowing L to be reduced only to ~16 nm.

5 QUANTUM MECHANICAL EFFECTS

It becomes clear in Figure 11 that 10 nm DG MOSFETs require ultra-thin silicon channel around 3 nm and ultra-thin gate oxide around 1 nm. Carrier confinement in such a thin silicon film becomes significant, leading to energy quantization and carrier re-distribution. Taking into account both the band structure of silicon and the quantization effect, a quantum mechanical threshold voltage model has been developed for symmetric DG MOSFETs [14],

$$\Delta V_{THLong} = \frac{E_g}{2q} + \frac{kT}{q}\ln\left(n_i t_{Si}\right) - \frac{kT}{q}\ln\left[\sum_{i=1}^{2} g_i \frac{m_{D,i}^{*}}{\pi\hbar^2} kT \sum_j \exp\left(-\frac{E_{j,i}}{kT}\right)\right], \quad (9)$$

which is compared to DESSIS numerical simulations with close agreement (Figure 12). In general, multiple subbands are needed for model calculations. As t_{Si} decreases below 3 nm, quantization becomes so strong that the lowest subband alone seems to suffice. Quantum mechanical effects dramatically increase V_{TH}'s sensitivity to t_{Si} as it decreases, and t_{Si} outgrows L as the largest source of parameter variations at t_{Si}=2 nm (Figure 13).

6 IMPACT OF HIGH-K DIELECTRICS

High-permittivity (high-κ) dielectrics have been proposed to replace SiO_2 as the gate oxide to alleviate the increasingly large gate tunneling current. A much thicker gate dielectric layer that results, however, leads to fringe fields in the non-ideal parallel-plate gate-insulator-channel structure, which weakens the gate control over the channel and consequently exacerbates SCEs. Incorporating the fringe-induced barrier lowering effect (FIBL), a short-channel V_{TH} model with high-κ dielectrics has been derived for symmetric DG MOSFETs [15],

$$V_{TH} = \Phi_{MS,i} + \eta\frac{kT}{q}\frac{\cosh(\theta)}{\cosh(\theta/2)}\ln\left(\frac{Q_{TH}}{n_i t_{Si}}\right) - \left[\frac{\cosh(\theta)}{\cosh(\theta/2)}\eta - 1\right]\left(\varphi_{0m} + 2.39\frac{kT}{q}\frac{t_I}{t_{Si}}\ln\frac{\varepsilon_I}{\varepsilon_{SiO_2}}\right), \quad (10)$$

where t_I and ε_I are the thickness and permittivity of gate dielectric. Applying a concerted analysis of FIBL-enhanced SCEs and gate direct tunneling current, candidate high-k gate dielectrics are assessed on their impact on DG MOSFETs' scaling limits (Figure 14). High-k gate dielectrics may extend DG MOSFET scaling beyond that with SiO_2, but the amount of channel length reduction is probably less than 20%.

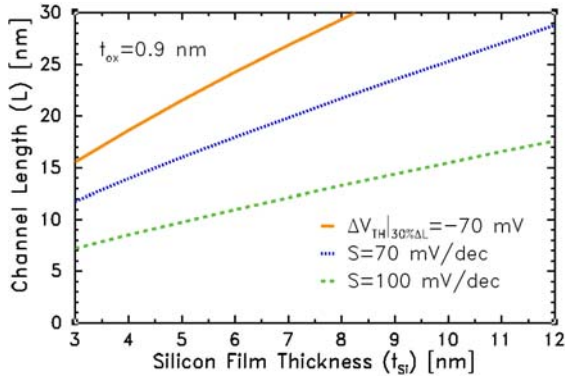

Figure 11: Scaling limits: L versus t_{Si}. [11].

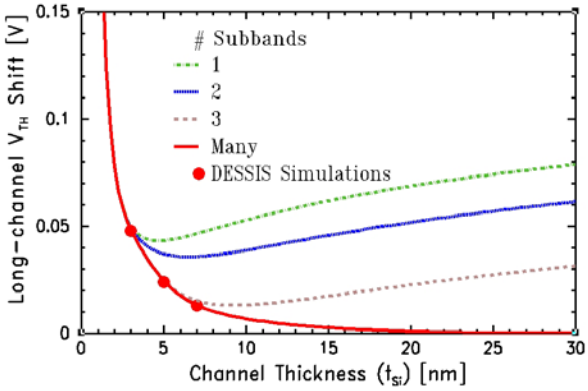

Figure 12: Quantization-based long-channel threshold voltage shift versus silicon channel thickness [14].

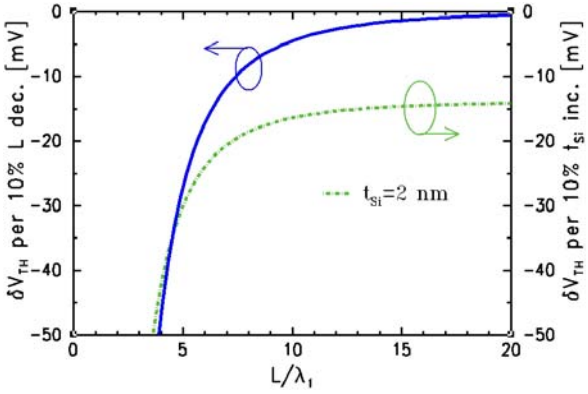

Figure 13: Overall V_{TH} change per 10% decrease of L (left) versus that per 10% increase of t_{Si} (right) as unified functions of the ratio of L/λ_1 [14].

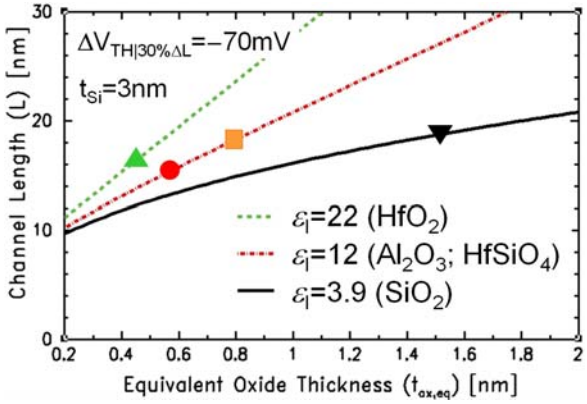

Figure 14: *L* versus EOT. Symbols mark minimum L's determined by minimum EOTs (allowed for gate tunneling current): ▼- SiO_2; ■ – $HfSiO_4$; ● - Al_2O_3; ▲ - HfO_2 [15].

7 CONCLUSIONS

Compact, physics-based models of subthreshold swing and threshold voltage are presented for undoped double-gate MOSFETs in symmetric, asymmetric, and ground-plane modes. While both symmetric and asymmetric DG MOSFETs have nearly ideal subthreshold swing at large channel lengths, ground-plane MOSFETs have significantly larger subthreshold swing. Subthreshold swing of ADG MOSFETs is slightly smaller than that of SDG devices. Based on a unique, scale-length based methodology, threshold voltage variations are analyzed comprehensively and exhaustively. In SDG MOSFETs, *L* causes 30% to 50% more V_{TH} variation than does t_{Si} for the same process tolerance. Contrarily, t_{Si} causes 35% to 100% more V_{TH} variation than *L* does in p+/n+ ADG devices. Quantum mechanical effects on threshold voltage have been analytically modeled. Multiple subbands are in general needed for model calculations, while the lowest subband alone seems to suffice for t_{Si} less than 3 nm. Fringe-induced barrier lowering effect has been modeled and included in the threshold voltage model for SDG MOSFETs. A concerted analysis of FIBL-enhanced SCEs and gate direct tunneling current shows that high-permittivity dielectrics may be helpful to reduce the channel length, but probably by less than 20% compared with SiO_2. Finally, scaling limits projections indicate that individual DG MOSFETs with good turn-off behavior are feasible at 10 nm scale; however, practical exploitation of these devices toward gigascale integrated systems requires development of novel technologies for significant improvement in process control.

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