Modeling and Characterization of On-Chip Inductance for High Speed VLSI Design

Narain D. Arora and Li Song
Cadence Design Systems, Inc., San Jose, CA, 95134, USA

ABSTRACT

Ever increasing circuit density, operating speed, faster on-chip rise times, use of low resistance Copper (Cu) interconnects, and longer wire lengths due to high level of integration in VLSI chip designs, have necessitated the need for modeling of wire inductive (L) effects which were ignored in the past. In this paper we will review different approaches of modeling the on-chip wire inductance, and discuss practical methods of assessing the inductance with special reference to return path in an IC chip. This will be followed by discussion on impact of inductance on performance of high speed VLIS. We then cover methods of validating the models using test chip approach.

Keywords: On-chip inductance, inductance modeling, inductance characterization, inductance test structures.

1 INTRODUCTION

As operational frequency of IC chips with copper (Cu) interconnects increases towards multi-gigahertz (GHz) range, the on-chip inductance effects can no longer be ignored for the state of the art VLSI design. The inductive effect can cause ringing and overshoot problems in clock lines, and reflections of signals due to impedance mismatch. In addition, the switching noise due to inductive voltage drops is an issue for the power distribution network. Thus it is important to model inductive effects accurately for high speed VLSI design.

Inductance of a wire is more complicated to model compared to resistance or capacitance because the inductance describes the magnetic flux being generated by current flowing in a loop. In a VLSI chip, calculation of wire inductance will therefore require knowledge of the current return path. However often the return path is not easily identified as it is not necessarily through the silicon substrate. Calculation is further complicated by the fact that not all the return currents follow DC paths as some are in the form of displacement current through the interconnect capacitances. Furthermore, unlike capacitive coupling, inductive coupling has long range effects because the magnetic field strength decreases much slowly compared to the electric field strength. As such localized windowing (nearest neighbor approximation) commonly used for capacitance calculation may not be valid for inductance calculation [1].

In section 2, we review different approaches of modeling the wire inductance, followed by discussions in section 3 on practical methods of assessing the inductance with special reference to return path in an IC chip. Section 4 covers methods of characterizing on-chip inductance and validating the models using test chip approach.

2. EFFECT OF INDUCTANCE ON IC DESIGN

Unlike line capacitance that is directly proportional to the length of the interconnect, inductance effect in an IC chip is length dependent. The length range where on-chip inductance is important is given by the following bound [2, 3]:

$$\frac{t_r}{2\sqrt{LC}} < l < \frac{2}{R}\sqrt{\frac{L}{C}} \tag{1}$$

As technology advances, with faster on-chip rise time, higher clock frequencies and the use of Cu wires as interconnect, the range of wire length where inductance is important becomes larger [4] (Fig. 1). For wires of a VLSI chip in this range, the use of RCL models as a distributed network becomes a necessity. Even more critically, a RCLK model, in which not only self inductance L, but the mutual coupling inductance K is considered, is needed. In fact, the inclusion of K becomes more important for technology node of 90nm and below. Figure 2 shows the results of simulation using 3 different interconnect delay modes [5]. The importance of mutual inductive coupling (RLCK model) is evident.

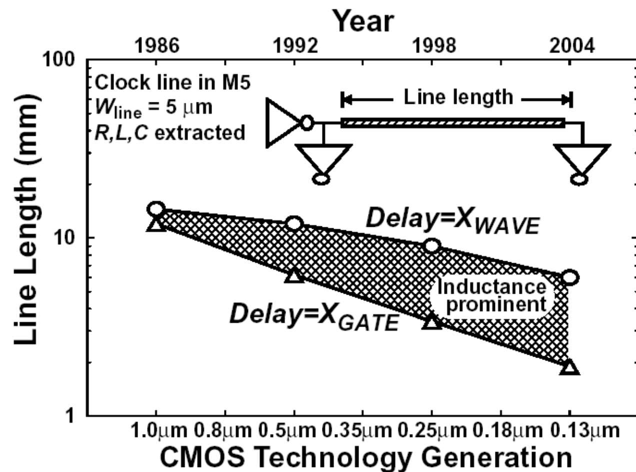

Fig. 1 Inductive effects vs. technology scaling. After Qi. et al. [4].

Traditionally, the inductance extraction and molding problem has been suppressed by design strategies, which minimize the formation of significant long-range inductance on chip. One straightforward approach is that wiring layers containing lines with high current density are sandwiched in between isolating metal planes above and

below [6]. With ground planes sufficiently close, the magnetic field is blocked and the couplings to adjacent layers and crosstalk are effectively suppressed [7]. By knowing current return paths, calculation of the loop inductance is easy. However, the isolating layers add significantly to the capacitive coupling of the surrounding lines which adversely impacts the speed and power dissipation of the circuitry.

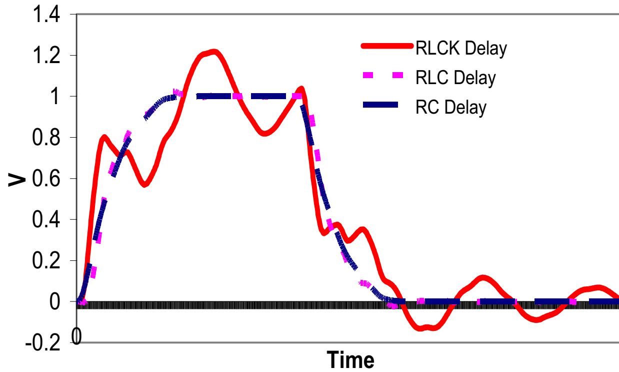

Fig. 2 Signal bus inductive noise simulation using various delay models

Another selective method of reducing inductance between high current wires is to introduce additional inverters in the lines at regular intervals [6]. This causes the current to change direction in each adjacent interval, thus the self inductance of the entire line is reduced significantly. At such point, the RC propagation dominates and inductance models are no longer required. However this approach can be costly in terms of IC area, performance and power consumption [8].

Scaling scheme has been proposed [9] to extend the current design tools and methodologies to cope with inductive effects of future technologies. The scheme includes the optimization of driver size, buffer area, and interconnects line width and length. The critical interconnect length l_{crit} for which the interconnect is neither over-damped nor under-damped can be obtained for a uniform distributed RLC line as a function of interconnect geometry and input vector. For each technology node, while keeping the aspect ratio and interconnect pitch as depicted by ITRS, global line widths are varied until l_{crit} vs. l plot coincides with the 180nm technology case, ensuring inductive effects remain constant across technology nodes. However the increase of the minimum wire width as a result of this scaling scheme creates wireability problem and may increase metal layer numbers and chip area.

Despite problems such as unwanted ringing and overshooting, reflection of signals and switching noise caused by inductive effect, the inductive behavior of the wire can be exploited for new concepts that benefit high-speed circuit design [10].

3. INDUCTANCE MODELING

Inductance, by definition, is for a loop of a wire, wider the current loop, higher the inductance,

$$L_{i,j} = \frac{\psi_{ij}}{I_j} \tag{2}$$

where Ψ_{ij} represents the magnetic flux in a loop i due to a current I_j in loop j The re are different methods of modeling inductance effect of a wire. The most accurate one is based on Maxwell equations, the so called field solver approach, but is not suitable for circuit level inductance calculation. At the chip level different approaches are used and discussed below.

3.1 Field Solver

The modeling and calculation of inductance of a wire in an IC chip requires knowledge of the return path(s). Three dimensional (3-D) field solvers are used to extract inductance using following current integral equation without the need to know the actual return paths,

$$\frac{J(r)}{\sigma} + \frac{j\omega\mu_0}{2}\int_V \frac{J(r')}{|r - r'|}dr' = -\nabla\Psi(r) \tag{3}$$

where V is the volume of the conductors, r' is the source point vector, ω is the frequency and μ_0 is the free space permeability.

Finite difference or finite element methods are applied to the governing Maxwell equations in differential form to calculate magnetic flux Ψ and current density J, hence L using Eq. 2. The Maxwell equation approach generates a global 3-D mesh that makes it impractical to extract complex 3-D structures such as the one encountered in a VLSI chip.

Sometimes inductance matrix [L] is derived directly from the capacitance matrix [C] such that $[L] = [C]^{-1}/\nu_0^2$, where ν_0^2 is the phase velocity of the medium. Because the relation holds only for ideal transmission lines, with perfect conductor and perfect dielectric, it will result in underestimation of the on chip wire inductance [3].

3.2 Partial Inductance/PEEC Method

At IC chip level, it is not clear which conductor forms the loop, and the return path is not easily identified. An effective way of analyzing inductive effect of complex wire structures is the partial inductance (PI) method, in which the current is assumed to return at infinity [11]. The infinite loop cancels out when two line segments are subtracted and the determination of the returning path for each wire is not required. Based on PI approach, the self, mutual inductances of two parallel lines of length l, width w, and thickness t, separated by distance d are:

$$L_{self} = \frac{\mu_0}{2\pi}\left[l.\ln\left(\frac{2l}{w+t}\right) + \frac{l}{2} + 0.2235(w+t)\right] \quad (4)$$

$$M = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{d}\right) - 1 + \left(\frac{d}{l}\right)\right] \quad (5)$$

Extending the PI approach to on-chip inductance calculation, the so called Partial Element Equivalent Circuit (PEEC) method [11-13], determines the inductance associated with each wire by breaking it into segments and then calculating self-inductance associated with each wire segment and mutual inductance associated with each pair of wire segments. Because of the long range influence of magnetic field, the inductance matrix is usually very dense and simulation of this scale may not be practical for every wire at chip level. Therefore, this method is often used to extract wire inductance for critical nets only.

Based on PEEC model, a frequency dependent inductance and resistance extractor (FastHenry) was developed [14]. The method divides conductors into filaments and solves for impedance matrix using accelerated multi-pole approach. Figure 3 is a simulation of the inductance vs. frequency of a signal line with multiple coplanar return paths, here w = 0.5μm, s = 0.5μm, h = 0.8μm and l = 1000μm. In this figure, the low frequency inductance value holds up to 1GHz before it starts to decay to coplanar two line return (CTR) model as shown in the figure. In the presence of 32 return paths, the actual inductance is more than double that of the CTR model [15] for frequency up to 1GHz.

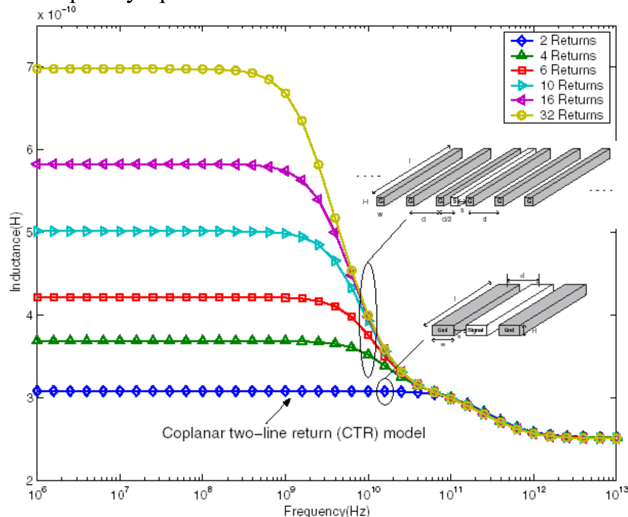

Fig. 3 Inductance vs. frequency using different number of return paths [14].

3.3 Loop Inductance

The formidable dense inductance matrix has prompted the returning of loop inductance approach to extract L for today's VLSI designs. The loop inductance model can be used to find the inductance effect, if the return path is known or can be estimated. The model is suitable for well designed IC structures, such as clock nets shielded by power/grounding wires next to them. For a structure of a single line over power grid, inductive interaction within every segment surrounding a signal line can be incorporated into an effective loop inductance L_{eff} [16]. Excellent linearity is observed for high frequency inductance because return current is mostly confined to the nearest power grid. The inclusion of up to the second nearest pair of grid is sufficient for less than 5% error in L_{eff}. The L_{eff} of diagonal wires over the power grid is insensitive to the relative location of the wires due to the fact that magnetic flux between the diagonal wires and the nearest power grid does not change much by changing the location of the diagonal wires [16].

Even with exact return path unknown, the Min/Max loop inductance estimation can provide an insight into inductance effects of a VLSI design [17]. The loop inductance of two wires is given as:

$$L_{loop} = L_1 + L_2 - 2M \quad (6)$$

where L_1 and L_2 are the partial self inductances and M is the partial mutual inductance. Note that the minimum loop inductance occurs when the mutual inductance is at its maximum, or the returning paths are provided at the nearest possible location. Assuming a constant layer thickness, the optimal spacing and wire width values can be calculated. As expected, the minimum loop inductance occurs when the spacing between the signal and ground wires is minimum. The optimal width of the ground wire is a function of the signal wire width, thickness and spacing [17]. An absolute upper bound for the loop inductance is obtained by assuming a return path at infinity with infinite width. In this case, the loop inductance is equivalent to the partial self inductance of the wire (see Fig. 4).

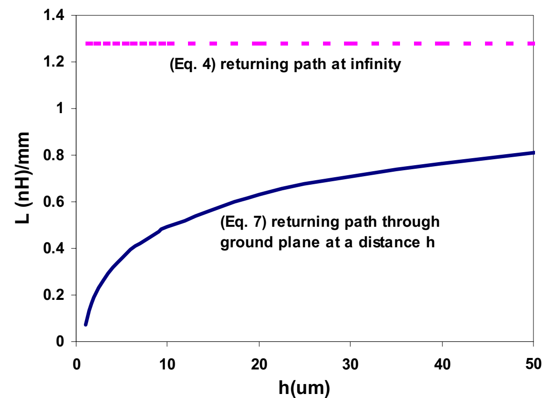

Fig. 4 Comparison of loop inductance with different returning paths (assuming W = 5μm, t = 0.5μm).

Inductance estimation can be obtained from formulations of the characteristic impedance for transmission lines and their relationship with distributed inductances. It has been shown that the loop inductance of a wire over a ground plane and the mutual inductance of two wires on a ground plane are [18]

$$L = 0.2 \ln\left(\frac{2\left(h + \frac{t}{2}\right)\pi}{w + t} \right) \text{ nH/mm} \quad (7)$$

$$M = 0.2 \ln\left(1 + \left(\frac{2\left(h + \frac{t}{2}\right)}{D} \right)^2 \right) \text{ nH/mm} \quad (8)$$

Where h is the wire height from the bottom of the wire to the ground plane. W and t are the width and thickness of metal wire, and D is the center to center wire separation.

Note that in Eq. 7 when the wire height increases, the loop inductance increases and approaches the upper bound which is defined by the self-inductance calculated using PEEC method (see Fig. 4).

3.4 Frequency Dependent Inductance Modeling

Inductance is frequency dependent as evident from Fig. 2. Ideally the frequency dependent parameters of general RLCG model in Fig. 5(a) should be used in the circuit simulation. However the frequency dependent parameters are not supported in many circuit simulators such as SPICE. A parallel RLC model (Fig. 5(b)) that consists of low-resistance, high-inductance path at low frequency, and high-resistance, low-inductance path at high frequency has been proposed [19] to incorporate the frequency-dependent behavior of an interconnect. Multiple parallel branches (Fig. 5(c)) are used to model inductance reduction at high frequency due to capacitive coupling of the signal line to random lines and power grids [20]. By introducing separate “slow-wave factor” (SWF) for parallel and crossing lines, and low-frequency (DC), moderate-frequency (MF) and high frequency (HF) parameters, the high frequency interconnect behavior can be modeled more accurately [20].

$$R_{\text{DC}} = R_1 \| R_2 \| R_3$$
$$L_{\text{DC}} = L_1 + \left(\frac{R_1}{R_1 + R_2 \| R_3} \right)^2 \left(L_2 + \left(\frac{R_2}{R_2 + R_3} \right)^2 L_3 \right)$$
$$R_{\text{MF}} = R_1 \| R_2; \qquad L_{\text{MF}} = L_1 + \left(\frac{R_1}{R_1 + R_2} \right)^2 L_2$$
$$R_{\text{HF}} = R_1; \qquad L_{\text{HF}} = L_1. \quad (9)$$

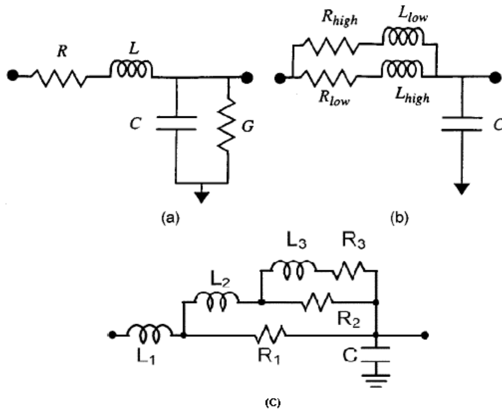

Fig. 5 (a) Telegrapher’s equation RLGC model (b) Parallel RCL model [19], (c) Frequency dependent RCL model [20]

4. INDUCTANCE CHARACTERIZATION USING TEST STRUCTURES

The only way to validate inductance extraction, and investigate the inductive effects accurately is to use test chip. Investigations of noise and delay values as functions of interconnect length, width and spacing, under lumped or distributed gate loading, and inductive effects in the presence of various returning paths including substrate, coplanar structures, under layers, power grid, ground bus, and random structures can be performed using test structures. Either direct time-domain approach such as using ring oscillators or frequency-domain measurement such as S-parameter characterization can be used to analyze on-chip inductance.

A ring oscillator in which two legs of the oscillator traverse a reasonably long interconnect path was used to study the performance of a given system of conductors [21]. The conductor configuration consists of aggressor wires and a victim wire. Different cases were studied as 1) no nearby return paths exists, 2) effects of a reference plane, and 3) various signal to return ratios with various return widths. The circuit enables the effects of inductance on delay and overshoots to be measured on the aggressor wires and induced noise to be measured on the victim wire. The loop frequency and noise level measurement showed excellent correlation to the simulation results. The results demonstrated significant overshoot if no nearby return paths were provided.

Ring oscillators were also used for characterizing the ratio between effective driver resistance and characteristic impedance of the wire [19]. Two different configurations of ring (loop) are used to study this behavior as shown in Fig. 6. The mismatch between the wire and the driver will result in overshoot and ringing.

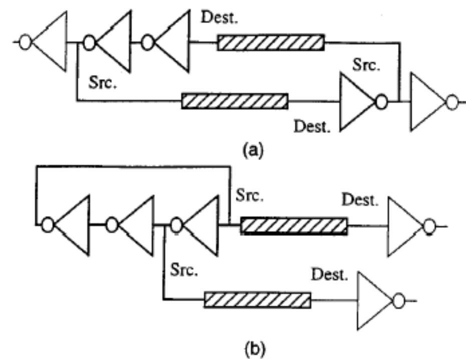

Fig. 6 Ring oscillators with connections at (a) destination (b) source [22].

Inductance-Oscillator whose oscillation frequency is determined by the wire inductance has also been developed to quantitatively evaluate inductance impact on on-chip interconnect delay [22]. It consists of a ring oscillator, long signal lines and on-chip frequency counter. The long signal lines have equal parasitic capacitance and resistance but

different loop inductance. Each structure includes different signal power supply and ground wire configuration, and each long signal line employs a coplanar wave guide configuration. The equivalent distance to the nearest ground grid, which serves as the current return path is varied to control wire inductance. The measurement results suggest that if an insufficient ground were used, unpredictable timing difference due to inductance may arise even for coplanar structures.

Frequency domain S parameter characterization is carried out by launching waves from both ends of a signal line and measuring the reflected (S_{11}) and transmitted (S_{21}) network parameters using a network analyzer over the frequency range up to 50-100GHz. Dummy open structures are required to de-embed the pad parasitics. Telegrapher's parameters (RLGC) or various frequency-dependent RLC models parameters (such as R1, L1, R2, L2, etc. as shown in Fig. 4) can be extracted from S parameters results [19-20, 23-24].

Interconnect transmission line effects due to the characteristics of a silicon substrate, ground planes, co-planar lines and power/ground grids were studied and characterized using S parameter measurement [4, 19, and 25]. Measurement results and FastHenry simulation show that at low frequency, most current returns through the minimum resistance path, the current uses as many return paths as possible, and often through the nearest ground wires. The inductance increases for increasing spacing between the wire and the nearest ground wires of the co-planar structure because more flux is enclosed between the signal and the return ground. At higher frequency, current return path is to minimize loop inductance. The inductance is decreased due to the proximity effects between the wires as well as between the wire and the substrate. Time-varying magnetic fields coupled to the substrate generate eddy currents that offer a portion of the current return paths. With eddy current, the substrate, even power grid and random lines can reduce inductance.

For VLSI chip, power and ground are usually distributed through grid structure in order to minimize IR drop and reduce ground bounce. Due to proximity effects, the nearest power and ground wires provide the return paths for most of the signal current through coupling. With substrate excluded, multiple parallel (with signal line) ground wires in ground grids reduce signal wire inductance by providing multiple current return paths. Floating wires do not affect the signal wire inductance if these wires are smaller than 20μm due to negligible eddy currents. However dense grid and ground planes can generate eddy current due to the existence of time-varying magnetic field. Whether the grid structure is floating or grounded does not make much difference in the wire inductance.

Using a test structure that consists of a set of pseudo-random signal lines that are connected to on-chip drivers to mimic a real chip (Fig. 7), the inductance effects were studied and compared to the conventional co-planar wave guide structures [18-19]. The results showed that random signal lines and power grids reduce high-frequency inductance significantly by providing closer return paths through capacitive coupling. The signal lines could couple inductively to the parallel random lines which effectively reduces the line inductance. They can also couple capacitively to the orthogonal random lines that in turn connect or couple to parallel random lines. Whether the drivers of the random lines are on or off does not significantly affect the inductance because the nature of capacitive couplings to the power grid and signal lines.

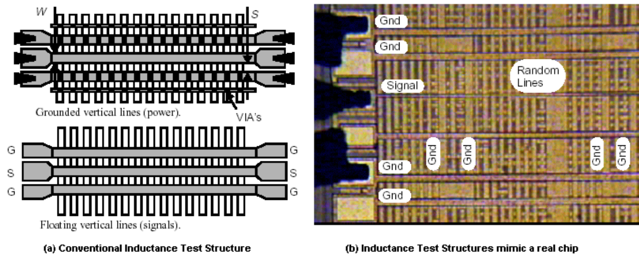

Fig. 7 Inductance test structures [18] (a) conventional (b) mimic a real chip

Due to its low resistance value, the inductive effects of Cu wires are expected to be different from those of Al wires. Figure 8 is the micrograph of inductance test structures designed to study 90nm Cu inductive effects for various current return paths such as co-planar structures, ground plane, power grid, as well as random structures. The results will be reported after the availability of the data.

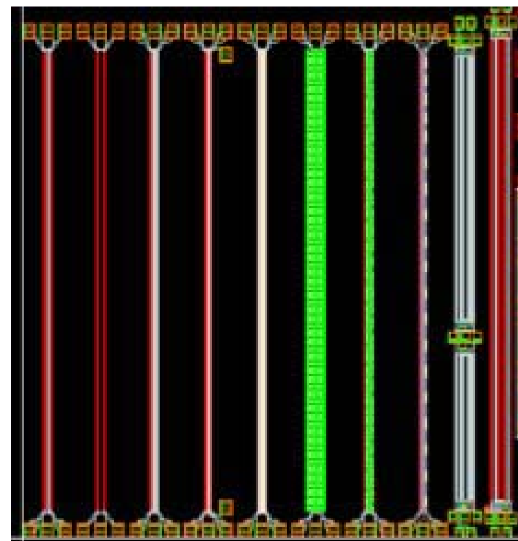
Fig. 8 Micrograph of inductance test structures designed for 90nm Cu process

5. CONCLUSION

The inductance causes unwanted effects such as ringing, overshoot, cross-talk etc. in chip designs. The inductive effects are often suppressed during design using techniques and structures such as micro-strip line and co-planer strip

line. Inductance can be modeled using Field solvers, PEEC and loop inductance approaches. Due to the large inductance matrix associated with PEEC, the use of loop inductance approach has been revisited for today's VLSI design. The concept of effective loop inductance is compact and could be applied to extract the inductance of signal lines in the presence of random structures where return paths are difficult to be determined. Ultimately, inductance test structures are the only means of validating inductance models accurately. Using well designed test structures, one can characterize inductance of a wire in the presence of co-planar structures, ground planes, power grids, and random structures etc.

REFERENCES

1. N. D. Arora, "Challenges of Modeling VLIS interconnects in the DSM Era", *Proc. Modeling and Simulation of Microsystems,* pp.645-648, 2002.
2. Y. Ismail, E. G. Friedman and J. L. Neves, "Figures of merit to characterize the importance of on-chip inductance", *IEEE Tran. VLSI System,* Vol. 7, pp. 442-449, Dec. 1999.
3. Y. Ismail, and E. Friedman, "On-chip Inductance in High Speed Integrated-circuits", Kluwer Academic Publishers, 2001.
4. XQ B. Kleveland, G. Wang, ZYu, S. S. Wong, R. W. Dutton, and T. Furusawa, "High Frequency Characterization and Modeling of VLSI On-Chip Interconnects ", *Proc. of the Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI)*, Japan, Oct. 2001.
5. N. D. Arora, "Modeling and Characterization of Copper Interconnect for SoC Design", *Proc. SISPAD*, pp.1-6, 2003.
6. M. W. Beattie and L. T. Pileggi, "IC Analyses Including Extracted Inductance Models", *Proc. IEEE DAC*, pp. 915-920, 1999.
7. J. A. Davis, R. Venkatesan, A. Kaloyeros, M. Beylansky, S. J. Souri, K. Banerjee, K. C. Saraswat, A. Rahman, R. Reif, and J. D. Meindl, "Interconnect limits on gigascale integration (GSI) in the 21st century", *Proc. of IEEE* , Vol. 89, pp. 305-324, March 2001.
8. P. Kapur, G. Chandra, J. P. McVittie, and K. C. Saraswat, "Technology and Reliability Constrained Future Copper Interconnects - Part II: Performance Implication", *IEEE Tran. On Electron Dev.* Vol. 49, pp.598-603, April, 2002.
9. K. Banerjee and A. Me hrotra, "Inductance Aware Interconnect Scaling", *Proc. IEEE ISQED*, pp. 43-47, 2002.
10. S. S. Wong, P. Yue, R. Chang, S. Kim, B. Kleveland and F. O'Mahony, "On-Chip Interconnect Inductance –Friend or Foe", *Proc. IEEE ISQED*, pp. 389-394, 2003
11. A. E. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM J. Res. & Dev.*, Vol. 16, pp. 470, 1972.
12. P. A. Brennan, N. Raver and A. Ruehli, "Three dimensional inductance computations with partial element equivalent circuits", *IBM J. Res. & Dev.*, vol. 23, pp.661-668, Nov. 1979.
13. P. Restle, A. Ruehli and S. G. Walker, "Dealing with Inductance in High Speed Chip Design", *Proc. IEEE DAC*, pp. 904-909, 1999.
14. M. Kamon, M. Tsuk, and J. White, FastHenry: A Multi-pole Accelerated 3-D Inductance Extractions Program*", IEEE Trans. Microwave Theory and Techniques*, Vol. 42, No. 9 pp. 1750-1758, 1994.
15. S. Kim, Y. Massoud, and S. S. Wong, "On the Accuracy of Return Path Assumption for Loop Inductance Extraction for 0.1um Technology and Beyond", *Proc. IEEE ISQED*, pp. 401-404, 2003.
16. S. Sim, C. Chao, S. Krishnan, D. M. Petranovic, N. D. Arora, K. Lee and C. Y. Yang, "An Effective Loop Inductance Model for General Non-Orthogonal Interconnect with Random Capacitive Coupling", *Proc. IEEE IEDM*, pp. 315-318, 2002.
17. Y. Lu, M. Celik, T. Young, and L. Pileggi, "Min/Max On-Chip Inductance Models and Delay Metrics", *Proc. IEEE DAC*, pp. 341-346, June, 2001.
18. B. Kleveland, XQ L. Ma dden, R. W. Dutton, and S. S. Wong, "Line Inductance Extraction and Modeling in a Real Chip with Power Grid" *Proc. IEEE IEDM*, pp.901-904, Dec. 1999.
19. B. Kleveland, XQ L. Madde n, T. Furusawa, R. Dutton, M. A. Horowitz, and S. S. Wong, "High-frequency characterization of on-chip digital interconnects", *IEEE ISSC*, vol. 37, pp.716-725, June, 2002.
20. S. Sim, K. Lee, and C. Y. Yang, "High-Frequency On-Chip Inductance Model", *IEEE EDL*, Vol. 23, pp.740-742, December, 2002.
21. S. V. Morton, "On-chip Inductance in Multiconductor Systems", *Proc. IEEE DAC*, pp. 921-926, 1999.
22. T. Sato, and H. Masuda, "Design and Measurement of an Inductance-Oscillator for Analyzing Inductance Impact on On-chip Interconnect Delay", *Proc. IEEE ISQED*, pp. 395-400, 2003.
23. A. Deutsch, P. W. Coteus, G. V. Kopcsay, H. H. Smith, C. W. Surovic, B. L. Krauter, D. C. Edelstein, and P. J. Restle, "On-chip wiring design challenges for gigahertz operation", *Proc. IEEE*, Vol. 89, pp.529-555, April, 2001.
24. B. Krauter and S. Mehrotra, "Layout-based frequency dependent inductance and resistance extraction for on-chip interconnect timing analysis", *Proc. IEEE DAC*, pp. 303-308, 1998.
25. XQ B. Kleveland, ZYu, S. S. Wong, R. Dutton, and T. Young, "On-Chip Inductance Modeling of VLSI Interconnects", *IEEE ISSCC*, pp.172-173, Feb. 2000.