Inverse RIE Lag of Silicon Deep Etching

C.K. Chung and H.N. Chiang

Dep't of Mechanical Engineering, National Cheng Kung University,
Tainan, Taiwan 701, ROC, ckchung@mail.ncku.edu.tw

ABSTRACT

This paper reports for the first time that the phenomena and reaction mechanism of inverse reactive ion etching (RIE) lag occurs in the silicon deep RIE process without feature coalescence. This phenomenon is related to two important parameters of feature area and process pressure. Increasing the process pressure in different patterns with equivalent feature area will increase the etching rates as well the smaller width has higher increasing etching rate ratio. So, the smaller feature pattern has the chance to get higher etching rate than the larger one as the pressure increased is high enough. This will lead to three stages of RIE lag transition: reduced RIE lag, lag elimination and inverse RIE lag. A possible new reaction mechanism exists in the inverse RIE lag phenomena. The increasing etching rate ratio of different feature sizes is affected more obvious by C_xF_y radicals dissociated from C_4F_8 passivation gas than F radicals or SF_x ions dissociated from SF_6 etching gas.

Keywords: inverse, RIE lag, deep etching, ICP, MEMS

1 INTRODUCTION

Silicon deep reactive ion etching (DRIE) for deep and high aspect ratio microstructure is a very important technology in microfabrication and microelectromechanical system (MEMS) industry [1-3]. RIE lag in ICP etching is a frequently seen defect in semiconductor or microfabrication processes and appears in MEMS feature sizes up to hundreds of micrometers. It will affect the etching micro-uniformity and is much dependent on the pattern geometry. The effect is more severe as the feature width becomes smaller. Many publications reported the related study of silicon DRIE including effect of process parameters [4, 5] and pattern shape [6, 7] on RIE lag, 2D simulator [8], and curved surface using RIE lag [9]. For example, Jansen et al. [4] reported that RIE lag could be improved by lower pressure. Ayon et al. [5] proposed that high SF_6 flow rate, the dominant variable, can minimize RIE lag. Kiihamaki et al. [6] reported that the RIE lag is related to the feature length-to-width ratio (L/W ratio), width and pattern shape. Jiao et al. [7] proposed that the etching rate under silicon deep etching process is much affected by the mask layout related area including the other features around it. All reports are related to the normal RIE lag, no inverse RIE lag and less discussion on area effect. In this paper, we report the special inverse RIE lag phenomenon in DRIE process correlated to the effect of area and pressure parameters. It will be much helpful for the process control of etching uniformity, 2D-3D simulator establishment, and the application for different level or curved surface device.

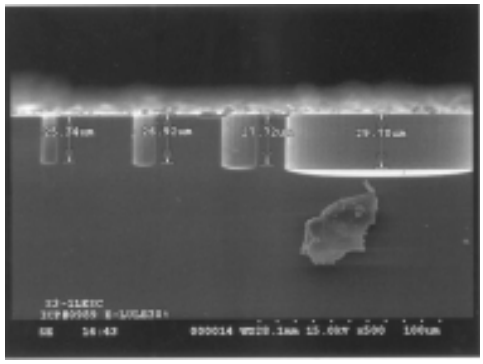
2 EXPERIMENTAL PROCEDURE

Boron-doped p-Si(100) wafers of 4- 10 Ω-cm were initially cleaned in the H_2SO_4:H_2O_2 = 3:1 solution. Standard lithography was used to transfer the photo mask pattern to silicon surface and the etching mask was photoresist. The different feature geometry of rectangles, squares, circles and donuts is designed to realize how the pattern geometry dimension affects the ICP etching properties. Three major kinds of patterns of constant length, constant width and constant area with different feature sizes of 2 to 100 μm are divided to understand the dominating factor of geometry for RIE lag in ICP etching. Silicon DRIE was performed by ASE™ process in STS Multiplex ICP system [10-11]. The etching and passivation gases were SF_6 and C_4F_8 respectively and switched during the process. Little O_2 was added to SF_6 during etching process. Process pressure was adjusted by auto pressure control (APC) from 30% to 75% to understand the process pressure effect on RIE lag. The plasma source was generated by 600 W 13.56 MHz RF generator and biased by 10- 14 W 13.56 MHz RF generator at platen during the etching step. The wafer was electrostatically clamped and cooled by backside helium flow. Scanning electron microscope (SEM) was used to examine the etching result after ASE™ process.

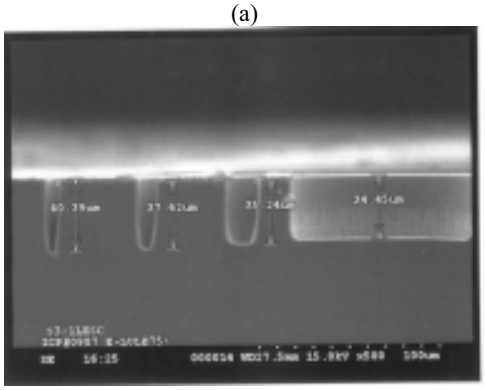
3 RESULTS AND DISCUSSION

Figures. 1(a) and 1(b) show the SEM micrographs of the etched donut trench with constant area of of $\pi \times 52.5^2$ μm^2 at pressures of APC (a) 30% and (b) 75%, respectively. The RIE lag exists at low pressure of APC 30% while an inverse RIE lag appears at much high pressure of APC 75%. Normal RIE lag of trenches at constant length in Figure 2 shows that smaller feature size leads to lower etching rate. Increasing process pressure to the feature in Figure. 2, we still get the RIE lag, not inverse RIE lag. Figures 3(a) and 3(b) show the etching depth of trenches with feature length from 100 to 500 μm at constant width of 5-10 and 25 μm, respectively. The etching depths of trenches are nearly the same at the identical feature width and vary with width dimension. For example, the etching depth is 57.91 μm for the fixed feature width of 5 μm while the etching depth is 64.35 μm for the fixed feature width of 10 μm as shown in

Figure 3(a). And the etching depth is 72.76 μm for the fixed feature width of 25 μm, Figure 3(b). The etching depth of rectangular trench increases with the increasing feature width and is insensitive to the feature length. It indicates that the feature width of pattern geometry is a dominating factor affecting the RIE lag in ICP etching.



(a)



(b)

Figure 1 SEM micrographs of the etched donut trench with constant area of π x 52.5^2 μm^2 at pressures: (a) APC 30% and (b) APC 75%, respectively. The RIE lag exists at low pressure of APC 30% while an inverse RIE lag appears at much high pressure of APC 75%.

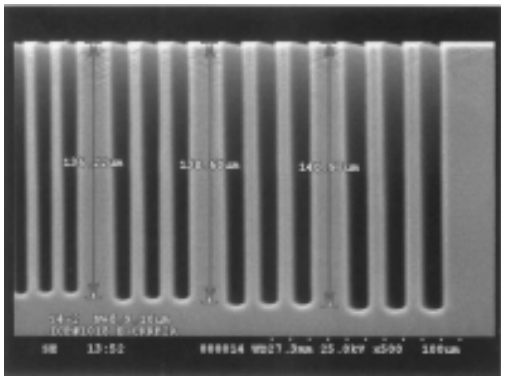
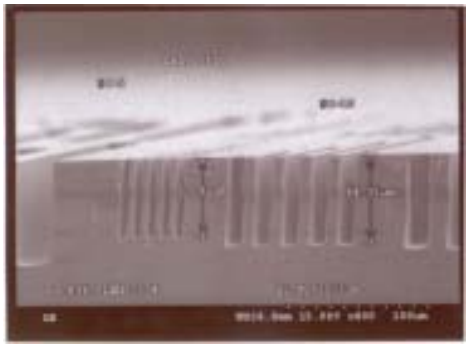
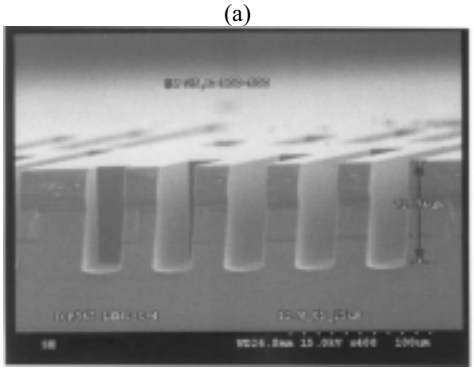


Figure 2 SEM micrograph of trenches with feature width of 8, 9 and 10 μm at constant length. The smaller feature size, the slower etching rate.

Besides the feature width, the continuous feature area or pattern shape also affects the etching rate. As the shape of feature with constant width is changed from rectangles to donuts, the etching depth increases with the continuous feature area as shown in Figure 4. Etching rates of rectangular trenches are sensitive to width while the donut trenches are sensitive to both width and area. The larger continuous feature area, the deeper etching depth. It implies that the feature area of pattern geometry is a secondly factor affecting the RIE lag.



(a)



(b)

Figure 3 SEM micrographs of trenches with feature width of 100-500 μm at constant width of: (a) 5, 10 μm, and (b) 25 μm. Etching depths of trenches are sensitive to width, not length or area.

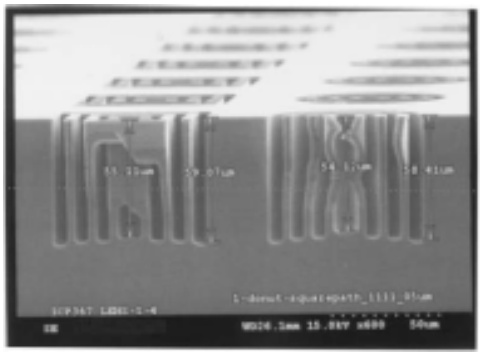


Figure 4 SEM micrographs of rectangular and circular donut trenches with constant width or radius of 5 μm.

The ICP etching behavior is relevant to the pattern geometry and process condition. To study the process parameter effect on RIE lag in ICP etching, we fixed the secondary factor of feature area to decrease the extra geometry contribution to RIE lag. The process pressure is a crucial factor on the RIE lag control. Figures 5(a)-5(c) show SEM micrographs of etched donut trench with constant area of π x 105^2 μm^2 at pressures of APC (a) 50%, (b) 70%, and (c) 75%, respectively. The etching time is for 15 min. Obvious RIE lag is present at APC 50% and elimated at 70% while inverse RIE lag trenches are obtained at APC 75%. The inverse RIE lag means the higher etching rate occurs at smaller feature width. It implies that other mechanism exists in Si DRIE with respect to the previous reports [4-7]. A possible new reaction mechanism is C_xF_y radical dissociated from C_4F_8 passivation gas playing an important role to affect the etching rate ratio of different feature sizes. The total etching rate is related to the formation of C_4F_8 passivation film on the Si trench bottom by C_xF_y radicals and its removal by S_xF_y ions from SF_6 etching gas, in addition to the arrival of F radicals dissociated from SF_6 etching gas to etch Si surface at the bottom. The formation and removal of C_4F_8 passivation film impedes the increasing of etching depth while the arrival of SF_6 etching gas enhances the etching processing. These two contrary reaction mechanisms compete by density and mass transport of radicals and ions dissociated from C_4F_8 and SF_6 reaction gases and affect the total etching rate. The increasing pressure will proportionally increase the C_xF_y and F radical density and decrease the S_xF_y ion density [12]. The aspect ratio will affect the formation and removal of C_4F_8 passivation film and Si etching at different feature width due to the mass transport. The smaller width with larger aspect ratio will lead to thinner passivation film than larger width. The removal of passivation film by ions under bias will be similar for different features. So Si etching dominated by F radical density will start earlier in the small width than large one. As the pressure increases, the increasing C_xF_y radical density and reducing S_xF_y ion density will delay longer to start etching Si surface at bottom in large feature than small one. The etching rate is enhanced more at small width than large one. This will lead to the reduction and elimination of RIE lag. If the pressure is much high, the inverse RIE lag occurs. It indicates that the effect of C_4F_8 passivation gas on RIE lag is more important than SF_6 etching gas.

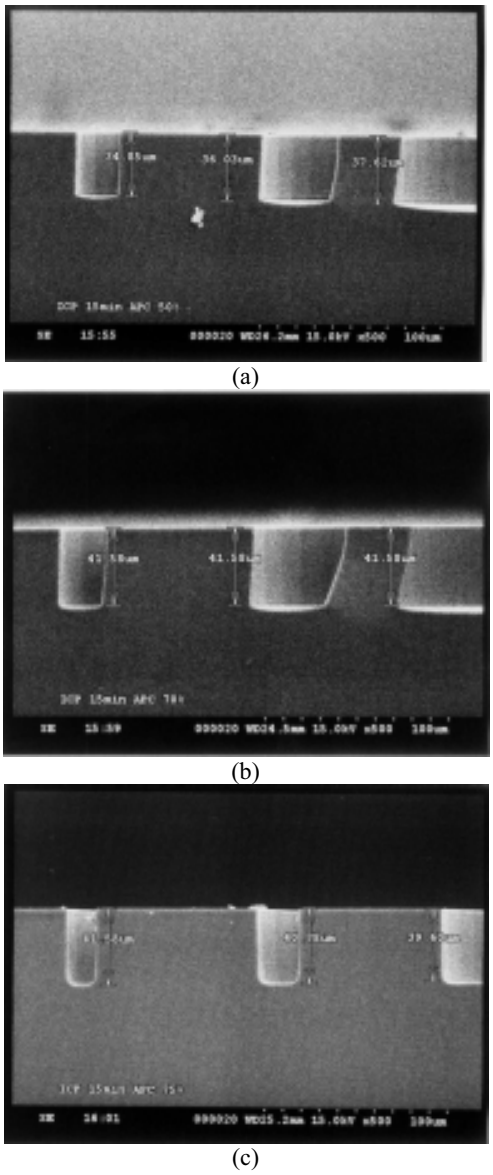


Figure 5 SEM micrographs of etched rectangular trench structure with constant area at pressures of APC: (a) 50%, (b) 70%, and (c) 75%, respectively. Obvious RIE lag is present at APC 50% and elimated at 70%, as inverse RIE lag trenches are obtained at APC 75%.

4 SUMARRY

A RIE lag phenomenon occurs in many patterns and becomes more severe at the smaller feature width and higher etching depth. In general, the smaller feature size, the lower etching rate and the more obvious RIE lag. A RIE lag elimination can be achieved for different feature size at constant area by higher process pressure of APC 70 % and the inverse RIE lag appears at much higher pressure of APC 75 %. This will lead to three stages of RIE lag transition: reduced RIE lag, lag elimination and inverse RIE lag. As the pressure increases, the increasing C_xF_y radical density and reducing S_xF_y ion density will delay longer to start etching Si surface at bottom in large feature than small one. So, the etching rate is enhanced more at small width than large one to result in the reduction, elimination and inverse of RIE lag. It indicates that the effect of reaction gas of C_4F_8 passivation on RIE lag in Si deep etching is

more important than SF_6 etching gas. It is an interesting phenomenon. The etching rate could be adjusted by the pattern geometry and process parameter. Different structures with RIE lag, RIE lag-elimination or inverse RIE lag would be fabricated by proper pattern and process design in future.

ACKNOWLEDGEMENTS

I would like to express my sincere thanks to Miss H.C Lu and Mr. K.S. Yen for their technical support. I also pay my sincere thanks to Common Laboratory of the Microsystems Technology Center of Electronic Research Service Organization in Industrial Technology Research Institute and the Southern Regional MEMS Center in National Cheng Kung University for the process equipment support.

REFERENCES

[1] R. Kassing and I.W. Rangelow, "Etching process for High Aspect ratio Micro Systems Technology (HARMST)", *Microsystems Technology* **3** pp. 20-27, 1996.

[2] W.H. Juan and S.W. Pang, "High-aspect-ratio Si etching for microsensor fabrication". *J. Vac. Sci. Technol. A* **13,** pp. 834-838, 1995.

[3] C. Zhang and K. Najafi, "Fabrication of thick silicon dioxide layers using DRIE, oxidation and trench refill", *MEMS2002*, pp. 160-163, 2002.

[4] H. Jansen, M. de Boer, R. Wiegerink, N. Tas, E. Smulders, C. Neagu and M. Elwenspoek, "RIE lag in high aspect ratio trench etching of silicon", *Microelectronic Engineering*, **35**, pp. 45-50, 1997.

[5] A.A. Ayon, R. Braff, C.C. Lin, H.H. Sawin and M.A. Schmidt, "Characterization of a time multiplexed inductively coupled plasma etcher", *J. Electrochem. Soc.*,**146**(1), pp.339-349, 1999.

[6] J. Kiihamaki and S. Franssila, "Pattern shape effects and artifacts in deep silicon etching", *J. Vac. Sci. Technol.*, **A 17**(4), pp.2280-2285, 1999.

[7] J. Jiao, M. Chabloz, T. Matsuura and K. Tsutsumi, "Mask layout related area effect on HARSE process in MEMS application", *Transducers'99*, pp.546-549, 1999.

[8] R. Zhou, H. Zhang, Y. Hao, D. Zhang and Y. Wang, "Simulation of profile evolution in etching-polymerization alternation in DRIE of silicon with SF_6/C_4F_8", *MEMS2003*, pp.161-164, 2003.

[9] T-K A. Chou and K. Najafi, "Fabrication of out-of-plane curved surface in Si by utilizing RIE lag", *MEMS2002*, pp.145-148, 2002.

[10] J.K. Bhardwaj and H. Ashraf, "Advanced silicon etching using high density plasma", Proc. *SPIE Micromachining and Microfabrication Process Technology*, **2639, pp.** 224- 233, 1995.

[11] A.M. Hynes, H. Ashraf, J.K. Bhardwaj, J. Hopkins, I. Johnston, and J.N. Shepherd, "Recent advances in silicon etching for MEMS using the ASE^{TM} process", *Sensor and Actuators* **74,** pp.13-17, 1999.

[12] M.A. Blauw, T. Zijlstra, and E. van der Drifta, "Balancing the etching and passivation in time-multiplexed deep dry etching of silicon", *J. Vac. Sci. Technol. B* **19(6)**, pp. 2930-2934, 2001.