Process Factors in the Reduction of Output Conductance in Sub-micron CMOS

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ABSTRACT

CMOS Analog circuits require transistors with low output conductance (g_{ds}) in order to achieve high gain. Submicron MOSFETs with halo implants and retrograde wells are designed to have high transconductance (g_m) but often suffer from poor output conductance. In this paper we investigated the process factors affecting g_{ds} and we show how to optimize g_{ds}. Our experimental results from 180nm CMOS are compared with 2D simulations in order to understand the mechanisms involved. Output conductance is the derivative of the I_D-V_D curve, $g_{ds} = dI_D/dV_D$. In saturation, several effects contribute to the increase of I_D with V_D, namely channel length modulation (CLM), drain-induced barrier lowering (DIBL), and substrate current body effect (SCBE). We have mainly focused on PMOS transistors at voltages where the substrate current is not significant.

Keywords: channel length modulation, drain-induced barrier lowering, early voltage, output conductance, output resistance

1 INTRODUCTION

Successful integration of mixed signal circuits incorporating high performance and analog circuits are vital for system on chip applications (SoC). However, CMOS device design scale-down is particularly challenging as the requirement for analog and digital devices are often conflicting and thus usually result in trade-offs. High performance logic devices are optimized for good drive current, low leakage and SCE control which incorporate super halo and double-pocket structures. These structures however, often result in low output resistance, device gain, transconductance-to-drive current ratio and matching properties [1].

Low output resistance is the result of increase I_D with V_D in saturation regime. Three components are associated with this increase, namely channel length modulation (CLM), drain-induced-barrier-lowering (DIBL) and substrate current body effect (SCBE). Novel structures such as single pocket implant [1,2,3] and shadow-mask implant [4] were proposed to increase analog performance while maintaining good high performance characteristics. Both structures refer to asymmetric channel doping profile that has good SCE control for high drive current. It also has good control of CLM and DIBL for low output conductance. However, asymmetric device also means higher cost of production and increase in device complexity. Therefore, the paper is aimed to study the existing process factors that can be tuned in for the reduction of g_{ds}. We have mainly focused on PMOS transistors at voltages where the substrate current is not significant.

2 EXPERIMENTAL/SIMULATION

PMOS and NMOS transistors were fabricated with gate length of 180nm. We systematically varied the process factors LDD implant, halo implant, well anneal, spacer and anti punch-though (APT) implant to study their effects on output conductance. Experiments in silicon were run as well as 2D simulations. Process simulator, TSUPREM4 and MEDICI were used for simulations. Each factor was evaluated by comparing the Early Voltage (V_A) as a figure of merit rather than g_{ds} directly because g_{ds} varies as a function of gate voltage and drain current. Early Voltage is defined as $V_A = I_D/g_{ds} - V_D$. It is always desired to get high V_A, which corresponds to low output conductance. At the same time, it is also desirable to maintain high drain current.

3 RESULTS AND DISCUSSION

Table 1 shows the parameters and the variables that were varied to study the various process factors. The experimental and simulation results shown are mainly from PMOS with gate length of 180nm. Even though NMOS results are not shown, their results are consistent with PMOS.

Parameter	Variation
LDD implant	dose
Halo implant	dose and tilt
Nwell implant	dose
Spacer	thickness
Well Anneal	anneal temperature
APT implant	dose and energy

Table 1: Parameters and their variations used in this study.

3.1 LDD Implant

Figure 1 shows the sensitivity of V_A to LDD dose for a PMOS transistor with gate length of 180nm. Increasing the LDD dose decreases V_A because the effective channel

becomes shorter, which is shown in Figure 2. Shorter channel length results in larger residual DIBL thus causing output resistance to decrease [5]. The doping profiles of the different LDD dose in the channel are illustrated in Figure 3.

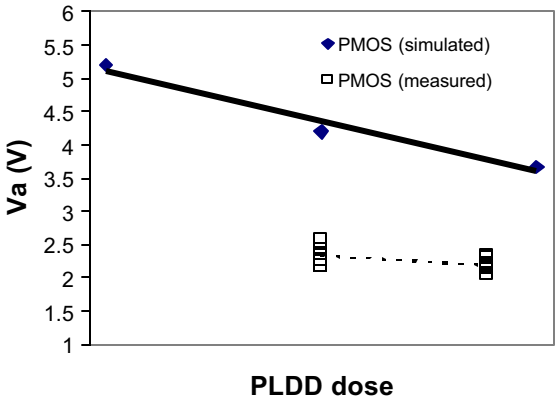

Figure 1: V_A dependence on PLDD dose. Note as dose increases, V_A decreases.

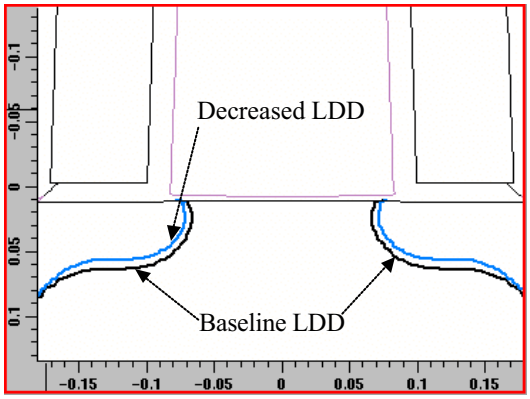

Figure 2: Junction profile for different LDD dose (MEDICI). Higher LDD dose shortens the channel length

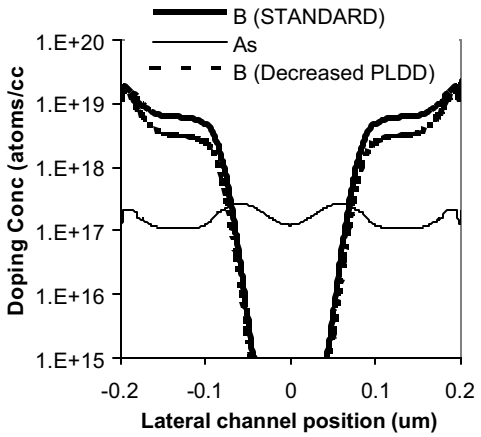

Figure 3: PLDD and channel doping profiles (TSUPREM4)

3.2 Halo Implant

Figure 4 shows that increasing the halo dose increases V_A. Increasing the halo tilt angle also increases V_A as shown in the inset. The larger tilt angle placed the halo implant almost at the center of the channel as in Figure 5. The additional arsenic in the channel lessens the effect of DIBL as shown in Figure 6. However, increasing halo dose also causes Idsat to decrease. As can be seen in Figure 7, increasing halo dose has opposite effect on V_A and Idsat. Experimental studies have also shown that pocket implant has tradeoff effects on V_A and Idsat [5].

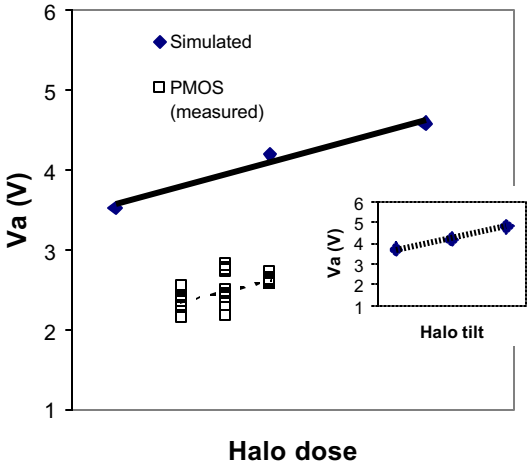

Figure 4: V_A dependence on halo dose. Higher halo dose produces higher V_A

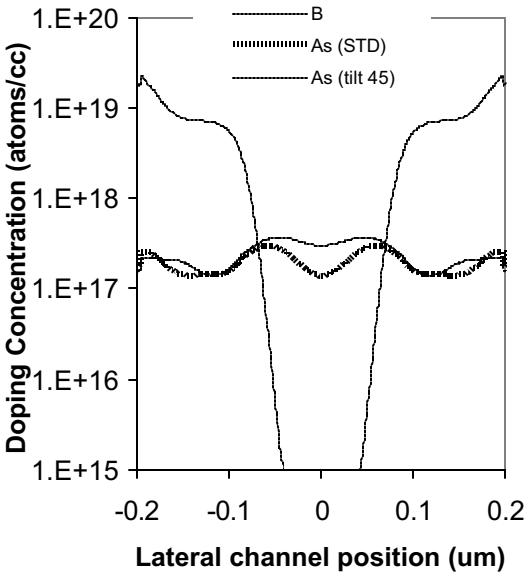

Figure 5: Halo doping profiles in the channel (TSUPREM4). Higher halo dose in the channel at higher tilt

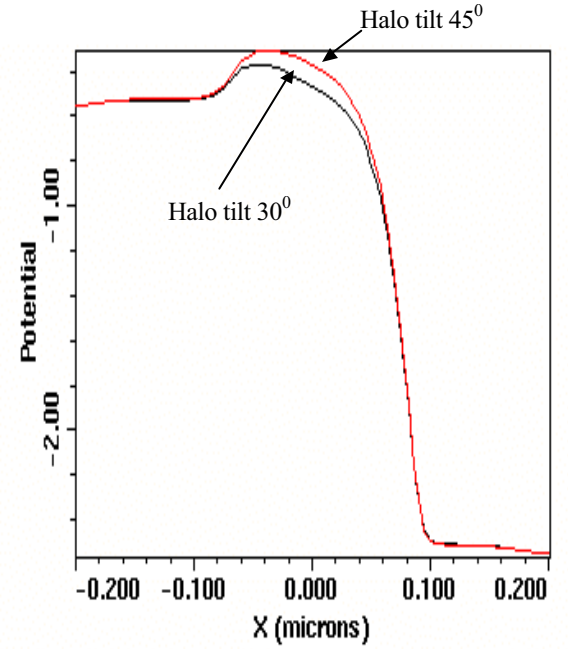

Figure 6: Potential barrier shifts at different halo tilt angle (MEDICI). Higher tilt has higher potential barrier, thus decreases DIBL.

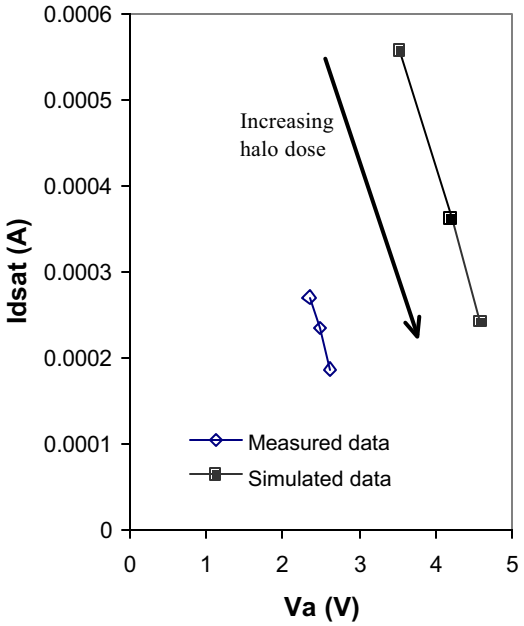

Figure 7: Idsat vs. Va plot. Effect of increasing halo dose on Idsat and Va. Va increases but Idsat decreases as halo dose is increased.

3.3 Nwell Implant

Figure 8 shows that increasing well dose has no effect on V_A. As shown in the inset, the well is far deeper than the channel, and the surface doping is dominated by channel implants.

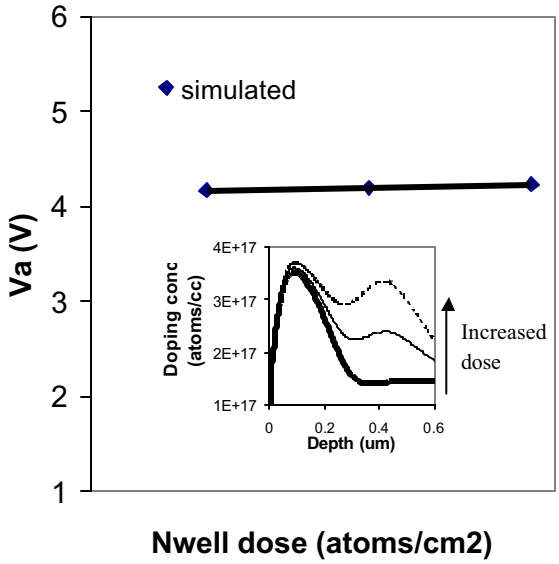

Figure 8: V_A dependence on Nwell dose. No effect of Nwell dose on V_A.

3.4 Spacer Thickness

Figure 9 shows that spacer width also has very little effect on V_A. Increasing the spacer width makes the LDD longer towards the source-drain (Fig. 8 inset), thus increasing the resistance, but does not affect DIBL or CLM.

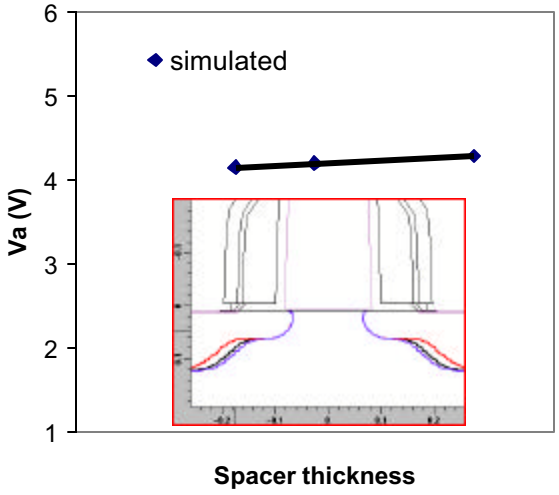

Figure 9: V_A dependence on spacer thickness. Note insignificant effect of spacer thickness on V_A

3.5 Well Anneal

Figure 10 shows the effect of well anneal temperature against V_A. An optimum well anneal temperature is observed for each device. It was found that output resistance is very sensitive to well anneal temperature due

to degradation of retrograde implant shape at very high and very low anneal temperature [6]. At very high temperature, large thermal diffusion and pile-up at SiO/Si interface causes the degradation. On the other hand, transient enhanced diffusion (TED) occurs at gate oxidation process at low temperature [6].

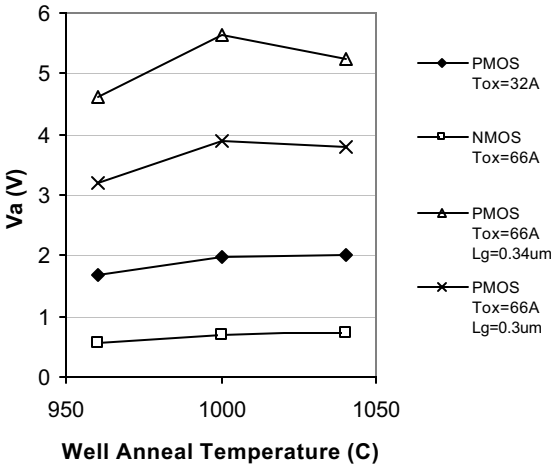

Figure 10: Measured V_A dependence on well anneal temperature. Optimum temperatures are observed.

3.6 Anti Punch-through Implant

Figure 12 shows the plot of Idsat versus V_A at different anti punch-through (APT) implant conditions. As APT energy implant is increased, V_A shows a contradict trend depending on the implant dose used. At high dose and high energy, the plot is shifted to the up-left when energy is increased. However, the plot shifted to the up-right as energy is increased at low APT implant dose and energy. At low dose and energy, increasing the APT implant energy forms super steep retrograde (SSR) channel, which has positive effects for analog applications [1,6].

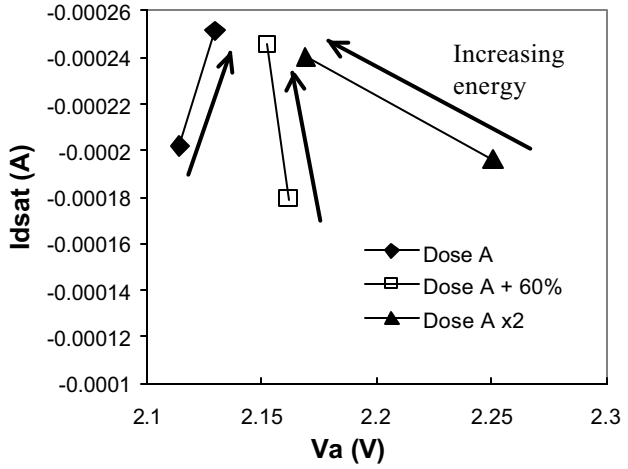

Figure 12 : Effects of APT implant on V_A and Idsat.

4 CONCLUSIONS

In this work we have shown what process factors affect g_{ds} and we have optimized these factors to achieve low g_{ds}. We found that g_{ds} is most sensitive to LDD dose, halo dose, halo tilt and APT dose and energy. Our experimental results confirmed the trends of the 2D simulations.

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