# Planarize the sidewall ripples of silicon deep reactive ion etching

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## ABSTRACT

In order to diminish the sidewall defects in silicon deep reactive ion etching process, depositing doped silicon dioxide and post-annealing processes are applied. Compared with conventional approaches, the filling-reflow surface shows nearly optical quality. This novel scheme is not restricted to design layout without silicon crystal orientation dependence in the wet chemical etching methods. The unique integrated processes are expected to implement in the micro devices or replica master with optical surfaces.

***Keywords***: silicon deep RIE, sidewall roughness

## 1 INTRODCUTION

High aspect ratio technology is used to realize structures with feature sizes up to hundreds of microns in MEMS fabrication. Bosch silicon deep reactive ion etching (DRIE) based technologies are generally satisfying the demands of the MEMS fabrication. This process is based on the technique invented by Laermer and Schilp[1] and uses a variant of the sidewall passivating technique, which is deliberately segregated by using sequentially alternating etching and deposition steps. First a sidewall passivating polymer is deposited and subsequently the polymer and silicon are etched from the base of the trench, to allow the etching to proceed directionally. In this cyclic way the etching and deposition can be balanced to provide accurate control of the anisotropy. However, the process leaves sidewalls with ripples, or scallops, because of the nature of the process sequence that is cycled between etch and passivation phases. The defect limits the process virtues in optical device such as micro cavity lasers, and some micro fluidic component applications.

Reactive ion etching (RIE) is the combination of mechanical ion bombardment (as in sputter etching) and the chemical process of plasma etching. DRIE is also based on reactive ion etching, but an important consideration in the decision of using reactive ion etching vs. deep reactive ion etching is the aspect ratio of the trench. The aspect ratio is defined as the maximum depth versus the maximum width. When aspect ratios are too high (>3:1), etching with RIE may lead to lag, bowing, bottling, micrograss, and tilting. These issues are a major concern because trenches will not result in perfectly straight walls. Many microfluidic and micromechanical devices require very deep trenches or very tall beams, with straight sidewalls. In order to achieve high aspect ratios (up to 30:1) using reactive ion etching, the sidewalls must be prevented somehow from being etched.

In the time-multiplexing scheme of DRIE, the etching and passivating gas monomers are flowed independently one at a time, and the machine alternates between an etching cycle and a passivating cycle. The etch step forms a shallow trench in the silicon substrate, with an isotropic profile characteristic of fluorine-rich glow discharges. This process, succinctly described as time-multiplexed deep etching, TMDE, offers the advantage of exploiting the high silicon etching rate. Surface roughness issues are particularly important in TMDE tools. Because of the alternating etching and passivating cycles and the spontaneous nature of the etch in fluorinated chemistries, structures fabricated by means of TMDE exhibit a characteristic scalloped sidewall roughness that can be unacceptable in some applications, see in the figure 1.

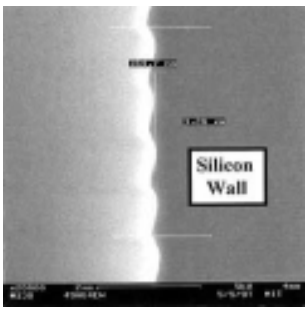



Figure 1, the sidewall ripples of DRIE structure

Lin etc. [2] proposed the technique in fabricating a solid polymer dye microcavity laser, which is molded with the etched Si cavity. By a combination of deep-RIE and EPW (the ethylenediamine pyrocatechol and water etchant) wet etching of silicon, optically smooth surfaces have been obtained. Alternately, Nillson etc. [3] removed the surface roughness of the sidewalls with adding a short etch in KOH+IPA after the deep etching processes in optimized parameters. Early, Volland etc. [4] reported on the development of a novel gas chopping etching technique (GCET)process in order to achieve a smooth (rippled free) sidewall surface. However, the modified GCET has lower

selectivity (in range of 30) than the conventional approaches.

The sidewall ripples are decreased in the above techniques, but some compromises are made. The microstructure features created by wet etching methods, for example, depend on silicon crystal orientation. The ripple-free sidewall can be obtained by anisotropic etching instead of isotropic mode during etching- passivating switch cycle, but the modification must loss the benefit of selectivity in Volland's process. We have established a novel scheme to diminish the sidewall ripples and kept the virtues of the DRIE process.

## 2 EXPERIMENTAL

Figure 2 shows the conventional process sequence for the fabrication of silicon deep reactive ion etching. The substrate of the mold is a Si (100) wafer with a thickness of about 500μm. Before photolithography, a layer of low pressure chemical vapor deposition, LPCVD, silicon oxide as an etch mask for etching is put on the wafer. The design layout is patterned by photolithography and the resist and oxide masks are stripped in sequential processes.

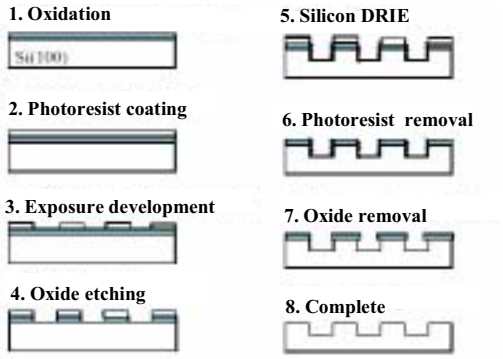



Figure 2, DRIE fabrication processes

Borophosphosilicate glass, BPSG, films have been used as fusible deposited dielectrics in silicon-gate MOS integrated circuits, with fusion tapering achieved at temperatures 100 °C to 200 °C lower than is normally possible with phosphosilicate glass, PSG, films. Both glass films can be deposited by LPCVD or plasma enhanced chemical vapor deposition, PECVD processes. The former produce conformable film profile over the microstructures, and overhang rise by the latter way, see in the figure 3 (a) and (b).

BPSG film of 3μm thickness is deposited by PECVD process. Soften the layer 90 minutes with the high temperature of 800°C. To improve the step coverage on the etching structure, deposit PSG of to fill in the scallop structure. Annealing PSG film is processed at 1000 °C for two hours; see in the figure 3(c). Compare the sidewall roughness of different schemes by cross-section views of scanning electron microscope, SEM, and by ripple profiles of atomic force microscopy, AFM.

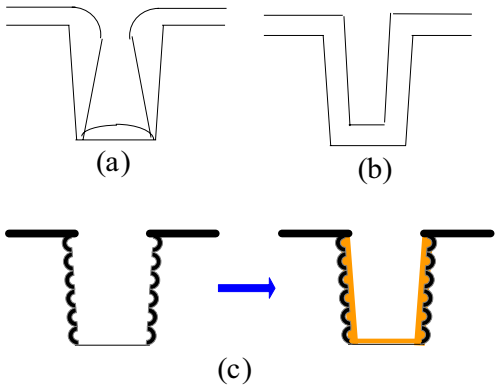



Figure 3, Step coverage of film deposited by PECVD (a) and LPCVD (b) processes; doped silicate glass depositing and annealing after DRIE etching(c).

## 3 RESULTS

### 3.1 BPSG film with PECVD process

The microstructures of 5μm wide and 15μm depth are etched and remove the passivated polymer layer of the etching process by oxygen plasma. The sidewall surfaces are shown in the figure 4(a) and ripples of 0.5μm size is obvious in the SEM images. The structures covered by BPSG show the smooth profile and the overhang produced by PECVD process exits on the top corner in figure 4(b).

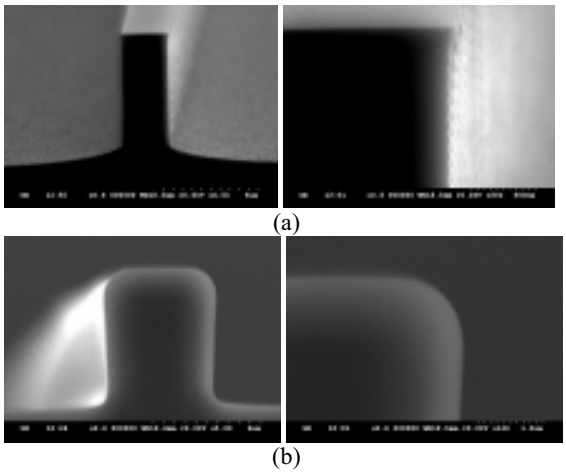
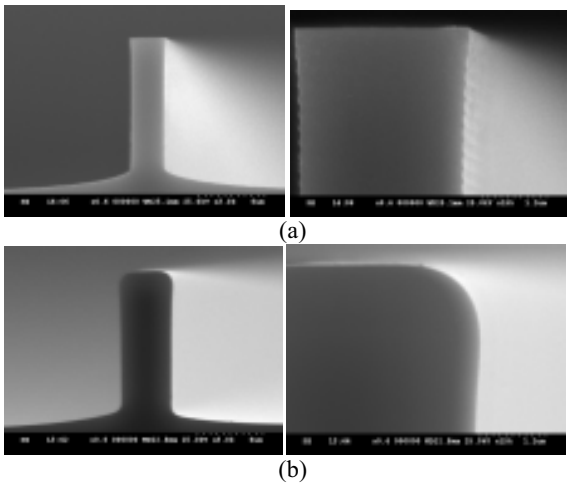



Figure 4, the sidewall ripples of DRIE structure: prior to BPSG film deposition (a); afterwards film deposition and annealing (b).

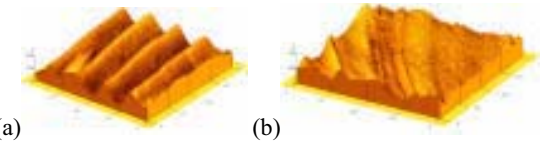
### 3.2 PSG film with LPCVD process

The same etched structures are deposited with 2μm PSG film. The good step coverage profile is observed by SEM and the sidewall performance shows in the Figure 5(b). No overhangs appear on the corner of the etched structures. The surface roughness monitored by AFM indicates 77 and 22 nm in the etched structure and 37 and 8 nm for the PSG-deposited structures; respectively peak-to-valley difference and root mean square, which is satisfied for the optical device application, see in the figure 6.



(a) (b)

Figure 5, the sidewall ripples of DRIE structure: prior to PSG film deposition (a); afterwards film deposition and annealing (b).



(a) (b)

Figure 6, Surface roughness measurements by AFM; Prior to PSG film deposition (a):77nm (peak-valley), 22 nm (mean square). Afterwards film deposition and annealing (b): 37nm (peak-valley); 8nm (mean square)

## 4 DISCUSSIONS

The proposed strategy of doped silicon dioxide deposited and annealing films processes after etching procedures can refill the sidewall defects, competed with conventional approaches including replacing of the isotropic etching step by an anisotropic etching step, shortening etching and passivating cycle time in recipes and using a combination of DRIE and anisotropic wet etching with KOH. Our approach avoids the limit of optimizing the etching parameters in Nillson [3], who reduced the etching-passivating switch time. To improve the roughness by reducing the switch time, the time is too short to be completely evacuated the atmosphere of the etching or passivating respectively, before entering the next state, see in the Table 1. The post-DRIE wet etching strategies suffer the etching selectivity of silicon crystal orientation and restrict the freedom of the layout designer. Our scheme keeps all benefits of the Bosch's DRIE technique and improves the sidewall to the optical surface quality. Furthermore, the processes can also be used to smooth the vertical mirror roughness [5] or replica the nickel embossing mold by tuning the de-mold angle.

| | Recipe I | Recipe II |
|---|---|---|
| Etch time | 7.5 sec | 3.75 sec |
| Passivation time | 5 sec | 2.5 sec |
| Cycles | 20 | 30 |
| Process time | 3 min 9 sec | 3 min 9 sec |
| Resulting etch depth | 20 μm | 20 μm |
| Resulting scallops vertical size | 1 μm | 700 nm |
| Resulting scallops lateral size | 300 nm | 130 nm |

Table 1, selection of optimized parameters for silicon deep RIE and the resulting features. [3]

## 5 CONCLUSIONS

The reflow process of doped silicate glass produces liquid free surfaces to get the optical quality and is not limited to the crystal orientation in design layout. We successfully diminish the sidewall ripples of silicon etched structures. The unique integrated processes are expected to implement in the micro devices or replica master with optical surfaces.

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