Fabrication of 20 nm embedded longitudinal nanochannels transferred from metal nanowire patterns

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ABSTRACT

In this paper, we propose a technique of fabricating nanometer-scale channels embedded by dielectric materials. Longitudinal "embedded" nanochannels with an opening size 20 nm x 80 nm have been successfully fabricated on silicon wafer by sacrificial etching nanowire structures.

Keywords: nanochannels, focused ion beam, sacrificial etching.

INTRODUCTION

The traditional electron beam lithography and more recently developed focused ion beam (FIB) milling/lithography techniques have been exploited for generating *exposed* nanometer-size nanochannels for the manipulation and analysis of biomolecules such as DNA and proteins at single molecule resolution [1]. An additional process step of sealing exposed nanochannels can't be avoided to generate complete nanodevices. Currently, sealing techniques such as wafer bonding and soft elastomer sealing are being used for sealing micrometer-scale exposed channels. However, current wafer bonding requires defect free and flat surface, and elastomer sealing process comes with clogging because of soft material intrusion into the channels [2]. Our proposed technique provides a wafer bonding-free process to fabricate embedded nanochannels. We demonstrate that the combined use of high-resolution focused ion beam lithography, a subsequent reactive ion etching and sacrificial etching may be a good candidate as a novel fabrication technique for embedded nanochannels for bio-applications.

EXPERIMENTAL RESULTS

We utilized a sacrificial etching method to prepare nanochannels embedded by dielectric materials. When we create nanometer-scale nanofluidic structures for molecular level detection, reducing size and creation of sealed fluidic channels will be needed. Current sealing techniques such as wafer bonding and soft elastomer sealing are suitable for relatively big planar surfaces and provide an effective sealing. However, defect-free and flat surface is necessary for sealing exposed nanochannels. We report two new methods to fabricate embedded nanochannels and characterizing nanochannels by sacrificial etching and FIB, milling, respectively. The essence of the fabrication technique of embedded nanochannels is the selective etching of the patterned sacrificial layer to create the inner space of nanofluidic channels, leaving the embedded materials. 2 mm long nanochannels having height of 20 – 100 nm by sacrificial etching of amorphous silicon in a TMAH solution was reported [4]. We were successful in fabricating smaller nanochannels by a similar sacrificial etching technique. Characterization method by FIB was performed to check if nanochannels are all the way through. In order to do it, micrometer-scale trenches were created both ends of nanochannels after a sacrificial etching. Longitudinal nanometer-scale embedded channels have been fabricated by a sacrificial nanowire etching technique. In our fabrication, an array of nanometer-scale metal nanowire patterns was first fabricated on SiO_2/silicon wafer using Focused Ion Beam (FIB) lithography and a subsequent metalization/lift-off process. The metal nanowire patterns were transferred onto SiO_2 layer by reactive ion etching (RIE). Figure 1 shows the SiO_2 nanowire prepared by FIB lithography and a subsequent RIE process. Nanometer-scale SiO_2 nanowires as sacrificial patterns were obtained after removing metal mask patterns (Fig. 2-a). Plasma Enhanced Chemical Vapor Deposition (PECVD)dielectrics were deposited on the SiO_2 nanowire patterns (Fig 2-b). FIB milling was used to generate trenches both front region and rear region of the nanowires (Fig. 2-c). Figure 3 shows a cross-sectional view of the 20 nm x 80 nm size SiO_2 nanowire patterns embedded by PECVD dielectrics. Those trenches provided openings through which etchant chemicals (BOE) were going. As a result of a different etch rate of SiO_2 and dielectrics in BOE, "embedded" nanochannel patterns were fabricated on silicon substrates (Fig. 2-d). In order to reveal that channels were gone through two openings, FIB milling was used for a fast and precise analysis. Figure 4-a shows the big trenches prepared by FIB milling for generating openings for easy sacrificial etching and the small trenches for etching analysis. FIB characterization technique was introduced to check if the etching area was cleared. Broad beam ion milling, where ions (usually Ga^+) of a high energy are incident on a surface, is a widely used method of material removal [8]. One or two atoms of the substrate are removed per incident ion. Whereas for FIB, where the energy is about two orders of magnitude higher, the situation is expected to be similar. The yield increases slowly as a function of energy then flattens out and turns downward at about 50 keV [9]. When a gallium (Ga) ion

beam is scanned in a line on a surface, a trench is produced which initially has the shape of an inverse Gaussian as expected from the beam profile. However, when the dose is increased, the trench becomes sharp, narrow, V shaped, and deep. The need for fast precision cross sectioning and inspection of submicron structures in multi-layered integrated circuit devices continues to grow and to be a major force in the development of focused ion beam milling technique. FIB milling techniques offer the high level of precision and flexibility required for inspection of submicron devices. In our work, FIB milling was used as a convenient tool to check if the inner space of nanochannels're etched all the way through during sacrificial etching. High-resolution FIB techniques routinely locate and section the area of interest as small as a few microns. A rectangular area containing area of interest is milled. The sample is then tilted and observed *in situ* using ion induced microscopy or is transferred to a field emission scanning electron microscope (FESEM) for high-resolution imaging. By checking both ends of nanochannels, we were able to confirm that our nanochannels are etched all the way through. The 20 nm x 80 nm x 3 um long enclosed channel is shown in Figure 4-b. Five various lengths (3, 6, 8, 10, 20 μm) of pillar patterns were tried to find a maximum length of enclosed channels which were able to be generated without experiencing "diffusion–blocking" during a sacrificial pillar etching process. 3 μm long longitudinal nanochannels were successfully fabricated.

CONCLUSIONS

In conclusion, we have fabricated nanometer-scale embedded nanochannels. This technique is based on a conventional sacrificial layer etching. To confirm our nanochannels are all the way through, high-resolution FIB milling was used. The major technological advantage of the present technique in preparing nanometer-scale embedded nanochannels is that it allows for the use of sacrificial etching for fabrication and FIB milling for characterization, respectively.

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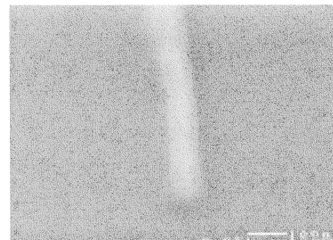

Figure 1: Scanning electron micrograph showing a nanometer-scale SiO_2 nanowire prepared by FIB lithography and a subsequent RIE process. The metal mask still remained on the top of the nanowire.

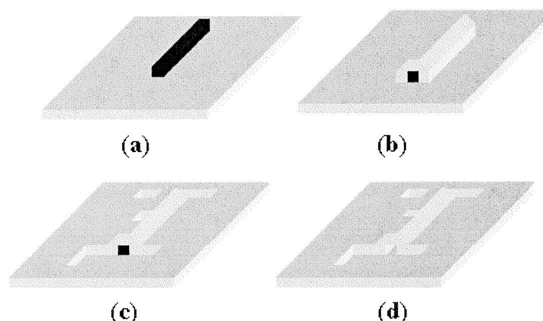

Figure 2: Fabrication process of enclosed nano-channels. (a) fabricating SiO_2 nanowires by FIB lithography and a subsequent RIE. (b)depositing PECVD dielectrics (c)generating trenches by FIB to be used for openings for flowing etchant in (d) etching sacrificial SiO_2 nanowire by BOE.

PECVD dielectrics

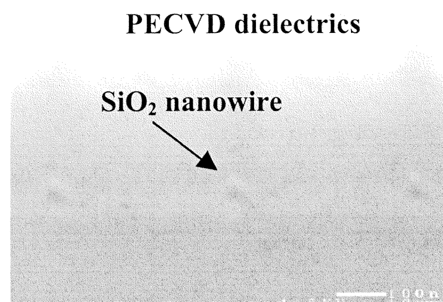

Figure 3: Scanning electron micrograph showing a cross-sectional view of sacrificial SiO_2 nanowires embedded by PECVD dielectric layers.

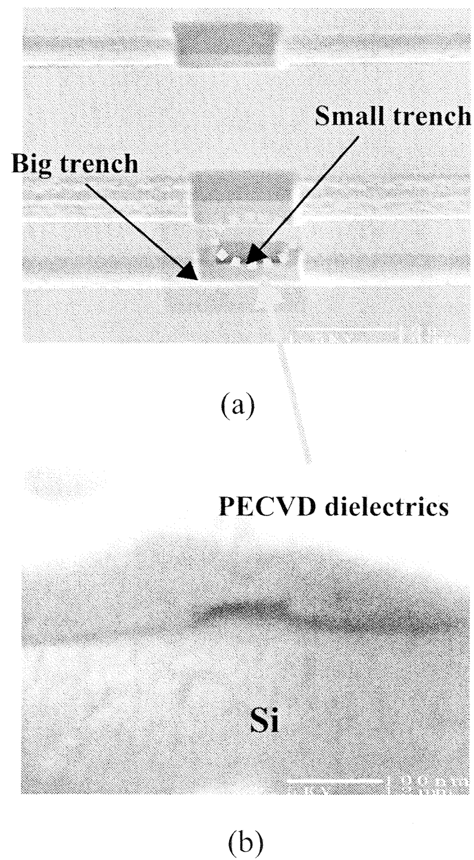

Figure 4: (a) Scanning electron micrograph showing a big trench prepared by FIB for generating openings for easy sacrificial etching and a small trench for a fast and a precise etch analysis. (b) scanning electron micrograph indicating a cross-sectional view of 20nm x 80 nm enclosed nanochannels.