# Multi Tunnel Junction Memory : Analyses of Feasibility for Non-Volatile Memory Applications

C. Le Royer*, G. Le Carval* and M. Sanquer**

* CEA-DRT - LETI/DTS - CEA/GRE, 17 avenue des Martyrs, 38054 Grenoble Cedex 9, France, cyrille.leroyer@cea.fr
** CEA-DSM - DRFMC - SPSMS, 17 avenue des Martyrs, 38054 Grenoble Cedex 9, France

## ABSTRACT

In this work, we simulate the electrical behavior of the Quantum-Dot-based Multi Tunnel Junction Memory (MTJM) [1] thanks to a new compact model dedicated to this device. Electron transport through ultra-small quantum dots is investigated using a master-equation model taking into account the discreteness of quantum levels.

We analyze the effects of the technological parameters (dots density and size, geometries) on the writing and retention characteristics of the MTJM cell. We also study at room temperature the conditions under which this Memory concept could be an alternative for Non-Volatile Memories (for the 50 nm node).

*Keywords*: Non-Volatile Memory, quantum dot memory, Coulomb blockade phenomena, Master Equation Model, simulation

## 1 INTRODUCTION

MOSFET memories based on quantum dots have been investigated extensively because of their promising applications to non-volatile and low voltage memories [2]. Among these memories, the Multi-Tunnel-Junction Memory (MTJM) [1,3] appears to be a promising concept for both DRAM [4] and Non-Volatile Memories (NVM). For this last application, we analyze by simulation the effects of the technological parameters (dots density and size, geometries) on the writing and retention characteristics of the MTJM cell.

## 2 DEVICE DESCRIPTION

### 2.1 Principle of the MTJ Memory

The memory cell is described in Figure 1. The principle is similar to Flash Memory : The information charge is stored on a Floating Gate (FG) of a MOSFET, but here the writing is ensured by a "single-electron" current between the Control Gate (CG) and FG via quantum dots.

The retention is ensured by the Coulomb Blockade (CB) phenomenon [5] above FG and a thick High-k gate insulator (which prevents the gate-to-channel leakage).

In this paper, we assume that, for the modeling, the dots are metallic : The tunneling of charges between CG, dots and FG shows nonlinear conduction characteristics which can be described thanks to the "orthodox theory" of Coulomb Blockade (CB) [2,5].

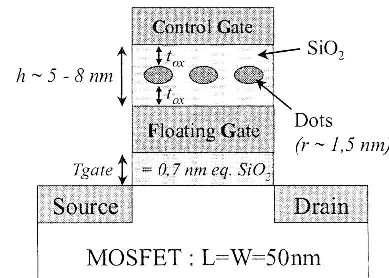



Figure 1: Multi Tunnel Junction Memory structure.

### 2.2 Technological parameters

The parameters needed to describe accurately the Memory are related to the shapes of the dots. Usually spherical dots are considered [3]. In fact, TEM (Fig 2.b) and SEM observations of dots show that they are ellipsoidal (at least for our $SiO_x$-based process).

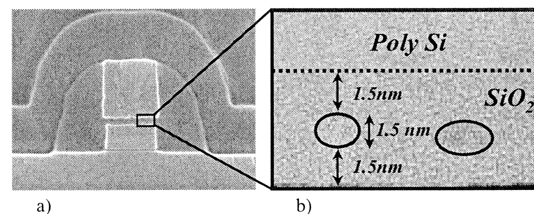



Figure 2 : SEM image of MTJ Memory (a), TEM image of Si dots (b).

So we consider that dots can be described by two parameters, $R_H$ (radius in the horizontal plane) and $R_V$ (radius in the vertical direction).

# 3 THE SIMULATION MODEL

## 3.1 Physical phenomena

The tunneling of charges between CG, dots and FG is described by "tunnel junctions" [2,5]. A tunnel junction is characterized by two elements : a capacitance $C_j$ and a conduction term, $R_t$, called "tunnel resistance". (We model the upper part of the MTJ Memory (above FG) with tunnel junctions.)

In the usual range of density of dots ($10^{11}$ - $10^{12}$ $cm^{-2}$), we checked [3] that for nano-dots (radius < 4-5 nm) the Memory cell characteristics show a negligible dependence on the repartition of dots (periodic or random). This result allows us to consider that the interactions between dots are negligible and therefore, that the central element of the Memory is the "double junction" (Figure 3, Figure 4).

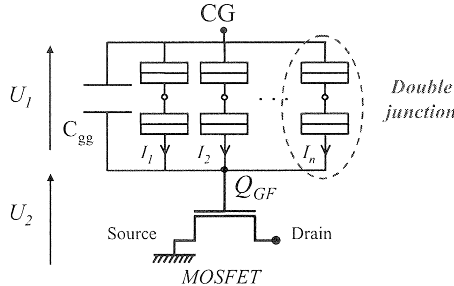
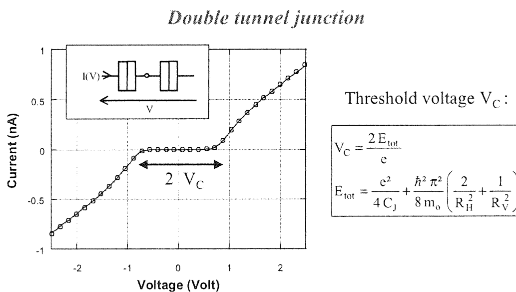



Figure 3 : Equivalent electrical circuit of a MTJ Memory cell.

We calculate the I-V(t) characteristics of the "double tunnel junction" with a master-equation model [3,5] taking into account :

- the geometries and the materials
- the states of charge of the dots (q=-e, 0 or +e)
- the transition rates across the tunnel junctions
- the tunnel resistances depending on biases
- the transient effects
- the quantum confinement in the dots (Figure 4)




$$V_C = \frac{2E_{tot}}{e}$$

$$E_{tot} = \frac{e^2}{4C_j} + \frac{\hbar^2\pi^2}{8m_o}\left(\frac{2}{R_H^2} + \frac{1}{R_V^2}\right)$$

Figure 4 : Current-voltage characteristics of the double tunnel junction (with the threshold voltage $V_C$).

The parameters that describe the Memory are the tunnel resistances $R_t$ and the junction capacitances $C_j$ (for the tunnel junctions), the capacitance $C_{gg}$ between the Control Gate (CG) and the Floating Gate (FG) and the capacitance $C_{MOS}$ between FG and the channel of the MOSFET (Figure 3).

## 3.2 Capacitances of the cell

For the calculation of the tunnel junction capacitances $C_j$, and the CG-FG capacitance $C_{gg}$, we use the 3D Capacitance Calculator ICARE [7]. The values of the studied parameters are chosen according to a Design of Experiment (DoE), to ensure a good predictivity on the whole domain.

## 3.3 Tunnel resistances

To study the tunneling through the "double tunnel junction", four expressions of tunnel resistance are calculated. For electron tunneling in the direction of positive (resp. negative) values of $V_i$ (voltage across the barrier i=1,2) we obtain [5] :

$$\vec{R}_{t,i}(V_i) = \frac{R_q}{\vec{T}(V_i, E_F)} \quad (1)$$

$$\overleftarrow{R}_{t,i}(V_i) = \frac{R_q}{\overleftarrow{T}(-V_i, E_F)} \quad (2)$$

$R_q = h/e^2$ is the quantum resistance [2,5] and $T(V_i, E_F)$ is the tunnel transparency of the barrier ($V_i$ is the bias across the barrier i=1,2 and $E_F$ is the energy of the Fermi level in the initial electrode).

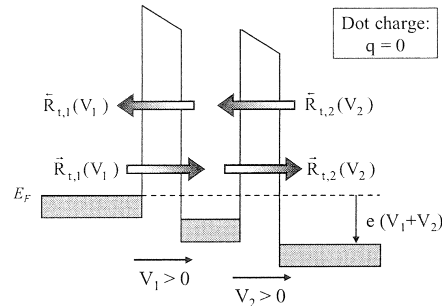



Figure 5 : Band structure of the Double junction : Barrier voltage dependence of $R_t$.

The tunnel transparency is calculated according to the WKB approximation with the Register correction [7]. Figure 6 shows that this correction is significant and therefore, must be taken into account.

As $R_t$ controls the current through the "double tunnel junction", the modeling of this current implies an accurate modeling of $R_t(V)$.

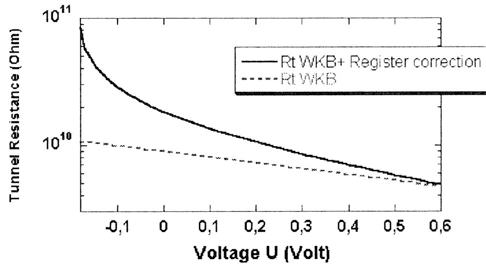



Figure 6 : Impact of the Register Correction on the tunnel resistance.

# 4 RESULTS

In the following, we monitor the number of stored charges on the Floating Gate, $N_{FG}$, during and after the writing cycle (at room temperature).

From the curves $N_{FG}(t)$, we extract a retention time defined as the time during which the stored charge ensures a shift of the threshold voltage higher than 0.15 V (Figure 7). The target for NVM applications is retention time equal to 10 years ($\approx 3\ 10^8$ s) for a writing time equal to 1 ms.

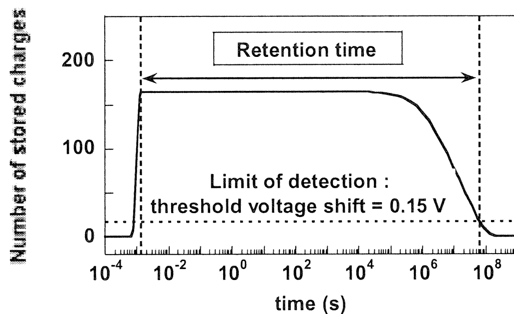



Figure 7 : Definition of the Retention time. (dots density : 1.6 $10^{11}$ $cm^{-2}$, $V_{write}$ = 5 V, $T_{write}$ = 1 ms).

## 4.1 Impact of the size of the dots

First, we analyze the impact of the size of the dots on the retention time in the case of ellipsoidal dots. Our model enables us to calculate under which conditions of metallic dots size, the retention time is more than 10 years (Figure 8) : The radii $R_H$ and $R_V$ must be less than 1 nm (this limit could be improved with Silicon dots).

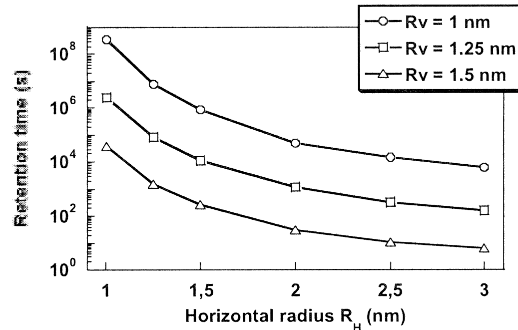



Figure 8 : Retention time vs. the geometries of the dots (dots density : 1.6 $10^{11}$ $cm^{-2}$, h = 7.5 nm, $V_{write}$ = 5 V, $T_{write}$ = 1 ms).

Figure 8 and Figure 9 show the precise impact of the radii $R_H$ and $R_V$ on the retention time : We note that it is highly sensitive to the two radii and that $R_V$ is the most influent (Figure 9).

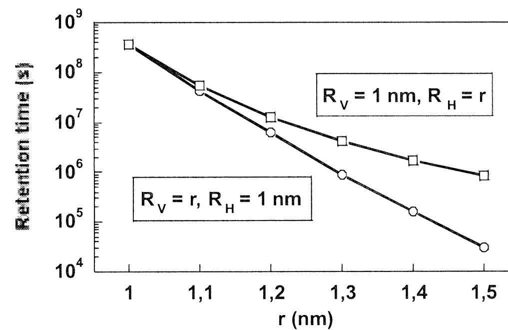



Figure 9 : Impact of $R_H$ and $R_V$ on the Retention time. (dots density : 1.6 $10^{11}$ $cm^{-2}$, $V_{write}$ = 5 V, $T_{write}$ = 1 ms).

## 4.2 Impact of the inter-gate distance h

As the smallest dots give the best retention time, in the following, we focus on the case $R_H$ = $R_V$ = 1 nm, which allows to reach 10 years retention.

We analyze the impact of the distance, h, between the two gates (Figure 1). Figure 10 shows that the shape of the curve $N_{FG}(t)$ strongly depends on h :

- For small h, the number of stored charges is high but the retention is too low.
- On the opposite, large h lead to good retention times but the number of charges is low (Figure 10).

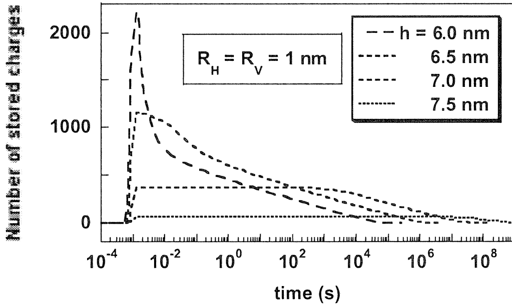



Figure 10 : Impact of h between gates on $N_{FG}(t)$ (dots density : 1.6 $10^{11}$ $cm^{-2}$, $V_{write}$ = 5 V, $T_{write}$ = 1 ms).

And too large values for h (≥ 8nm) don't allow to reach the limit of detection (Figure 10 and Figure 11). In these cases, the thickness of the tunnel oxide around the dots is more than 3 nm which leads to very large tunnel resistances and therefore to very small currents through the double tunnel junctions. So, for large h, the charge of the Floating Gate (which only depends on these tunnels currents) doesn't increase much. But for the same physical reason, the retention is better because of the small tunnel leakage.

At the opposite, small h values lead to good writing characteristics but small retention times (the leakage degrades the retention).

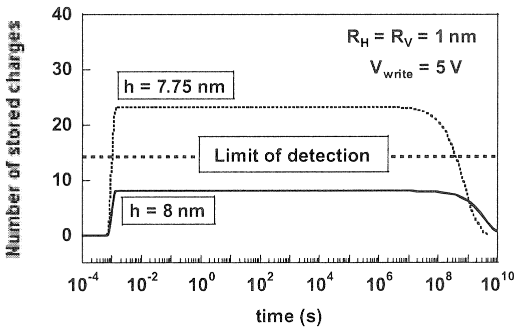



Figure 11 : Determination of the threshold value of h (~ 7.75 nm) above which the detection is no more possible.

Figure 12 shows that the retention time depends exponentially on h. This is qualitatively explained by the exponential relation between tunnel currents and oxide barrier thickness.

But for h higher than a limit ($h_{lim}$), the retention time falls down to zero (Figure 11). This limit depends on the writing voltage $V_W$ : Figure 12 shows that $h_{lim}(V_W)$ increases when $V_W$ increases, which leads to better retention times.

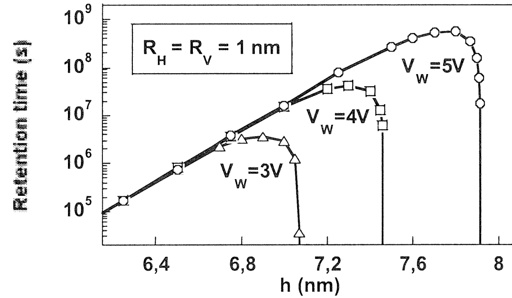



Figure 12 : Retention time vs. distance h between gates for $V_{write}$ = 3, 4 and 5 V ($T_{write}$ = 1 ms).

## 5 CONCLUSIONS

We have analyzed the impact of the technological parameters (size of the dots, geometries of the cell) and of the writing voltage on the retention time for NVM applications. Thanks to the compact model that we have developed for the MTJM cell, we have shown that the geometries of the dots and the inter-gate thickness may be optimized to reach 10 years retention.

This work has been carried out, in the frame of CEA-LETI / CPMA collaboration, with PLATO Organization teams and tools.

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