Unified RLC Model for On-chip Interconnects

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ABSTRACT

We present a unified RLC model for deep sub-micron on-chip interconnects. The model consists of two components, a quasi-3D capacitance extraction based on a novel concept of "effective width" and an effective loop inductance model. In the quasi-3D capacitance model, the effective width provides an efficient way to decompose any 3D structure into a series of 2D segments, resulting in an accurate capacitance extraction. Validation and extraction methodology for the effective loop inductance, which is more computationally efficient than the partial inductance approach, will be addressed. Random capacitive coupling effect, which is important at high frequencies, will be investigated through a full-wave solver and S-parameter analysis, leading to a frequency-dependent RLC model valid up to 100GHz.

Keywords: On-Chip Interconnect, Compact Modeling, Capacitance, Inductance.

1 INTRODUCTION

Increasing interconnect delay and signal integrity problems in ULSI systems make accurate understanding and modeling of wires more critical than ever [1]. In particular, the growing complexity of today's ULSI systems requires an accurate compact model of on-chip wires for fast full-chip-level extraction. In on-chip interconnect modeling, the contrasting behaviors of capacitance and inductance must be taken into consideration. Since electrostatic interaction between wires is very short-range, only nearest neighbors are considered for capacitance extraction. However, the capacitance is a sensitive function of geometry, making any single closed-form model for general 3D wires formidable. Therefore quasi-3D (Q-3D or 2.5D) modeling [2, 3] became a promising approach to alleviate the difficulty of pure 3D model. The major challenge in Q-3D model is how to decompose a 3D structure into 2D structures and include effects of the fringing electric field between adjacent 2D structures. Here we propose a convenient concept, an effective width, to provide an efficient and physics-based Q-3D model.

On the other hand, magnetic field has long-range interaction. Therefore in inductance extraction, not only nearest neighbors but also distant wires must be considered. Defining current loops or finding return paths becomes a major challenge in inductance modeling. Although partial-inductance-based methodology [4, 5] has been used to alleviate the difficulty of finding return paths, it is restricted to small structures due to computational difficulties in solving the resulting dense matrix. Here we present an effective loop inductance model for compact and hierarchical model construction of high-speed on-chip wires. To meet high-frequency demands of today's ULSI systems, we include the random capacitive coupling effect on inductance, which becomes dominant at frequencies above a few GHz. Finally, combining the capacitance and inductance model, we generate a frequency-dependent SPICE-compatible RLC model.

2 CAPACITANCE MODEL

2.1 Effective Width of Crossover Line

Various components of 3D crossover capacitance (C_{cross}) are illustrated in Fig. 1. Keeping the 2D cross-section along aa' and corresponding capacitance (C_{self}) in mind, the components are represented in 2D-like forms. An effective width (W_{eff}) of the crossover wire is defined as follows.

$$\begin{aligned} C_{cross} &= W_1 W_2 C^a + W_1 C^{fr1} + W_2 C^{fr2} + C_{wtw} \\ &= W_2 (W_1 C^a + C^{fr2}) + W_1 C^{fr1} + C_{wtw} \\ &= \{W_2 + \frac{W_1 C^{fr1}}{C_{self}} + \frac{C_{wtw}}{C_{self}}\} C_{self} = W_{eff} C_{self} \end{aligned} \quad (1)$$

with
$$W_{eff} \equiv W_2 + \frac{W_1 C^{fr1}}{C_{self}} + \frac{C_{wtw}}{C_{self}} \quad (2)$$

As shown in equation (2), W_{eff} is enlarged from the physical width of crossover line (W_2) by the 2D fringing field and the 3D wall-to-wall fringing field. With equation (2), W_{eff} of any wire can be calculated if we have a 2D and a wall-to-wall capacitance models. We used functional fitting methodology [6] to obtain 3D wall-to-wall capacitance (C_{wtw}) as well as 2D capacitances (C^a, C^{fr1}, C^{fr2}). By including the closed form wall-to-wall fringing capacitance model for the first time, our crossover capacitance model and effective width concept were confirmed to provide accurate capacitance for deep sub-micron wires [7].

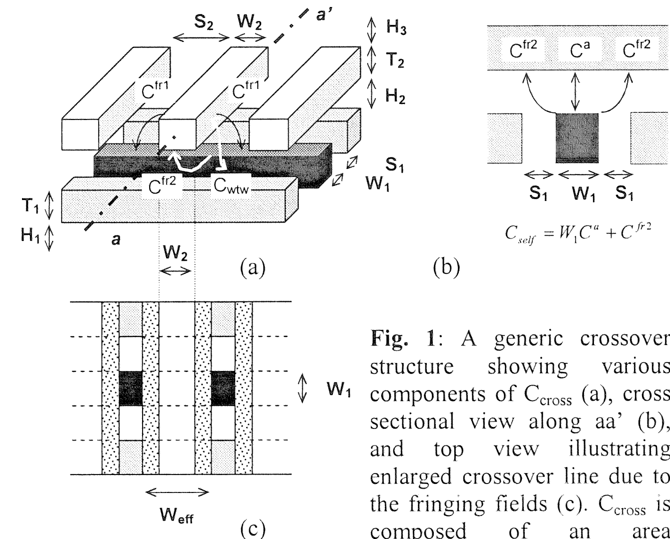


Fig. 1: A generic crossover structure showing various components of C_{cross} (a), cross sectional view along aa' (b), and top view illustrating enlarged crossover line due to the fringing fields (c). C_{cross} is composed of an area component (C^a), 2D fringing components (C^{fr1}, C^{fr2}), and 3D wall-to-wall fringing component (C_{wtw}).

2.2 Q-3D Extraction Using Effective Width

W_{eff}, defined in the previous section, can be interpreted as an electrostatic width of the crossover line. With this interpretation, W_{eff} provides a physics-based approach to decompose any general 3D wire structure into 2D structures for Q-3D extraction, as illustrated in Fig. 2. If we segment each crossover line along the object line with W_{eff}, capacitance for each cross-section (C_i) is readily determined by the 2D model as outlined in Section 2.1. Thus the total capacitance is determined by simply adding the capacitances (C_iW_i) from each 2D segment. Here C_i includes coupling capacitance to parallel neighbors as well as self capacitance to crossing neighbors.

2.3 Generalization and Applications

In the general case of non-orthogonal crossover as described in Fig. 3, we note that area and edge are each increased by $1/\sin(\phi)$ for rotation angle ϕ, leading to increase of area capacitance and 2D fringing capacitance. Fortunately, we find that $C_{wtw}(\phi)$ also assumes the same ϕ dependency. Thus $C_{cross}(\phi)$ and $W_{eff}(\phi)$ are generalized as follows.

$$C_{cross}(\phi)=\left\{\frac{W_2}{\sin(\phi)}+\frac{W_1C^{fr1}}{C_{self}\sin(\phi)}+\frac{C_{wtw}(90°)}{C_{self}\sin(\phi)}\right\}C_{self}=W_{eff}(\phi)C_{self} \quad (3)$$

with

$$W_{eff}(\phi)\equiv\frac{W_2}{\sin(\phi)}+\frac{W_1C^{fr1}}{C_{self}\sin(\phi)}+\frac{C_{wtw}(90°)}{C_{self}\sin(\phi)}=W_{eff}(90°)\csc(\phi) \quad (4)$$

In Fig. 3, the generalized model shows excellent match with a 3D field solver. We apply the proposed Q-3D model using effective width for a long line with parallel and crossing neighbors as shown in Fig. 4. Our Q-3D model agrees well with 3D field solver, within 4% error for either orthogonal or diagonal architecture. In addition, either architecture yields virtually the same results. This is due to the fact that for a long wire, the density of crossover lines decreases by $\sin(\phi)$, which precisely offsets the increase in capacitance.

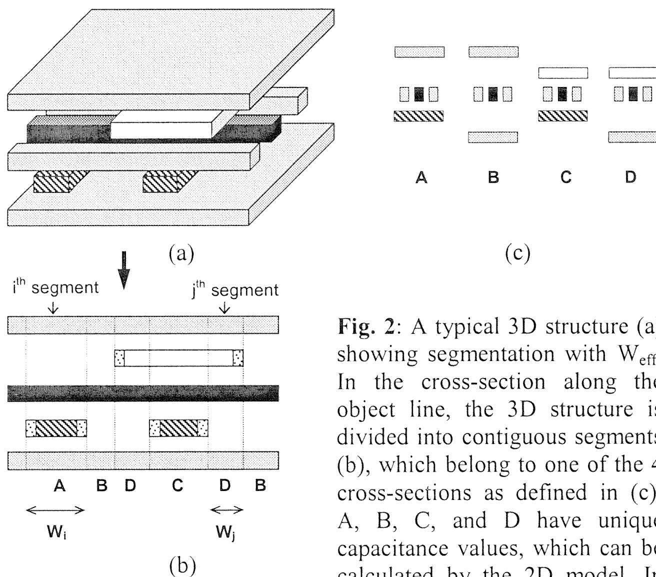


Fig. 2: A typical 3D structure (a) showing segmentation with W_{eff}. In the cross-section along the object line, the 3D structure is divided into contiguous segments (b), which belong to one of the 4 cross-sections as defined in (c). A, B, C, and D have unique capacitance values, which can be calculated by the 2D model. In (b), W_{eff} of each crossover line defines the actual width (W_i) of the relevant segment used to obtain the total capacitance.

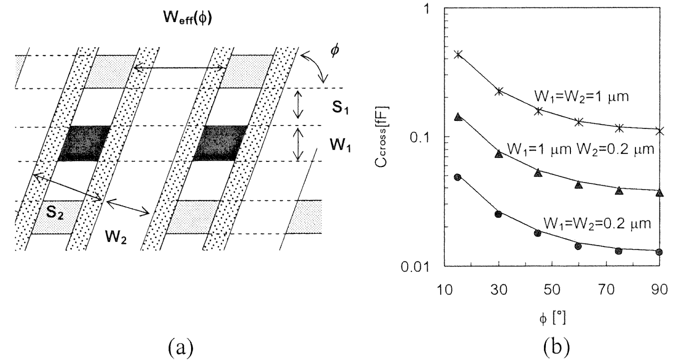
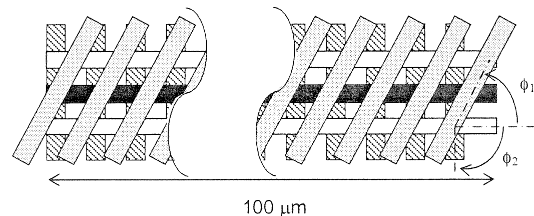


Fig. 3: Schematic drawing of a general non-orthogonal crossover wire structure (a) and C_{cross} vs. angle (b). In (b), where S_1,S_2=0.2μm, T_1,T_2=0.35μm, and H_1,H_2,H_3=0.45μm, our model (line) and 3D field solver (symbol) are compared.



Routing \ C[fF]	Model	Field Solver
Orthogonal (ϕ_1=ϕ_1=90°)	20.2	19.7
Diagonal I (ϕ_1=ϕ_2= 45°)	20.4	19.7
Diagonal II (ϕ_1=90°, ϕ_2=45°)	20.3	19.6

Fig. 4: An application structure and extracted total capacitance for a 100μm long wire (black line). Here we used the same process and design rule, W=S=0.4, T=0.35, and H=0.45 μm for every metal layers and routings.

3 INDUCTANCE MODEL

A typical high-speed on-chip interconnect configuration is shown in Fig. 5. At relatively low frequencies, each power grid provides a good return path due to low resistance of the grid. As the frequency of the signal advances into multi-GHz regime, random signal lines start to participate in the return path. After all, virtually all the wires surrounding the high-speed signal line can function as possible return paths. We consider return path through the power grid and random signal lines separately and then combine their effects on inductance.

3.1 Effective Loop Inductance and Resistance

As illustrated in Fig. 6, inductive interaction within every segment surrounding a signal line can be incorporated into an effective inductance, generating a single isolated RL model. The effective loop inductance (L_{eff}) and resistance (R_{eff}) in Fig. 6 can be analytically derived as follows [8] using the equivalence of energy or power stored in the two equivalent systems.

$$\frac{1}{2}\sum_i\sum_j L_{ij}I_iI_j\equiv\frac{1}{2}L_{eff}I^2,\qquad \sum_k R_kI_k^2\equiv R_{eff}I^2 \quad (5)$$

Power grid configuration, which is common in high-speed digital interconnects, is an important consideration in our analysis. We investigate the linearity of R_{eff} and L_{eff} for a signal line on power grid using FastHenry [9]. As shown in Fig. 7, L_{eff} and R_{eff} show excellent linearity, except at low frequencies for L_{eff}. Low-frequency inductance displays super-linearity because the return current spreads out as the length of wire increases. Thus, for high-speed interconnects on power grid, the linearity observed provides a sound basis for hierarchical model construction for a long wire by concatenating models for all segments. In Fig. 8, we compare our analytic effective loop inductance model with FastHenry. Our model shows excellent match with simulation except for a slight underestimation of inductance at low frequencies, which is caused by the super-linearity. Since low-frequency impedance is dominated by resistance, the underestimation has no significant effect on the total impedance of the signal line and on the signal transfer characteristics [10].

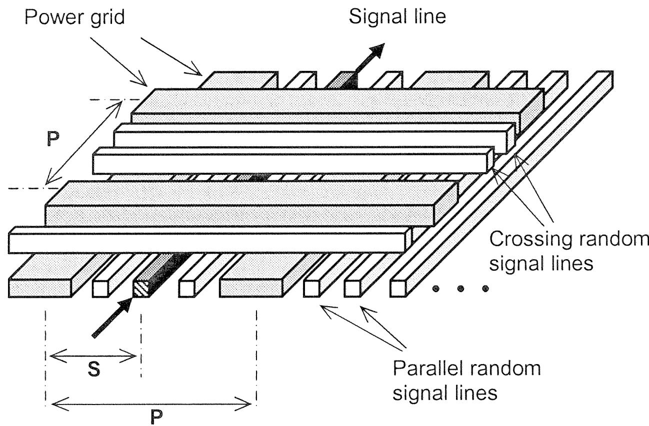


Fig. 5: Typical high-speed on-chip interconnects. Horizontal and vertical power grids are tied together through vias. P and S denote the pitch of power grid and the distance between signal line and the nearest power grid, respectively. Wires are assumed to be copper with a thickness of 0.35μm each. Widths of signal line and power grid are assumed to be 1μm and 4μm, respectively.

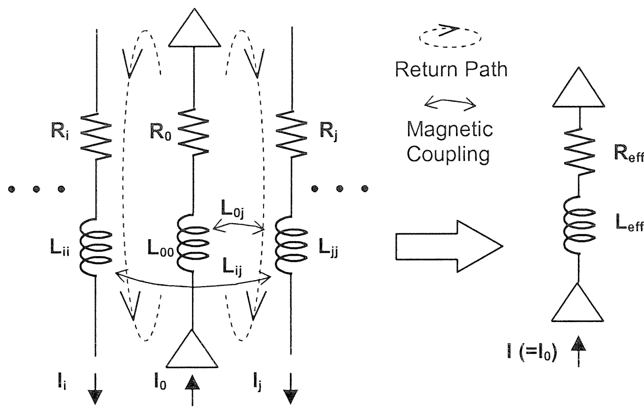


Fig. 6: Simplification of multiple return paths into a single signal line with effective resistance (R_{eff}) and effective inductance (L_{eff}). L_{ij} represents a partial inductance of ith line segment, induced by a current I_j flowing through j^{th} line segment. I (=I_0) represents the current flowing through the signal line, which is equal to the sum of all return currents I_j, j>0.

3.2 Random Signal Line Effect

As Kleveland demonstrated [1], random signal lines reduce the high-frequency inductance significantly by providing a closer return path through capacitive coupling. We investigate this effect with a full-wave solver [11]. Telegrapher's parameters, RLCG, are extracted from S-parameters obtained from simulations for the structure as shown in Fig. 5 with various random coupling lines. At high frequencies, parallel random capacitive coupling can provide a pseudo ground line next to the signal line, inferring quasi TEM-mode wave propagation [12]. This hypothesis is supported by a close relationship between L and C as shown in Fig. 9. Based on lossless transmission line theory, the reciprocal of the LC product for TEM wave being the square of the phase velocity, our simulation data are fitted to a semi-empirical expression

$$(LC)^{-0.5} = SWF^{-1}\nu \qquad (6)$$

where ν is the phase velocity in the medium and SWF is the dimensionless "slow-wave factor" used to characterize the deviation from ideal wave propagation along a lossless transmission line.

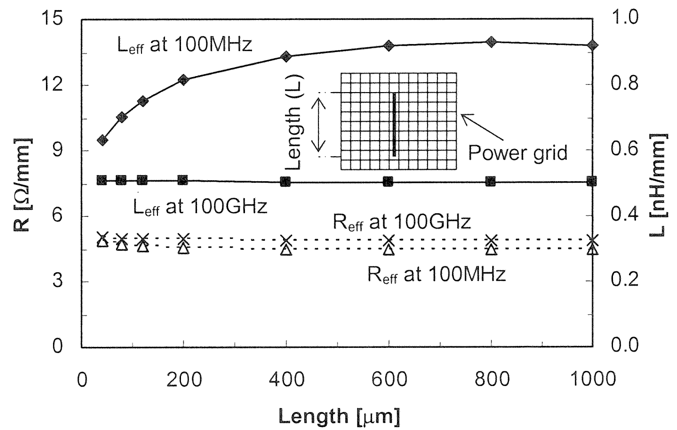


Fig.7: R_{eff} and L_{eff} vs. length of wire on power grid (see inset). S=3μm and P=40μm in Fig. 5 are assumed. In our FastHenry simulations, skin effect is not considered, in order to focus on proximity effect.

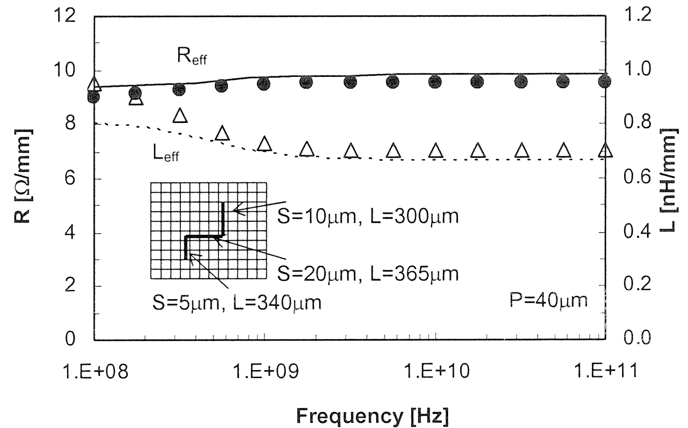


Fig. 8: L_{eff} extracted using our effective loop inductance model (line) is compared with FastHenry results (symbol) for a signal line on power grid as shown in inset. Here frequency dependency is modeled using the circuit shown in Fig. 10. For R and L extractions, only up to the second nearest grid pairs are considered.

In Fig. 9, crossing random coupling lines show a slightly slower wave-like propagation mode than parallel lines, as the former can support electric field more easily than magnetic field. By introducing a separate SWF for parallel and crossing lines, which depends only on technology, the high-frequency inductance in TEM-mode is extracted from the capacitance of the signal line (as presented in Section 2) using (6).

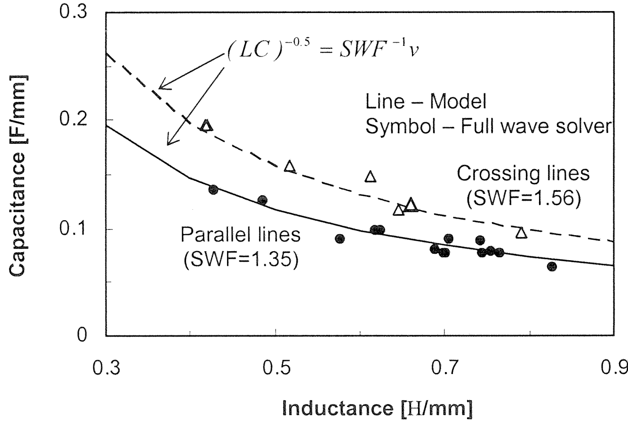
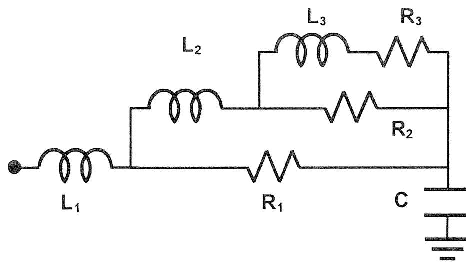


Fig. 9: Relationship between capacitance and inductance obtained from full-wave solver at 20.1GHz for various capacitive coupling configurations. Lines represent the slow-wave mode formulas given by Equation (6).

3.3 Frequency-Dependent RLC model

In Fig. 10, we use parallel branches to model frequency dependency of R_{eff} and L_{eff}, as in Krauter [13]. R_{eff} and L_{eff} at low and medium frequencies (R_{LF}, L_{LF}, R_{MF}, and L_{MF}) are extracted from the power grid configuration, while L_{HF} and R_{HF} are extracted from the configuration of random signal lines using (6). We apply a modified skin-effect formula [1] to extract R_{HF}, because charge flows near the surface at high frequencies. We applied our effective loop inductance model to a structure shown in Fig. 11. Our model shows an excellent match with full-wave solver for a wide range of frequencies, from 100 MHz to 100 GHz, while the previous model [13] significantly overestimates high-frequency inductance and underestimates high-frequency resistance.



$$R_{LF} = R_1 \| R_2 \| R_3 ; \quad L_{LF} = L_1 + \left(\frac{R_1}{R_1 + R_2 \| R_3} \right)^2 \left(L_2 + \left(\frac{R_2}{R_2 + R_3} \right)^2 L_3 \right)$$

$$R_{MF} = R_1 \| R_2 ; \quad L_{MF} = L_1 + \left(\frac{R_1}{R_1 + R_2} \right)^2 L_2 ; \quad R_{HF} = R_1 ; \quad L_{HF} = L_1$$

Fig. 10: Frequency-dependent RLC circuit model. The lumped element values are calculated using the given equations.

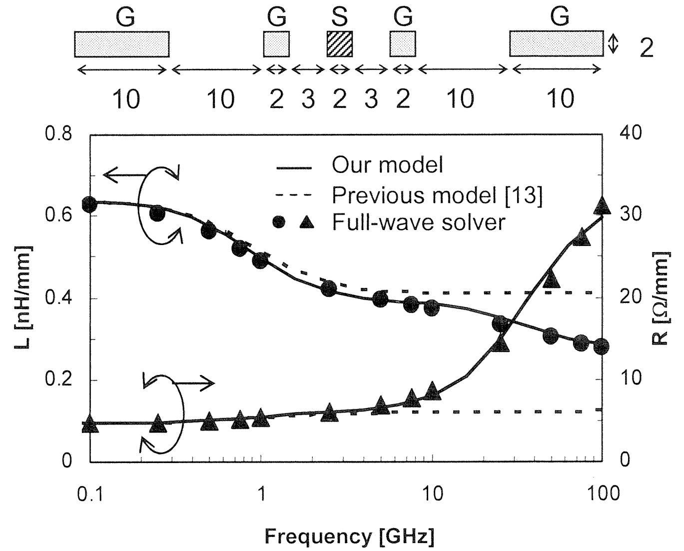


Fig. 11: Frequency-dependent resistance and inductance for a structure shown above. Numbers in the structure represent dimensions of the structure in μm and random lines (both parallel and crossing) are not shown for simplicity.

4 CONCLUSION

Aiming for full-chip-level applications, we have developed a unified compact RLC model for interconnects. By combining a quasi-3D capacitance model and effective loop inductance model, we have successfully created a scheme for modeling and parameter extraction for on-chip interconnects valid up to 100GHz.

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