Unified Length-/Width-Dependent Threshold Voltage Model with Reverse Short-Channel and Inverse Narrow-Width Effects

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ABSTRACT

This paper describes a scalable threshold voltage model for the entire range of drawn length and width, considering important short-channel, reverse short-channel, narrow-width, and inverse narrow-width effects using a unified effective channel doping. The model has a simple compact form that can used to characterize advanced deep-submicron devices with halo-implanted MOSFET. The model has been verified with the experimental data from 0.18-μm CMOS shallow trench isolation technology wafer.

Keywords: Deep-submicron MOSFET, threshold voltage, compact model, reverse short-channel effect, inverse narrow-width effect.

1 INTRODUCTION

The impact of geometry variation and scaling on MOSFET electrical characteristics is becoming increasingly important as the technology is scaled into the deep-submicron regime. It becomes equally as important to model these geometry effects as modeling the bias-dependent characteristics in a compact MOSFET model, in which the most sensitive parameter is the threshold voltage (V_t). Experimental data show V_t roll-up and roll-off at decreasing channel length, which is the well-known short-channel effect (SCE) and reverse short-channel effect (RSCE) as well as V_t roll-up (slightly for short-/wide-channel) and roll-off at decreasing channel width for trench-isolated CMOS devices with nonuniformly-doped substrate [1]–[3], which is known as inverse narrow-width effect (INWE). The observed effects have been attributed to: i) the fringing field from the sidewall, which contributes to the fringing capacitance resulting in increased total gate capacitance [1] and, hence, V_t roll-off; ii) an increase in the minimum surface potential in the narrow-width device relative to that of the wide-channel device [2]; and iii) an increase in the effective channel doping concentration at decreasing channel width [3], giving rise to a slight V_t roll-up for wide channel before it rolls off at decreasing channel width.

In this paper, we focus on the development of a unified geometry-dependent V_t model based on "technology characterization" approach for the entire range of drawn length (L) and drawn width (W) of a CMOS shallow trench isolation (STI) transistor. This has been achieved based on the idea of our previous length-dependent $V_t(L)$ model [4], [5] by including NWE and INWE, which allows the unified V_t model to be extended to both length and width dimensions at various bias conditions.

The unified geometry-dependent V_t model is formulated from the ideal long-/wide-channel equation with short-/narrow-channel effects built into the model. Seven fitting parameters are introduced for width dependence, which are fitted to the technology data around the average values of the physical parameters. Parameter extraction follows a unique prioritized procedure, starting from simple long-/wide-channel V_t equation, and incorporates SCEs and NWEs for each step in subsequent extraction.

2 MODEL FORMULATION

2.1 Length-Dependent V_t Model

Our previously-developed short-channel V_t model [4]–[6], which includes all major SCEs and RSCEs, is given by

$$V_t = V_{FB} + \phi_s + \gamma_{eff}\sqrt{\phi_{s0} - V_{bs}} \tag{1a}$$

$$V_{FB} = \phi_m - \left(\chi + \tfrac{1}{2}E_g + \tfrac{1}{2}\phi_{s0}\right) - qN_{ss}/C_{ox} \tag{1b}$$

is the flatband voltage and

$$C_{ox} = \varepsilon_{ox}/t_{ox} \tag{1c}$$

is the oxide capacitance.

$$\phi_{s0} = 2\phi_F + \Delta = 2(kT/q)\ln(N_{ch}/n_i) + \Delta_1 V_{ds} \tag{1d}$$

is the long-channel surface potential at strong inversion.

$$\gamma_{eff} = \gamma - \frac{\lambda}{L_{eff}}\frac{2\varepsilon_{si}}{C_{ox}}\left(\sqrt{\phi_s - V_{bs}} + \frac{\delta V_{ds}}{\sqrt{\phi_s - V_{bs}}}\right) \tag{1e}$$

is the effective body factor including charge sharing, which at long channel approaches

$$\gamma = \sqrt{2q\varepsilon_{si}N_{ch}}/C_{ox} \tag{1f}$$

$$\phi_s = \phi_{s0} - \Delta\phi_s \tag{1g}$$

is the short-channel surface potential at strong inversion, with a barrier lowering from quasi-2D solution:

$$\Delta\phi_s = \frac{1}{\cosh\left(L_{eff}/2l_\alpha\right)}\left[(V_{bi} - \phi_{s0})\cosh\left(\frac{z}{2}\right) + \frac{\varphi V_{ds}}{2}\frac{\sinh\left(\frac{L_{eff}}{2l_\alpha} - \frac{z}{2}\right)}{\sinh\left(\frac{L_{eff}}{2l_\alpha}\right)}\right] \tag{1h}$$

$$z = \ln\left(\frac{V_{bi} - \phi_{s0} + V_{ds}}{V_{bi} - \phi_{s0}}\right) \quad (1i)$$

$$V_{bi} = (kT/q)\ln\left(N_{sd} N_{eff} / n_i^2\right) \quad (1j)$$

$$l_\alpha = \alpha(\phi_{s0} - V_{bs})^{0.25} \quad (1k)$$

The effective doping is derived from integrating two Gaussian pile-up profiles with peak concentration $N_{pile} = \kappa N_{ch}$, lateral spread

$$l_\beta = \beta(\phi_{s0} - V_{bs})^{0.25} \quad (1l)$$

and centroid l_μ:

$$N_{eff} = N_{ch} + \frac{\sqrt{\pi}\kappa N_{ch}}{L_{eff}/l_\beta}\left[\mathrm{erf}\left(\frac{L_{eff} - l_\mu}{l_\beta}\right) + \mathrm{erf}\left(\frac{l_\mu}{l_\beta}\right)\right] \quad (1m)$$

in which

$$L_{eff} = L - \Delta_{CD} - 2\sigma x_j \quad (1n)$$

The above $V_t(L)$ model approaches the well-known long-channel equation $V_t = V_{FB} + \phi_{s0} + \gamma\sqrt{\phi_{s0} - V_{bs}}$ in the long-channel limit: $N_{eff} \to N_{ch}$, $\gamma_{eff} \to \gamma$, and $\phi_s \to \phi_{s0}$.

2.2 Width-Dependent V_t Model

To incorporate NWEs and INWEs into the V_t model, the first modification is the gate oxide capacitance (C_g) to include the field-induced edge fringing effect for STI-isolated CMOS devices, given by

$$C_g = C_{ox} + 2C_f \quad (2a)$$

in which the fringing capacitance is formulated as [1]

$$C_f = \left(\frac{2\varepsilon_{ox}}{\pi W_{eff}}\right)\ln\left(\frac{2\pi t_d}{t_{ox}}\right) \quad (2b)$$

where t_d is the depth of recessed oxide and τ is a process-dependent fitting parameter. Eq. (2a) will replace all C_{ox} in Eqs. (1).

The width effect on surface potential shift [2] ($\Delta\phi_{s,w}$) is derived based on Gauss's law applied to a rectangular box of height X_{dep} and width ΔW:

$$\varepsilon_{si} X_{dep} \frac{dE_w(z)}{dz} + \varepsilon_{ox}\frac{V_{gs} - V_{FB} - \phi_s(z)}{t_{ox}} = qN_{ch}X_{dep} \quad (3a)$$

where $E_w(z)$ is the vertical field along the width dimension (z), $\phi_s(z)$ is the channel potential at the Si–SiO_2 interface. The solution to (3a) under boundary conditions of $V(0) = V_{bi}$ and $V(W_{eff}) = V_{bi}$ is

$$\begin{aligned}\phi_s(W) &= \phi_{s0} + (V_{bi} - \phi_{s0})\frac{\sinh(W/l_{a,w})}{\sinh(W_{eff}/l_{a,w})} \\ &\quad + (V_{bi} - \phi_{s0})\frac{\sinh[(W_{eff} - W)/l_{a,w}]}{\sinh(W_{eff}/l_{a,w})} \\ &= \phi_{s0} + \frac{(V_{bi} - \phi_{s0})}{\cosh(W_{eff}/2l_{a,w})}\end{aligned} \quad (3b)$$

To account for the surface-potential lowering due to narrow width, Eq. (1g) is modified to be

$$\phi_s = \phi_{s0} - \Delta\phi_s - \Delta\phi_{s,w} \quad (3c)$$

where

$$\Delta\phi_{s,w} = \frac{(V_{bi} - \phi_{s0})}{\cosh(W_{eff}/2l_{a,w})} \quad (3d)$$

$$l_{a,w} = a_w(L_{\min}/L)^{\omega_1}(\phi_{s0} - V_{bs})^{0.25} \quad (3e)$$

is the characteristic length with an empirical length dependence term $(L_{min}/L)^{\omega_1}$, with α_w and ω_1 as fitting parameters.

The INWE [3] is modeled in a similar way as our RSCE V_t model by assuming two Gaussian profiles (with peak doping $N_{pile,w}$, lateral characteristic length $l_{\beta,w}$, and centroid l_ω) at $z = 0$ and $z = W_{eff}$, as shown schematically in Fig. 1, and integrating along the channel width. The combined effective doping including length and width effects, which replaces Eq. (1m), is given by

$$\begin{aligned}N_{eff} &= N_{ch} + \frac{\sqrt{\pi}\kappa N_{ch}}{L_{eff}/l_\beta}\left[\mathrm{erf}\left(\frac{L_{eff} - l_\mu}{l_\beta}\right) + \mathrm{erf}\left(\frac{l_\mu}{l_\beta}\right)\right] + \\ &\quad \frac{\sqrt{\pi}\kappa_w(L_{\min}/L)^{\omega_2} N_{ch}}{W_{eff}/l_{\beta,w}}\left[\mathrm{erf}\left(\frac{W_{eff} - l_\omega}{l_{\beta,w}}\right) + \mathrm{erf}\left(\frac{l_\omega}{l_{\beta,w}}\right)\right]\end{aligned} \quad (4a)$$

$$l_{\beta,w} = \beta_w(\phi_{s0} - V_{bs})^{0.25} \quad (4b)$$

with four error functions to characterize the pile-up profiles at the corners in the channel length and width dimensions, where the peak doping $N_{pile,w} = \kappa_w(L_{min}/L)^{\omega_2} N_{ch}$ includes an empirical length dependence with β_w, κ_w, and ω_2 as fitting parameters. In all the above equations, effective channel width is

$$W_{eff} = W - \Delta W \quad (4c)$$

where ΔW is an optimization parameter.

3 PARAMETER EXTRACTION

In order to verify the unified length/width effects of $V_t(L, W)$ model, a 0.18-μm CMOS STI wafer is measured. Threshold voltages for various device geometries at different bias conditions have been extracted from $I_{ds} - V_{gs}$ curves based on the constant-current definition. Model parameters for $V_t(L)$ that include all major SCEs and RSCEs have been appropriately extracted for wide-channel by fitting one set of $V_t - V_{bs}$ data for long-channel V_t parameter extraction and four sets of $V_t - L$ data at corner bias for SCE and RSCE extraction [5], which requires a *one-iteration* extraction procedure.

In order to separate the different INWEs for long- and short-channel devices, we assume that the effect of V_t roll-up and surface-potential shift at decreasing channel width for long channel is small and can be neglected, and the V_t roll-off for long-/narrow-channel device is mainly from the fringing capacitance. The idea behind this assumption is reflected in the empirical length-dependent effective $\alpha_{w,eff} = \alpha_w(L_{min}/L)^{\omega_1}$ for $\Delta\phi_{s,w}$ and effective $\kappa_{w,eff} = \kappa_w(L_{min}/L)^{\omega_2}$ for N_{eff}, both diminishing at very long channel, in which ω_1 and

ω_2 are treated as (fixed) fitting parameters for fine tuning length dependence at short channel.

Starting from long-channel, the parameter τ is first extracted from the $V_t - W$ data at low drain and high body bias with α_w and κ_w being set to zero. This is followed by extracting the surface-potential shift and the effective doping due to V_t roll-off and roll-up at decreasing channel width at short-channel, in which $V_t - W$ data are used to extract α_w, β_w, and κ_w. ω_1 and ω_2 are extracted from $V_t - W$ data at low drain and high body bias at $L = 0.25$-μm in this work. The effective channel width (W_{eff}) is obtained through optimization loop on ΔW for minimum error in the modeled $V_t(W)$. The sequence of parameter extraction and the corner geometry/bias conditions are shown in Fig. 2.

4 RESULTS AND DISCUSSION

Result of the unified $V_t(L, W)$ model are shown in Figs. 3–6. Fig. 3 shows the total gate capacitance, including the fringing capacitance, normalized to the oxide capacitance C_{ox}, which accounts for the major V_t roll-off, and the surface-potential shift $\Delta\phi_{s,w}$ due to narrow-width effect. The Gaussian doping profiles along the channel width for three channel-length devices are shown in Fig. 4, and the corresponding effective (integrated) doping concentrations for different channel-width devices are plotted in Fig. 5, which models the observed minor V_t roll-up at large W.

The V_t model predictions for different device geometries at various biasing conditions are shown in Fig. 6, which demonstrates very good agreement with measured data.

It is worth mentioning that with the addition of 7 parameters (*regression*: τ, β_w, α_w, κ_w; *optimization*: ΔW; *fixed*: ω_1, ω_2), our unified V_t model can cover the entire geometry/bias range of a given deep-submicron technology. However, the significant of this work is beyond accurate V_t prediction — as will be shown in the companion paper [7] — for simple geometry-dependent current modeling, with only 3 additional fitting parameters for NWE that covers the entire length and width dependency.

5 CONCLUSION

In conclusion, our previous length-dependent V_t model has been extended to both length and width dimensions at various bias conditions. The unified length-/width-dependent V_t model with physical/semi-empirical modeling of all major SCEs, RSCEs, NWEs, and INWEs is shown to be scalable and predictive in the whole range of deep-submicron MOSFET geometry. Complete technology characterization of the threshold voltage can be relatively easily done with automated V_t measurement at the specified corner bias conditions, which simplifies drain-current modeling, which is critical for scalable drain-current model development.

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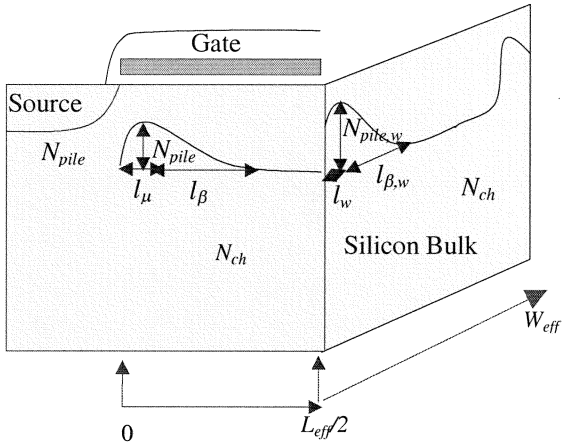

Figure 1: Device structure with two Gaussian profiles along the channel length and two Gaussian profiles along the channel width dimensions.

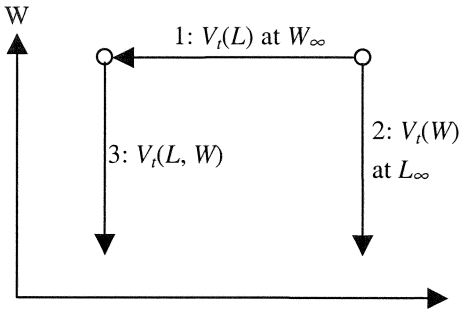

Figure 2: Sequence of parameter extraction at corner geometry/bias condition.

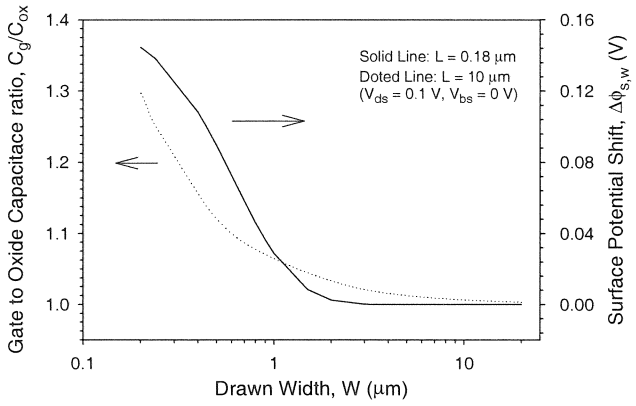

Figure 3: Effect of surface-potential shift and fringing capacitance for narrow-width device, based on the actual 0.18-μm model parameters, showing a 30% increase in C_g due to fringing capacitance and 0.16-V V_t roll-off due to surface-potential shift at the length/bias conditions as indicated for the range of W = 0.2~20-μm variation.

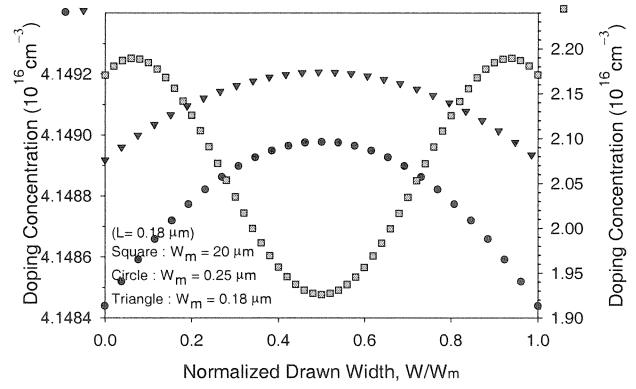

Figure 4: Doping profile along the width dimension at decreasing channel width for short-channel device.

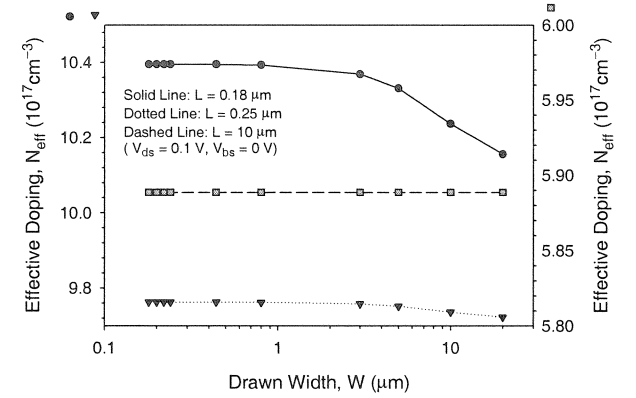

Figure 5: Combined length-/width-dependent effective doping concentration against channel width for three different channel-length devices.

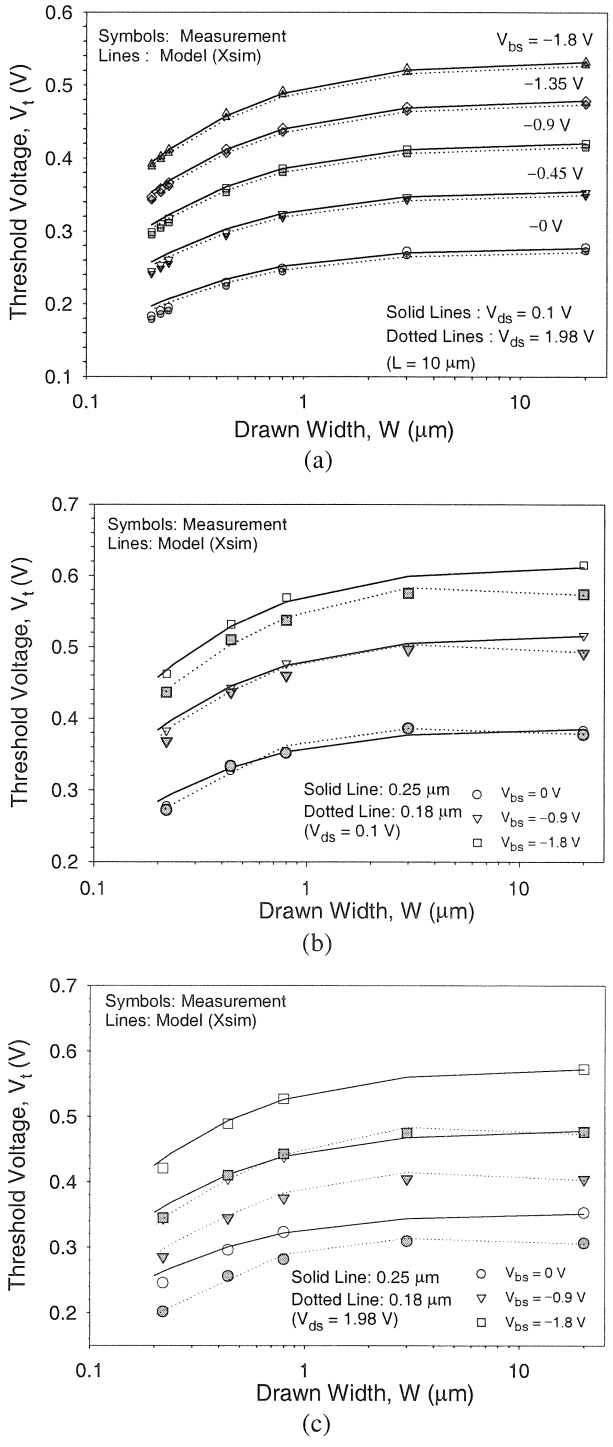

Figure 6: Threshold voltage against channel width for three different channel-length devices at various bias conditions.