Primary Consideration on Compact Modeling of DG MOSFETs with Four-terminal Operation Mode

T. Nakagawa, T. Sekigawa, T. Tsutsumi, E. Suzuki, and H. Koike

Electroinformatics Group
Nanoelectronics Research Institute
National Institute of Advanced Industrial Science and Technology
1-1-1 Umezono, Tsukuba, Ibaraki, 305-8568 Japan
E-mail: nakagawa.tadashi@aist.go.jp

ABSTRACT

Primary consideration for constructing a compact model of double-gate (DG) MOSFETs is discussed. The four-terminal operation mode with the independent front and back gate is considered. The modeled device is a fully-depleted (FD) DG MOSFET with practical silicon channel thickness ranging from 20nm down to 3nm. Two surface channels are inevitably not symmetrical each other. The nature of asymmetry, i.e. the number of active surface channels and the current partition between these two channels, dynamically changes during the circuit operation. As a start point, we consider the double charge-sheet model, where carrier density of two charge-sheets is calculated supposing the current which traverses between them is zero. Accommodation of carrier velocity saturation is also considered.

Keywords: double-gate, MOSFET, modeling, charge-sheet model.

1 INTRODUCTION

Recently, a double-gate (DG) MOSFET structure has attracted much attention as an emerging device concept. The DG MOSFETs, named as XMOS in the first publication[1], was originally proposed by one of the authors in 1984. Since then, we have investigated DG MOSFETs and experimentally confirmed the double-gate operation and the high suppression of the short channel effects (SCE)[2]-[4]. The DG MOSFET is regarded as the most scalable device because of its high current drivability and minimum SCE. As the technology node of ULSIs approaches to less-than-100 nm regime, the advantages of DG MOSFETs become more prominent over the bulk or SOI MOSFETs.

Usually the DG MOSFET is supposed to be used as a three-terminal transistor with one common gate. Compact modeling of this operation mode has been extensively studied[5]. The alternative four-terminal operation mode with the independent front and back gate is promising. This operation mode enables dynamic fine-grain control of threshold voltage (V_t), by changing V_t at each clock and even within a clock, and by applying different V_t control signals to each transistor. Sophisticated use for analog signal processing by using two gates is another interesting application.

Although these approaches sacrifice simplicity at the device level, we can expect performance improvements at the circuit level. In order to evaluate the merit of these modifications on circuit design, a compact and accurate device model of the four-terminal DG MOSFETs is strongly needed. To this demand, we develop a compact four-terminal DG MOSFET model.

2 MODELING

The first consideration for constructing the compact model of DG MOSFETs is the scaling range. Although DG MOSFETs are thought to be used to at the smallest technology node, it is still on the research stage and no commercial product is available. This is simply because of the difficulty of the manufacture. Even when DG MOSFET will appear in the market, the relative difficulty will last. So the interested largest scaling will be present-day scaling and not larger, that is about 100 - 200 nm. The smallest scaling range will be 10-15 nm, where the tunneling current from the source to drain will become unbearable amount. The model must, therefore, cover 200 nm to 10 nm node, and no or small need for the wider coverage.

For DG MOSFETs, channel silicon thickness is a most important parameter. Silicon layer for the SOI structure as thin as 10 nm is already available today. Since DG MOSFETs prefer thinner channel, the thickest channel to be considered will be 10-20 nm. From the device-physics point of view, channel thickness of 3-4 nm is optimum[6], since the electron mobility will reach the maximum value there. Since the possible absolute limit of the channel length of about 13 nm requires channel thickness of about 3 nm[7], lower limit of 3 nm is also a good target. Based on these facts, we conclude that the practical silicon channel thickness will range from 20 nm down to 3 nm.

Although the range is not wide, the device physics changes drastically within this range. The conduction channel will be surface channels at the 20 nm thick channel, and it will be a volume channel at the 3 nm thick channel.

If we consider the four terminal operation, two surface channels in the conduction channel is inevitably not symmetrical each other. The number of active surface channels and the current partition between these two surface channels, dynamically change during the circuit operation.

2.1 Double Charge-Sheet Model

To make a compact model for DG MOSFETs with these versatile requirements, we choose a double charge-sheet model as a base model, where electrons (or carriers) in the channel is considered to be sprit into two charge sheets of infinitesimally small thickness, just below/above the two corresponding gate-oxide layers.

Although the charge-sheet model will not account for the charge separation from the semiconductor/oxide interface by the quantum effect, this effect will be included replacing oxide thickness with an effective one. When the channel thickness approach 3 nm, the double charge-sheet model will become unphysical, because quantum effect makes these two charge-sheets coalesce. But the error by keeping the double charge-sheet model will also be small.

When the two gates are constructed with different oxide thickness or with different gate material, or when different voltages are applied to the two gates, charge concentration of the two charge-sheets at the source end will be different. It will be calculated by solving one-dimensional Poisson equation along the channel depth assuming the drain voltage as 0 V,

$$\frac{\partial^2\psi}{\partial x^2} = \frac{q}{\varepsilon_s} n_i e^{\beta\psi}$$

where ψ is the potential, ε_s is the silicon dielectric constant, n_i is the intrinsic carrier density, and $\beta = q/kT$. In this equation, only one carrier type (either electrons or holes) is considered. This assumption corresponds fully-depleted DG MOSFETs.

Integration of this equation along x produces,

$$\left(\frac{\partial\psi}{\partial x}\right)^2 - \left(\left.\frac{\partial\psi}{\partial x}\right|_{x=s1}\right)^2 = \frac{2qn_i}{\varepsilon_s\beta}\left(e^{\beta\psi} - e^{\beta\psi_{s1}}\right),$$

$$\left(\frac{\partial\psi}{\partial x}\right)^2 - \left(\left.\frac{\partial\psi}{\partial x}\right|_{x=s2}\right)^2 = \frac{2qn_i}{\varepsilon_s\beta}\left(e^{\beta\psi} - e^{\beta\psi_{s2}}\right),$$

where $s1$ and $s2$ stand for the upper and the lower silicon/oxide interface. If we choose x to the potential minimum (minimum for electrons, and maximum for holes), the first term of the l.h.s. vanishes. Coupling these equations to the gate-voltage expression;

$$\left(\left.\frac{\partial\psi}{\partial x}\right|_{x=s1}\right)^2 = \left(\frac{C_{OX1}}{\varepsilon_s}\right)^2 (V_{G1} - \psi_{s1})^2,$$

$$\left(\left.\frac{\partial\psi}{\partial x}\right|_{x=s2}\right)^2 = \left(\frac{C_{OX2}}{\varepsilon_s}\right)^2 (V_{G2} - \psi_{s2})^2$$

we obtain

$$\left(\frac{C_{OX1}}{\varepsilon_s}\right)^2 (V_{G1} - \psi_{s1})^2 + \frac{2qn_i}{\varepsilon_s\beta}\left(e^{\beta\psi_M} - e^{\beta\psi_{s1}}\right) = 0$$

$$\left(\frac{C_{OX2}}{\varepsilon_s}\right)^2 (V_{G2} - \psi_{s2})^2 + \frac{2qn_i}{\varepsilon_s\beta}\left(e^{\beta\psi_M} - e^{\beta\psi_{s2}}\right) = 0$$

where M stands for the potential-minimum. To calculate the potential-minimum point x_M, the following two equation should be solved iteratively.

$$s1 - x_M = \int_{\psi_M}^{\psi_{s1}} \left(\frac{\partial\psi}{\partial x}\right)^{-1} \partial\psi = \int_{\psi_M}^{\psi_{s1}} \{F_1(\psi,\psi_{s1})\}^{-1/2} \partial\psi$$

$$= \frac{2}{\beta}\{-F_1(-\infty,\psi_{s1})\}^{-1/2} \tan^{-1}\left(\frac{C_{OX1}(V_{G1} - \psi_{s1})}{\varepsilon_s(-F_1(-\infty,\psi_{s1}))^{1/2}}\right),$$

$$s2 - x_M$$

$$= \frac{2}{\beta}\{-F_2(-\infty,\psi_{s2})\}^{-1/2} \tan^{-1}\left(\frac{C_{OX2}(V_{G2} - \psi_{s2})}{\varepsilon_s(-F_2(-\infty,\psi_{s2}))^{1/2}}\right),$$

where

$$F_1(\psi,\psi_{s1}) = \left(\frac{C_{OX1}}{\varepsilon_s}(V_{G1} - \psi_{s1})\right)^2 + \frac{2qn_i}{\varepsilon_s\beta}\left(e^{\beta\psi} - e^{\beta\psi_{s1}}\right),$$

$$F_2(\psi,\psi_{s2}) = \left(\frac{C_{OX2}}{\varepsilon_s}(V_{G2} - \psi_{s2})\right)^2 + \frac{2qn_i}{\varepsilon_s\beta}\left(e^{\beta\psi} - e^{\beta\psi_{s2}}\right).$$

These equations can be solved numerically with the iteration, and the results gives the boundary condition for the potential ψ at the source end; $\psi_{s1}(0)$ and $\psi_{s2}(0)$.

The electron transport in a charge-sheet, taking drift and diffusion into account, is described as;

$$-\mu E(y)n(y) + D\frac{\partial n(y)}{\partial y} = \frac{I}{q}$$

where I is the current, E is the electric field along the channel, D is the diffusion coefficient which obeys the Einstein relation $D = \mu kT/q$. The electric field comes from the spatial change of carrier density, spatial change of depletion layer thickness just below the channel, and the drain electric field. For DG MOSFETs with no channel-

doping, there is no depletion-layer charge. And if we ignore the effect of the drain electric field that extends inside the channel, E will be described, under gradual channel approximation, as

$$E = -\frac{q}{C_{OX}}\frac{\partial n}{\partial y}.$$

These two equations are combined to a transport equation;

$$\mu\left(\frac{q^2}{C_{OX}}n + kT\right)\frac{\partial n}{\partial y} = I.$$

It looks much simpler than Brews' formulation[8], because there is no depletion-layer fixed-charge that may change along the channel.

Solving this analytically and considering the relation

$$C_{OX}\left(V_G - \psi_s(y)\right) = qn(y),$$

we obtain

$$I = \frac{\mu C_{OX}}{\beta L}\left[\left(\beta V_G + 1\right)\left(\psi_s(L) - \psi_s(0)\right) - \frac{\beta}{2}\left(\psi_s(L)^2 - \psi_s(0)^2\right)\right],$$

where L is the channel length. After the method developed by Brews[8], the current in a charge-sheet is then obtained by using the following V_D expression;

$$V_D = \psi_s(L) - \psi_s(0) + \beta \ln\frac{n(0)}{n(L)}.$$

For the double charge-sheet model, we have to solve two equations for each channel. And total current is the sum of the currents of two charge-sheets;

$$I = I_1 + I_2.$$

2.2 Current Mixing between the Sheets

Above discussion assumes that the current for each charge-sheet is constant for the entire channel length. In the rigorous sense, it is not true; I is constant, but I_1 and I_2 are not constant.

If we try to solve the equation supposing that only I is constant, we have to add the equation that describes the carrier transport between two charge-sheets. But it implies that we have to solve everywhere the charge partition equation of the former section. To make the model compact, we keep the independent current assumption.

We assessed this assumption by simulating the channel carrier behavior by using ATLAS device simulator. Figure 1 shows the carrier distribution in the channel of DG MOSFET with 5 nm thick channel and with symmetrical

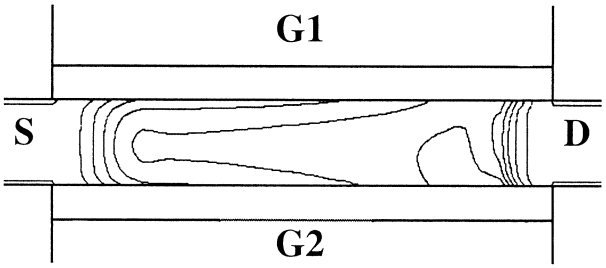

Figure 1: The carrier density in the channel for almost symmetric bias voltages. Channel thickness is 5 nm, the channel length is 110 nm. Drain voltage is 1 V, gate voltages are 0.4 V for G1, 0.3 V for G2. The contour of the charge density is 3 contour/decade.

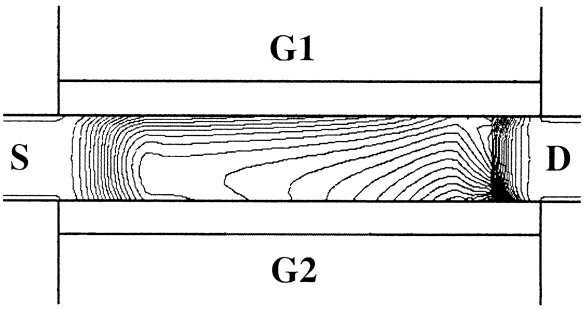

Figure 2: The carrier density in the channel for highly asymmetric bias voltages. Device structure is the same as that in the figure 1. Gate voltages are 0.4 V for G1, 0.1 V for G2. The contour of the charge density is 8 contour/decade.

device structure. The drain voltage is 1 V, and the gate voltages are 0.3 V and 0.4 V. This situation corresponds to the condition that the channel carrier density is asymmetric by the asymmetric gate voltages. The currents in two charge-sheets are different, but these are the same order. In this case, both two charge-sheets are quite distinct from the source to the so-called pinch-off point near the drain. The charge density amid two charge-sheets is small. So the independent current assumption will work very well.

In the figure 2, carrier density under another biasing condition is shown. In this case, the lower gate is biased to 0.1 V, and the upper gate is biased to 0.4 V. Other condition is the same to that of the figure 1. Because the charge density in the lower charge-sheet is much smaller than the upper one, the channel becomes quite asymmetrical. Furthermore, the lower charge-sheet vanishes much before the so-called pinch-off point. This implies that the independent current assumption is not

based on the physical background. It should be, however, noted that the contribution of the lower charge-sheet to the total current is rather small. Therefore, this assumption will be legitimated to achieve the model simplicity.

2.3 Transport Equation in the Channel

The transport model for the charge-sheet discussed above is essentially the same to that first stated by Brews. And this equation will be accurate enough to simulate the DG MOSFETs as a first step.

Since this equation is based on the gradual channel approximation, the equation cannot describe the electric field beyond the so-called pinch-off point. Brews' model can, however, describe the saturation region of the FET characteristics. The trick that is used is the definition of the drain voltage;

$$V_D = \psi_s(L) - \psi_s(0) + \beta \ln \frac{n(0)}{n(L)}$$

or, the drain voltage is defined by the Fermi level change of the electrons. Before saturation, V_D is derived mainly by $\psi_s(L) - \psi_s(0)$. In the saturation region, excess voltage of V_D is supplied by the third term.

The use of Fermi level as the definition of V_D is, in itself, orthodox. But the excess voltage is derived only when $n(L)$ becomes quite small, and, consequently, carrier velocity becomes larger in an unphysical way.

For short-channel devices, velocity saturation is significant phenomenon that must be considered. But as far as the model depends on the presence of the unphysical carrier velocity at the so-called pinch-off point, it is impossible to accommodate the velocity saturation into the model. Instead, in a conventional approach, mobility μ is modified to simulate the device characteristics at the velocity saturation region.

To make a further step for the refined DG MOSFET model, inclusion of the velocity saturation to the model will be necessary. This can be accomplished by replacing the velocity expression to a saturating one;

$$v \rightarrow \frac{v}{\left(1 + \left(v^2 / v_{\max}^2\right)\right)^{1/2}}.$$

Considering $v = \mu E = -\mu(q/C_{OX})(\partial n/\partial y)$, the transport equation will be rewritten as

$$\frac{\mu\left(\frac{q}{C_{OX}} n + \frac{kT}{q}\right)\frac{\partial n}{\partial y}}{\left(1 + \left(\frac{q\mu}{C_{OX} v_{\max}}\right)^2 \left(\frac{\partial n}{\partial y}\right)^2\right)^{1/2}} = \frac{I}{q}.$$

This can be integrated analytically by y, and can be used as a transport equation with velocity saturation.

3 SAMMARY

Primary consideration for compact modeling of the double gate (DG) MOSFETs was discussed. We chose the double charge-sheet model as a base model. The carrier partition between two charge-sheets at the source end was solved using one-dimensional Poisson equation. The traversing current between two sheets complicates the model significantly. From the result of the device simulator, it was found that such current really exists. But the current becomes significant only when the gate-voltage asymmetry is strong, or only when one sheet is a dominant current carrier. From this finding, it was concluded that the independent charge-sheet model is the simple and practical model with moderate accuracy.

Conventional charge-sheet model cannot accommodate velocity saturation directly. An alternative formulation which includes the velocity saturation was proposed.

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