Gate Current Partitioning in MOSFET Models for Circuit Simulation

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ABSTRACT

Gate current plays a critical role in circuits featuring sub-100nm MOSFETs. Thus, the importance of an accurate gate current model for circuit simulation is indisputable. As the trend of developing surface-potential-based compact models continues to evolve, we demonstrate that using one such model, HiSIM (Hiroshima STARC IGFET Model), to simulate gate current provides reasonably accurate results in the direct tunneling regime when compared to measurement data. To provide an accurate yet compact description, a gate current partitioning model suitable for circuit simulation is presented and validated by two-dimensional device simulation.

Keywords: gate current, direct tunneling, current partitioning, surface potential.

1 INTRODUCTION

With MOSFET insulator thickness expected to be in the 1.1-1.6nm range by 2003 [1], the significance of direct tunneling becomes more apparent in state-of-the-art technologies. For example, memory devices could be adversely affected in terms of charge storage, and logic device applications could suffer an unintended reduction in drive current. Thus the modeling of direct tunneling including source-drain partitioning in small-geometry devices is imperative for design and optimization of MOS integrated circuits. Although gate current models based on surface-potential exist [2], the calculation of surface potential was based largely on long-channel assumptions.

The consensus in recent publications has been that of three modes of carrier tunneling through the gate insulator in MOS devices, namely, tunneling of electrons from the conduction band, tunneling of electrons from the valence band, and tunneling of holes from the valence band. In this study, we focus on NMOSFET devices, thus we can neglect hole tunneling due to its relatively high effective mass and the large energy barrier necessary to bring it about. According to Cao [3], electron tunneling from the valence band is the dominant mechanism for generating substrate current, thus we can neglect it in this gate current work.

2 MODEL FOUNDATION

The direct tunneling gate current model presented here is based on detailed analyses of surface potential and inversion charge, and on band-to-band generation of carriers. The well-known phenomenon of band-to-band carrier generation allows us to use a closed-form expression for the direct-tunneling current. Inversion charge at the semiconductor-insulator interface is investigated with extensive two-dimensional simulation. Finally, these analyses are combined to form a comprehensive analytical model for MOSFET gate current including drain-source partitioning.

2.1 Surface Potential

Incorporating an accurate description of gate current into a surface-potential-based model requires reasonable accuracy in calculating surface potential with respect to channel position and bias. HiSIM has implemented calculation of the surface potential from an iterative solution based on the two-dimensional Poisson's equation. This formulation provides the user with the surface potentials at both ends of the channel. φ_{SL}, the surface potential at the drain end, can be calculated accurately since the pinch-off position in the channel is determined self-consistently. To illustrate the utility of HiSIM, a simple comparison with a device simulator is given in Figure 1 [4]. Using a self-consistent surface-potential-based compact model provides an inherent advantage of having a continuous description of surface potential in all regions of MOSFET operation. The necessity of calculating φ_{S0} and φ_{SL} accurately will become apparent in Section 3.

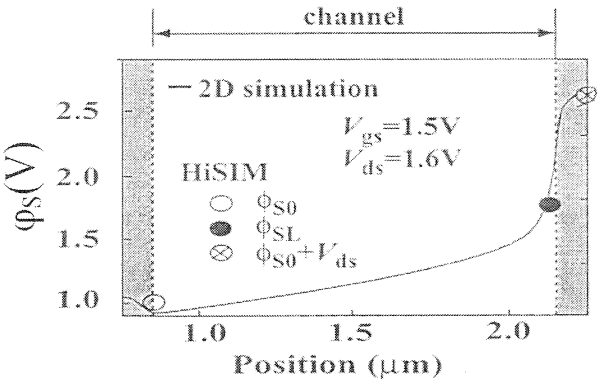

Figure 1. Simulated surface potential along the channel of a MOSFET in saturation with 2-D simulator MEDICI.

2.2 Inversion Charge

A useful way to understand gate current is to examine the inversion charge distribution along the channel. Inversion-layer thickness at low drain bias is one way to characterize the total charge at or near the Si-SiO_2 interface. Thus, we postulate that the probability of direct gate tunneling from a given position in the channel scales as a function of inversion-layer thickness at low drain bias. Figure 3 shows an inversion-layer thickness variation with the total inversion charge obtained from 2-D device simulation. From this behavior, we observe a square-root dependence of inversion-layer thickness on the total inversion charge at low drain bias. Thus we capture the effect of the inversion-layer thickness in our model by including the square root of inversion charge density at low drain bias (Q_i') in the gate current density expression.

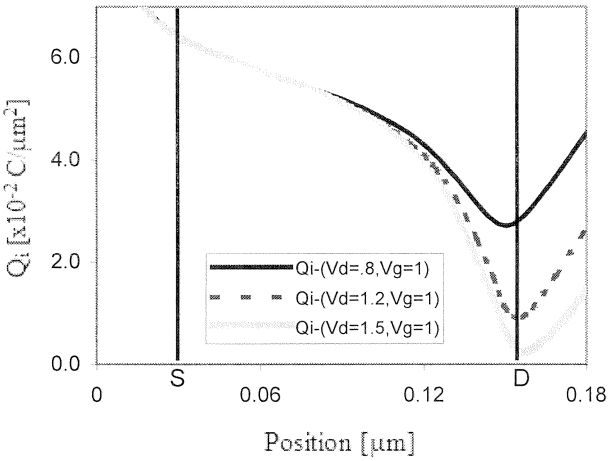

Figure 2. 2-D MINIMOS simulation of inversion charge density distribution along the channel.

2.3 Band-to-Band Generation of Carriers

The direct tunneling model proposed in this work is based on band-to-band generation of carriers at or near the semiconductor surface. Incorporating Kane's model of band-to-band carrier generation [5] in conjunction with inversion-layer thickness dependence, the gate current density, J_G, is expressed as follows.

$$J_G = Aq\bar{x}_C \frac{E_{ox}^2}{E_g^{\frac{1}{2}}} \exp(-B\frac{E_g^{\frac{3}{2}}}{E_{ox}}) \quad (1)$$

$$\bar{x}_C \equiv \sqrt{\frac{Q_i'}{qN_{sub}L_D\sqrt{2}}} \quad (1a)$$

The dependence of the normalized inversion layer thickness $\bar{x}_C$ on Q_i' results from the observed behavior in Figure 3. N_{sub} represents the substrate impurity concentration, L_D the extrinsic Debye length, and E_{ox} the vertical electric field at the substrate-insulator interface. A fitting parameter is used to determine appropriate values for E_{ox} at the source and drain [6]. The V_g dependence of E_{ox} allows effects such as drain-induced barrier lowering (DIBL), polysilicon depletion, and inversion-layer quantization to be modeled as shifts in gate voltage. E_g is the energy bandgap of silicon, while A and B are fitting parameters.

3 MODEL FORMULATION

The qualitative analysis of inversion charge in Section 2.2 leads us to formulate the gate current partitioning model based upon the partitioning scheme for inversion charge [7]. Using similar reasoning, we postulate that the gate current can also be partitioned in this manner since it is a function of carriers at the semiconductor surface. An explanation of the charge-partitioning scheme on which this work is based is described in [6]. The proposed model for the total gate current is derived from integrating J_G over the entire channel cross-section, as follows.

$$I_{G,D} = W\int_0^L \frac{y}{L} J_G dy \ , \ I_{G,S} = W\int_0^L (1-\frac{y}{L}) J_G dy \quad (2)$$

$$I_G = I_{G,S} + I_{G,D} \quad (3)$$

It is assumed that the variation of the gate current density along the channel is approximately linear, which was proposed in [8] and is verified in Figure 4. The linear variation description allows us to express the gate current as an explicit function of surface potentials at the source and drain ends of the channel. Using a change of variables in (2), the surface potentials and gate current densities (1) at both ends can be used to yield the total gate current (3) as a closed-form sum of partitioned source and drain current components. The key to using this approach is the accurate calculation of surface potentials.

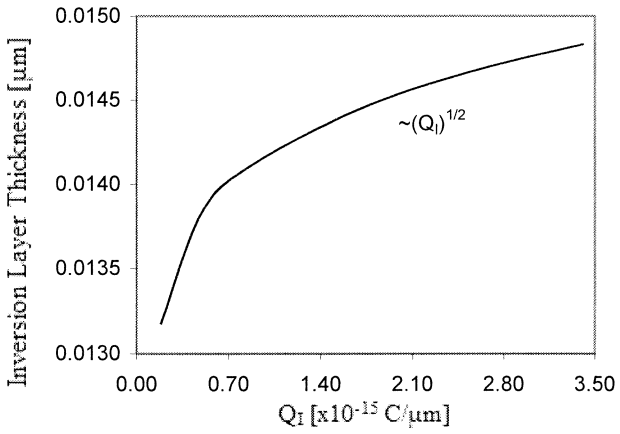

Figure 3. MEDICI simulation of inversion-layer thickness vs. inversion charge at low drain bias: V_d=0.05V, V_g=(0,1V), V_T=0.12V, L=0.5μm.

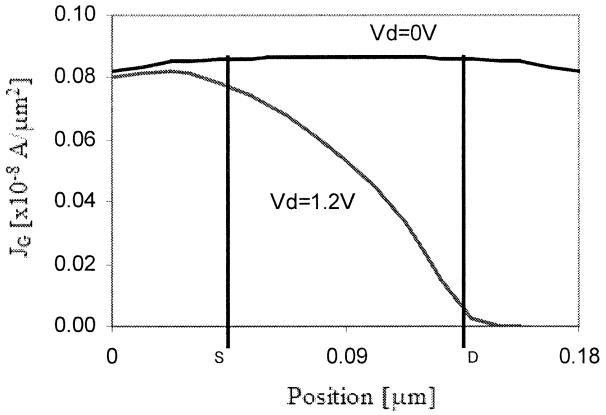

Figure 4. Gate current density calculated using (1) for a 0.18μm device. For this calculation, E_{ox} along the channel is obtained from MEDICI simulation.

4 RESULTS

Implementing equation (1) and carrying out the integrations in (2), we find good agreement with measured data in the direct tunneling regime for t_{ox}=2.48nm, as shown in Figure 5. The results show that our model parameters have no gate length dependence. A universal parameter set is extracted for all gate lengths with other process parameters held constant. Using the approach given by Shih [9], our gate current partitioning scheme is compared with the two-dimensional simulator MEDICI [10]. Figure 6 shows comparisons of results from our gate current partitioning model with those obtained from MEDICI, as well as those obtained from the partitioning scheme of Shih [9].

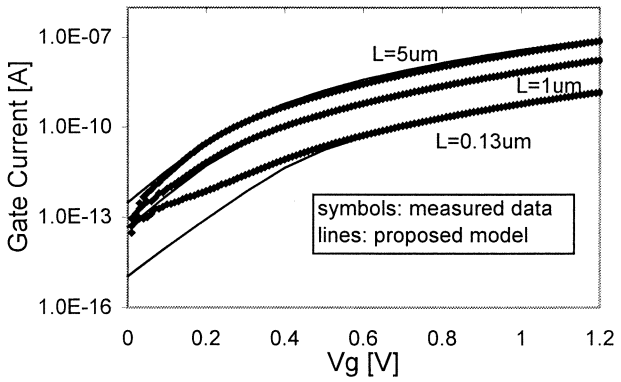

Figure 5. Comparison of model with measurement.

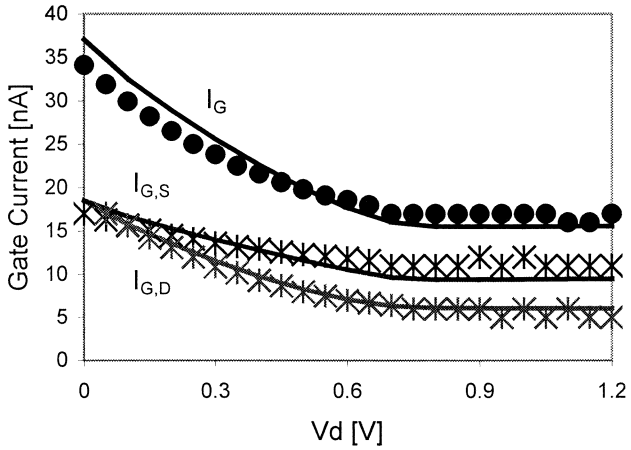

Figure 6. Comparison of our gate current model (solid lines) with MEDICI (circles). Our calculated partitioned currents are compared with those obtained by Shih [9] (asterisks). W/L=10μm/5μm, t_{ox}=2.48nm.

5 CONCLUSION

A model is presented for gate current in the direct tunneling regime, suitable for implementation in a circuit simulator. The model is formulated based on analyses of surface potential and inversion charge, and on band-to-band carrier generation. The inversion charge characteristics allow us to partition the gate current accurately between source and drain. The model is validated by both measurement and two-dimensional device simulation.

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