A Surface-Potential-Based Compact Model of NMOSFET Gate Tunneling Current

X. Gu*, H.Wang*, G. Gildenblat*, G. Workman**, S. Veeraraghavan**, S. Shapira*** and K. Stiles***

*Department of Electrical Engineering, The Pennsylvania State University,
University Park, PA 16802, USA (814) 865-0519 gildenblat@psu.edu
**Motorola DigitalDNA Laboratories, Austin, TX 78721, USA
***Agere Systems, Allentown, PA 18109, USA

ABSTRACT

This work presents a novel compact model for the gate tunneling current in n-channel MOSFET. The model is surface-potential based in both the channel and overlap regions. The Esaki-Tsu formulation is approximated to retain the essential physics without sacrificing the computational efficiency. Four parameters are sufficient to reproduce the bias and geometry dependence of the gate current.

Keywords: MOSFET, compact model, gate current, direct tunneling, current partition.

1 INTRODUCTION

Surface-potential-based approach provides significant advantages in the development of both the intrinsic [1] and extrinsic compact MOSFET models [2]. From the general point of view, it allows one to increase the physics content of the model and by doing so to reduce the total number of adjustable parameters. For example in this work four parameters are sufficient to reproduces complicated bias and geometry dependence of the gate current. The continued aggressive scaling of the gate oxide thickness (T_{ox}) makes the accurate modeling of the gate tunneling current I_g an important aspect of the compact MOSFET model. This work presents a novel compact model of I_g which is valid in all regions of MOSFET operation and is surface-potential based in both the channel and the overlap regions. This approach is made practical by the recently developed analytical approximations for the surface potentials in both the channel [3] and the overlap regions [2]. As shown in Fig. 1 the total gate current is a sum of three components, I_{gsov} and I_{gdov} from the overlap regions and I_{gc} from the channel area. The physics-based description of the overlap regions is particularly important for the scaled devices. Indeed as explained in section 4, the overlap components dominate in the accumulation and depletion regions and remain a significant fraction of I_g in inversion.

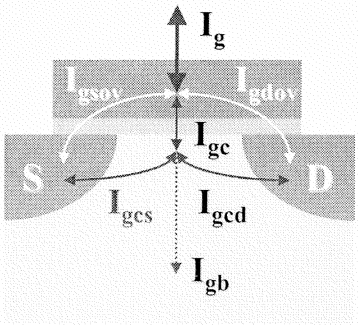

Figure 1: Gate tunneling current components.

2 GATE TUNNELING CURRENT DENSITY

In n-channel MOSFET, it has been shown that the dominant tunneling is between the conduction band in Si and the conduction band in polysilicon gate [5]. The tunneling current density [4]

$$J_g = qm^* k_B T / (2\pi^2 \hbar^3) \int_0^\infty D(E) F(E) dE \qquad (1)$$

where q is the absolute value of the electron charge, m^* is the effective electron mass in the direction perpendicular to the Si/SiO_2 interface, $D(E)$ and $F(E)$ are the transmission coefficient and the supply function as functions of the kinetic energy E in the direction of tunneling, respectively. The numerical integration inherent in (1) does not allow one to incorporate it directly into compact MOSFET models. Consequently in circuit applications it is common to use expressions significantly simpler than (1), which unfortunately do not include the supply function. This often produces some unphysical results which requires empirical fixes. In what follows, we present an alternative approach in which the integral in (1)

is approximated by assigning a single energy $q\psi_t$ (cf. Fig. 2) to all tunneling electrons:

$$J_g \approx qm^* k_B^2 T^2 / (2\pi^2\hbar^3) D(\psi_t) F(\psi_t) \quad (2)$$

In WKB approximation

$$D(\psi_t) = \exp\left\{\frac{2T_{ox}}{\hbar}\sqrt{2qm^*\chi_{Bt}}\left[G_1 + G_2 z_g (1 - G_3 z_g)\right]\right\} \quad (3)$$

where $\chi_{Bt} = \chi_B - \psi_t$, χ_B is the conduction band offset at the Si/SiO_2 interface, $z_g = |V_{ox}|/\chi_{Bt}$, and V_{ox} is the position dependent oxide voltage. The numerical difference between (1) and (2) is absorbed by parameter G_1 which controls the overall tunneling current level. Similarly, the uncertainty in m^* as well as the inaccuracy introduced by the WKB approximation are absorbed in the two remaining dimensionless model parameters, which control the slope (G_2) and curvature (G_3) of the $\log I_g$ vs. V_{gs} characteristics. The fourth parameter is used to adjust ψ_t (cf. Fig. 2). The supply function is given by

$$F(\psi_t) = \ln\left\{\frac{1 + \exp\left[(\phi_s - \phi_n - \alpha_b - \psi_t)/\phi_t\right]}{1 + \exp\left[(\phi_s - V_{gb} - \alpha_b - \psi_t)/\phi_t\right]}\right\} \quad (4)$$

where ϕ_s is the surface potential, ϕ_n is the imref splitting, α_b is the difference between the conduction band edge and the Fermi energy level in the Si bulk, and $\phi_t = k_B T/q$ is the thermal voltage. The gate bias dependence of the supply function is shown in Fig. 2. Note also the physically meaningful result $F(\psi_t) = 0$ and $J_g = 0$ for $V_{gb} = V_{ds} = 0$ (hence $\phi_n = 0$) which obtains without any artificial multiplication factors often required in the some compact models of I_g.

3 GATE CURRENT PARTITION

The same expressions (2)-(4) are used to compute all the three components of the gate current (I_{gc}, I_{gsov} and I_{gdov}) In the overlap contributions, $I_{gsov} = L_{ov} W_{eff} J_g$ and I_{gdov}, the overlap length L_{ov} is extracted from C-V data. As in [6,7], the tunneling current in the channel area

$$I_{gc} = W_{eff} \int_0^{L_{eff}} J_g \mathrm{d}y \quad (5)$$

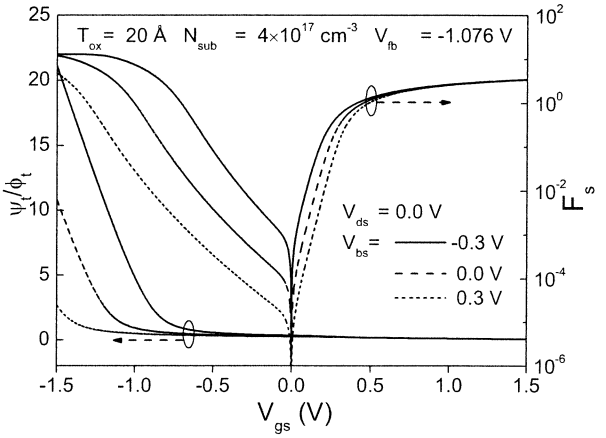

Figure 2: Gate bias dependence of the supply function.

is partitioned into the source and drain components following the theory developed in [6,7], $I_{gcs} = I_{gc} - I_{gcs}$ and

$$I_{gcd} = \left(W_{eff}/L_{eff}\right)\int_0^{L_{eff}} J_g y \mathrm{d}y \quad (6)$$

Using equation [1]

$$\mathrm{d}y/\mathrm{d}\phi_s = L_{eff}(q_i + \alpha_m\phi_t)/[(q_{im} + \alpha_m\phi_t)\phi] \quad (7)$$

the integrals can be evaluated in a closed form to obtain

$$I_{gc} = I_{gc0}\left[(1-b)\sinh(x)/x + b\cosh(x)\right] \quad (8)$$

and

$$I_{gcd} = \frac{I_{gc}}{2} - I_{gc0}\frac{\sinh(x)}{x}\left\{A_g x - B_g\left[\coth(x) - \frac{1}{x}\right]\right\} \quad (9)$$

In (7)-(9), q_{im} is the normalized inversion charge (q_i) at the potential midpoint ϕ_m, α_m is the symmetric linearization coefficient [1], $I_{gc0} = WLJ_g(\phi_m)$, $x = \phi/(2u_0)$, ϕ is the surface potential difference along the channel, $u_0 = 8\chi_{Bt}/\{3[1 + 2z_g(\phi_m)]\}$, $b = u_0/\left(q_{im}/\alpha_m + \phi_t\right)$, $A_g = \left(1 - 3b + 3b^2\right)/2$ and $B_g = b(1-b)/2$. The partition of I_{gc} for different gate biases is illustrated in Fig. 3. In the accumulation region $I_{gcs} = I_{gcd} = 0$, I_{gc} flows into the substrate and becomes a part of substrate current, ($I_{gc} = I_{gb}$ in Fig. 1).

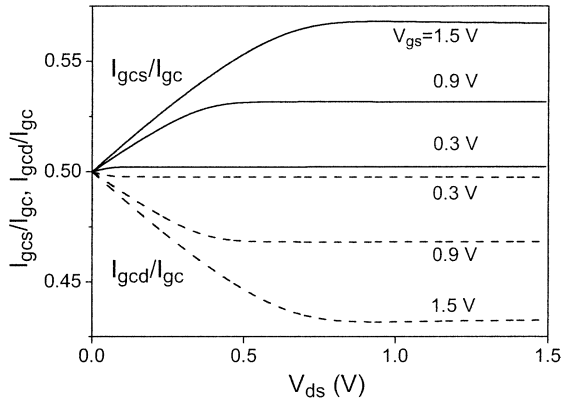

Figure 3: Partition of I_{gc} into source and drain components. Parameters are the same as in Fig. 3.

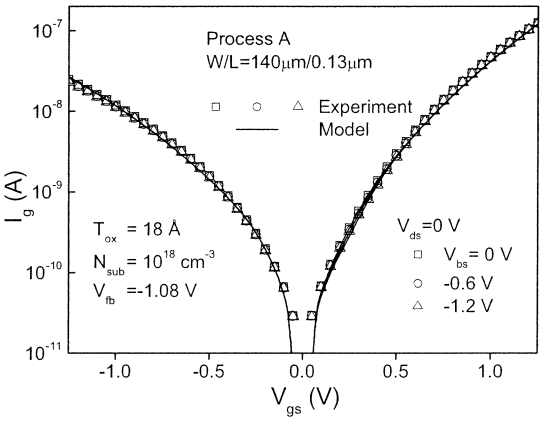

Figure 4: Experimental data for short-channel device by process A (symbols) and model calculations (lines).

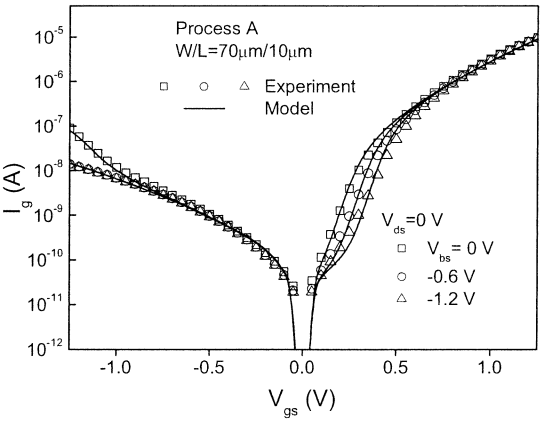

Figure 5: Experimental data for long-channel device by process A (symbols) and model calculations (lines).

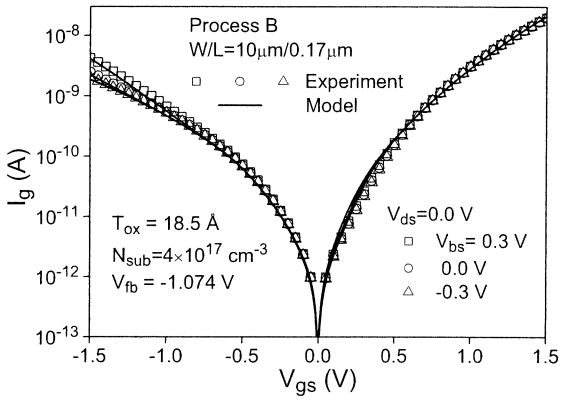

Figure 6: Experimental data for short-channel device by process B (symbols) and model calculations (lines).

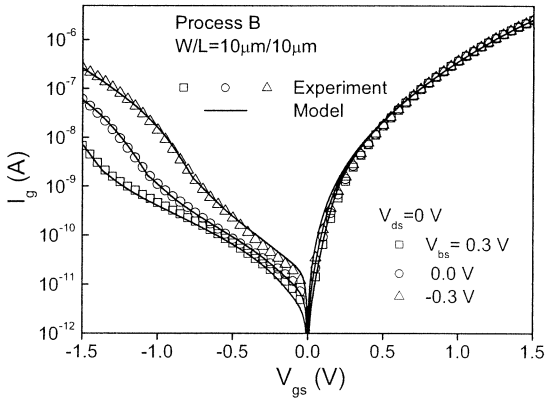

Figure 7: Experimental data for long-channel device by process B (symbols) and model calculations (lines).

4 RESULTS AND DISCUSSIONS

The accuracy of the new gate tunneling current model has been verified using experimental data for two advanced processes denoted as A and B. Typical results for $V_{ds} = 0$ are shown in Figs. 4-7. The back bias dependence for I_g of the long-channel devices is stronger than that of the short-channel devices, in which the contribution of the overlap regions is significant for all V_{gs}. This is illustrated in Figs. 8 and 9, where I_g is decomposed into the contributions of the channel and overlap areas. In the inversion region of the long channel devices I_{gc} dominates and the back bias effect of I_g is significant. However, for short-channel devices, $I_{gsov} + I_{gdov} \gg I_{gc}$ in the depletion region, and, since $I_{gsov} + I_{gdov}$ is not affected by V_{bs}, neither is I_g. The drain bias dependence of I_g is

presented in Fig. 10. There are two physical mechanisms responsible for $I_g(V_{ds})$ dependence. The gate current in the drain overlap region I_{gdov} is dependent on V_{ds}. Furthermore, the current in the channel area I_{gc} is also dependent on V_{ds} since V_{ds} controls the position dependence of the imref along the channel, which makes I_{gc} a decreasing function of V_{ds}. No scaling parameters are necessary to provide an accurate fit for devices with different geometries.

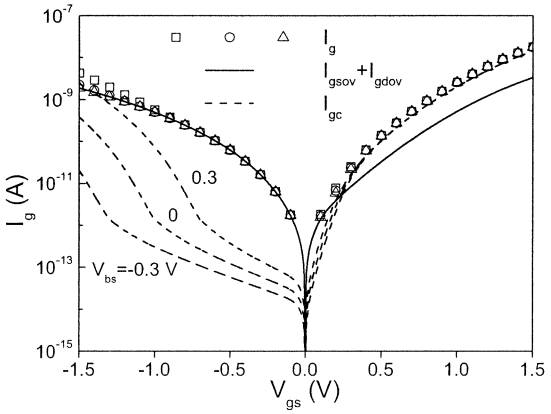

Figure 8: Decomposition of the total gate current into I_{gc} and $I_{gsov} + I_{gdov}$ for the data shown in Fig. 6.

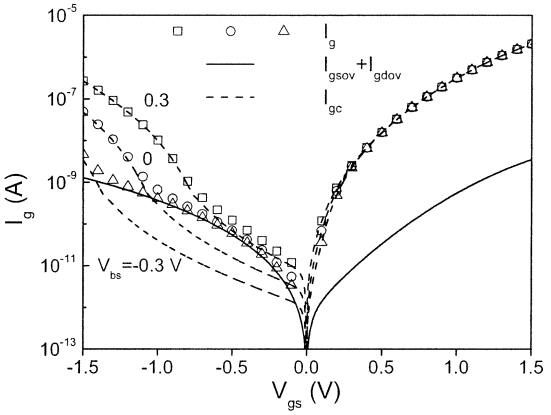

Figure 9: Decomposition of the total gate current into I_{gc} and $I_{gsov} + I_{gdov}$ for the data shown in Fig. 7.

5 CONCLUSIONS

The new I_g model presented here is a part of a recently developed surface-potential-based compact MOSFET model (SP). However, it can be included in any other MOSFET model where the surface potential in available. The increased physical content of the proposed model leads to high accuracy and physically meaningful results with a small number of adjustable parameters. Using symmetric linearization method, asymptotically correct partition of I_g into source and drain components is achieved in a closed form valid in all regions of operation.

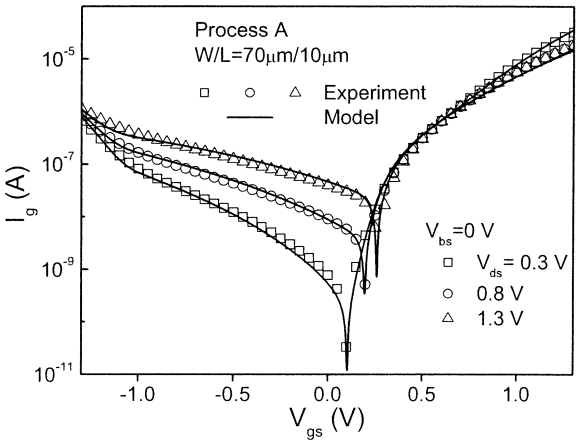

Figure 10: Experimental data for long-channel device by process A (symbols) and model calculations (lines) for different drain biases with Vbs=0 V.

Acknowledgement: This work is supported in part by Semiconductor Research Corporation (contract no. 2000-NJ-763). We are grateful to P. Bendix, C. McAndrew, K.R. Barry T-L. Chen, and X. Cai for their help with various aspects of the model development.

REFERENCES

[1] T-L. Chen and G. Gildenblat, ICMSM, 2002, p.657
[2] X. Gu, G. Gildenblat, G. Workman, S. Veeraraghavan, S. Shapira, K. Stiles, ICMSM 2003, in Press
[3] T-L. Chen and G. Gildenblat, Solid-State-Electronics, **45**, 335 (2001)
[4] R. Tsu and L. Esaki, Appl. Phys. Lett. **22**, 562 (1973).
[5] W-C. Lee and C. Hu, VLSI Symp., 2000. p.20.3
[6] R. van Langevelde, A.J. Scholten, R. Duffy, F.N. Cubaynes, M.J. Knitel, and D.B.M. Klaassen, IEDM Tech. Digest, 2001, p.13.2.1
[7] W-K. Shih, R. Rios, P. Packan, K. Mistry and T. Abbot, IEDM Tech. Digest, 2001, p.13.3.1