Clocked Quantum-dot Cellular Automata circuits

Ravi Kummamuru, Alexei O. Orlov, Craig S. Lent, Gary H. Bernstein, and Gregory L. Snider.

University of Notre Dame, Dept. of Electrical Engineering, B-31 Fitzpatrick Notre Dame, IN 46556, kummamuru.1@nd.edu

ABSTRACT

We present an experimental demonstration of clocked Quantum-dot Cellular Automata (QCA) circuits, where information is represented by spatial configurations of single electrons within geometrical arrangements of submicron-sized metal dots. We demonstrate the functional operation of these circuits and use a two-stage shift register to mimic the operation a multi-stage shift register.

Keywords: Coulomb blockade, single-electron tunneling, Quantum-dot Cellular Automata.

1 INTRODUCTION

The rapid pace of improvement in production and complexity of integrated circuits (ICs) in the past four decades has become possible due to the success in downscaling of the active elements of ICs - the field-effect transistors (FET). So far, the performance of FETs has steadily improved inspite of severe size reductions, but we are reaching the limits below which undesirable fundamental effects will make further scaling extremely difficult. Deleterious short channel effects and increased device density lead to intolerable levels of power dissipation per unit area.

Therefore, the search for alternative ways to perform binary operations with minimal achievable power dissipation becomes imperative. The alternate paradigm must be compatible with the inherent properties of nanostructures as it should exploit the effects that accompany small sizes rather than battling against them.

The ultra-low power dissipation using nanostructures for binary operations can be achieved in QCA [1], where the geometrically arranged arrays of coupled quantum dots are used to encode and process binary information. Logic levels are represented by the configurations of single electrons in these arrays. A typical QCA cell consists of four dots located at the vertices of a square. When a cell is charged with two excess electrons, they occupy diagonal sites due to mutual electrostatic repulsion. The two diagonal electron arrangements are energetically equivalent to each other and are the ground states of the cell. Since binary logic operations in QCA are performed by manipulation of the spatial configurations of single electrons, the power dissipation in such a system is greatly reduced compared to conventional, FET-based logic.

2 CLOCKING IN NANOSTRUCTURES

Cyclical manipulation of quantum wells for binary operations was first considered by Keyes and Landauer [2]. A particle in a time-varying potential represents a binary “0” or “1” by its position in the well (Fig. 1). At the initial phase, RESTORE, the system is in a monostable ground state. During the SWITCH phase, first the input potential is applied, biasing the well, and then the system is converted from a monostable to a bistable state by altering the potential profile of the well. This work is done by means of an external energy source - the clock. The particular binary state (corresponding to a particle in the left or right well in Fig.1) is selected by the external input, which creates an asymmetry in the emerging double-well and thus forces the particle to choose either the left or right well. The magnitude of the input signal is small, so that the particle cannot be moved by the input signal alone. By the end of the SWITCH phase, binary information is stored in the system. During the HOLD stage the barrier of the bistable well is raised high so that information is preserved, and the particle in the well acts as an input for the subsequent stage (e.g. by means of Coulomb interaction). Finally, the system is returned to its initial, monostable state, and is ready to receive a new input.

This approach was used by Lent et al. [3] to propose clocked QCA circuits where the barriers between quantum

![Figure 1. Keyes-Landauer clocking scheme. (E - energy, X- coordinate). Black circle represents particle in the potential profile. Binary 1(0) is defined when particle is confined in the left (right) well.](image-url)
dots are electrostatically modulated. The important advantage of clocked QCA architecture is its inherent ability to realize digital latches (STORE phase in Fig. 1). As a result, the locked electron provides a firm input signal for the next cell. Latches could be used to break a large QCA array into sub-arrays with each sub-array working on different parts of a computational problem (pipelining). It is important to note that the primary source of energy in clocked QCA is the clock, just as the power supply in conventional electronic circuits. Clocked QCA exhibits power gain needed for logic level restoration [4] since a weak input can be boosted using the power supplied by clock.

The application of the above clocking scheme for the classical Coulomb blockade system with tunnel barriers was theoretically discussed in [5,6]. The variable barrier in this case is formed by an extra well with adjustable energy minimum, placed between the two end wells in Fig. 1. The three operational modes, are defined by the combination of input and clock biases. The operation of this elementary building block, a QCA latch, was experimentally demonstrated in [7].

2 FABRICATION

The fabrication of QCA arrays could be accomplished in a number of ways. While the goal of making QCA devices work at room temperature could be achieved using molecular implementations, the technology to fabricate molecular QCA arrays is not yet available. However, it is possible to build working prototypes to verify the concepts using any system exhibiting Coulomb blockade [8] in electron transport between dots forming the cells.

To demonstrate clocked QCA devices we use the well established aluminum tunnel junction (TJ) technology which combines direct E-beam lithography with suspended mask technique [9]. In this way we fabricate thin-film aluminum dots, separated by tunnel junctions, on an oxidized silicon substrate. This method of QCA fabrication requires only 3 major processing steps: direct E-beam writing, development, and metal deposition with in situ oxidation. To detect charging in cells, single-electron transistors (SET) are used as capacitively coupled electrometers [10]. Since aluminum dots produced by the metal TJ process have small charging energy (EC ~ 1 meV), the operational temperature is limited to below 4K. Therefore the measurements are performed in the dilution refrigerator with a base temperature of about 15 mK. To suppress the superconductivity of aluminum, a magnetic field of 1T is applied to the sample.

It is important to point out a major advantage of the QCA paradigm compared with conventional FET-based logic - the improvement in performance as the device sizes shrink. As appropriate technologies become available, it should be possible to make complex QCA arrays operating at room temperature with much better performance in speed and reliability than existing metal TJ prototypes.

3 EXPERIMENT AND DISCUSSION

3.1 Operation of a QCA two stage shift register - information storage and processing

Information in clocked QCA is processed and stored using shift registers comprised of capacitively coupled latches [7]. The simplest, two stage, QCA shift register (SR) consists of only two latches. The circuit diagram of the device is shown in Fig. 2, and an SEM micrograph is shown in Fig. 3. Each QCA latch (L1 and L2) consists of three metal dots separated by multiple tunnel junctions to suppress cotunneling [11]; latches are coupled capacitively. SET electrometer E1 (E2) provide the readout of L1 (L2). The state of SR is controlled using two phase-shifted clock signals (CLK1 and CLK2).

![Figure 2. Circuit diagram of a QCA two-stage SR.](image)

The operation of the two-stage SR in the time domain is shown in Fig. 4. First, the differential signal V_{IN} corresponding to logical “0” (logical “1”) is applied to the inputs V_{IN}^+, and V_{IN}^- at t_1 (t_7) (Fig. 4A). L1 remains in the monostable null state until CLK1 is set HIGH at t_2 (t_8) (Fig. 5B). When CLK1 is activated, it causes a transition of an electron in L1 (Fig. 4C). After that the input signal is removed at t_3 (t_9) and the state of L1 no longer depends on the input signal. Then CLK2 is applied to L2 at t_4 (t_{10}) (Fig. 4D), and an electron in L2 switches in the direction determined by the state of L1 (Fig. 4E). L2 holds the bit after CLK1 is removed at t_5 (t_{11}) for as long as CLK2 is high (until t_6 (t_{12})). The cycle describing the operation of a QCA SR is as follows: monostable → input applied → CLK1 applied and L1 is active → input removed → CLK2 applied and L2 is active → CLK1 is removed. At this time,
L1 becomes inactive and is ready to receive new information. The information encoded in the position of a single electron is shifted to L2 and stored there. Thus, the QCA SR operation in accordance with theories [5,6] is successfully demonstrated.

One of the most important parameters which determine the success of any logic device is the speed of switching for binary operation. The operational speed of the SR stage is determined primarily by the tunneling time of an electron ($\tau \sim R_i C_j \sim 10^{-10}$ s, where $R_i \sim 10^6 \\Omega$, and $C_j \sim 10^{-16}$ F are the resistance and the capacitance of the junction, respectively). Thus, for the current Al/AlOx QCA prototype, the estimate for the switching “speed limit” is on the order of 1 ns. For future molecular implementations due to much smaller total capacitance ($C \sim 10^{-19}$ F) the expected switching speed is on the order of ps.

### 3.2. Multi-stage SR operation

In large-scale QCA circuits, multi-staged SRs will be used to control the flow of binary information through the circuit. There, a bit is first written into the circuit by the input and then moved along the circuit using each latch as an input to the next (Fig. 5A). The same situation can be simulated using the two-stage SR by moving the bit back and forth from one latch to the other (Fig. 5B). Initially, a bit is written into the first latch by the input. Then, using L1 as input, the bit is copied into L2 after which L1 is turned off. Then using L2 as input, the bit is copied back into L1, and L2 is turned off. This process can be repeated a number of times to achieve the same effect as transferring a bit through a long line of latches.

Figure 6 shows the timing diagram of the experiment performed for 5 clock cycles. Initially, all the signals are zero and both L1 and L2 are in the neutral state. Once CLK1 is set HIGH, L1 switches into the state defined by the input (binary “1”). The input is then removed and the bit is stored in L1. The clock signal is then applied to L2, and it switches using L1 as its input. L1 is then switched off, and the bit is now stored in L2. Instead of applying the clock signal to a third latch in the line, it is applied to L1 which sees L2 as an input and

Figure 5. Simulation of a multi-stage SR. (A) In a multi-stage SR, a bit is moved sequentially in a single direction from one latch to the next. (B) The two-stage SR can be used to simulate a longer SR by moving the bit back and forth from one latch to the other.
switches accordingly. Then L2 is switched off and the bit is stored once again in L1. This cycle is repeated 5 times to simulate an SR made of 11 latches. In the second half of the experiment, this scheme is repeated with an input of the opposite sign (binary “0”) to verify that bit inversion at the input indeed leads to the bit inversion at the output. The above experiment demonstrates that the direction of the information flow in the circuit is controlled by the sequence of clock signals applied to latches. No degradation in the signal observed as the bit is moved back and forth between the latches, indicating that signal levels would be preserved in multi-stage QCA SRs. The major reason for this stems from the ability of clocked QCA to exhibit power gain [4].

4 CONCLUSIONS

The experiments so far showed the feasibility of the QCA architecture, demonstrating functional cells, logic gates [12,13], and latches [7]. Future research includes the search for possible QCA cell candidates using metal nanoclusters and molecular complexes, interfacing and assembling of QCA devices. This is headed towards significantly higher operating temperatures. Another important field of experimental QCA research lies in the area of the high-speed QCA studies.

This allows the determination of the limiting parameters for QCA switching, and thus opens the door to the real-world application of nanostructures to computation and signal processing. Once this is achieved, real QCA applications can be contemplated that employ nanoscale size devices for logic and computation.

ACKNOWLEDGEMENTS

This research was supported in part by the W. M. Keck foundation, DARPA, Intel and NSF. We wish to thank W. Porod and A. N. Korotkov (UC Riverside) for helpful discussions.

REFERENCES