Compact Modeling for RF and Microwave Integrated Circuits

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ABSTRACT

Compact modeling has been an integral part of the design of integrated circuits for digital and analog applications. The availability of scalable CMOS device models has enabled rapid simulation and design of present and future device technologies. Increasingly RF and microwave circuits designed with CMOS and SiGe technologies obviate the need for compact modeling in this domain. In this paper we will summarize the unique requirements of high-frequency compact modeling efforts by focusing on key components, such as passive devices, interconnect, substrate coupling, and active devices.

Keywords: RF and microwave compact modeling, passive device modeling, interconnect modeling, substrate coupling.

1 INTRODUCTION

Compact modeling for RF and microwave devices is a key enabling technology for low cost mass-producible wireless communication devices. Traditionally, RF and microwave wireless circuits and devices were fabricated in small quantities targeting military or space communication applications. This enabled manual post fabrication measurement and tuning. Furthermore, such systems were not integrated and many separate components could be easily measured and characterized in building a larger system. Today we build entire radios on a single chip with minimal external circuitry targeting the mass consumer market. To keep costs low, the chips should work without any post-fabrication tuning. To achieve this goal, much work is needed in the modeling of passive and active elements at frequencies exceeding several GHz.

2 PASSIVE DEVICES

The paramount philosophy in designing analog circuits is to use the transistor as much as possible to avoid using passive devices. Passive devices realized on-chip, such as resistors and capacitors, are physically large and of comparatively low quality. Therefore circuit designers favored active loads and active current mirrors to minimize chip area and to maximize the reliability of the circuit. RF and microwave circuits, though, are critically dependent on passive devices. Passive devices such as inductors, capacitors, transmission lines, and transformers allow more optimal circuit blocks such as low-noise amplifiers and high-dynamic range filters. The realization of other circuit blocks, such as the voltage-controlled oscillators, is impossible without inductors and varactors. At low frequencies, external components can be used, but due to package and bond-wire parasitics, there is an upper limit on the frequency at which these components can be placed off-chip. Furthermore, the stray coupling due to bond-wires, package pins, and board parasitics, can lead to undesirable spurs in noise sensitive circuits.

For these reasons passive devices can no longer be ignored and much work has gone into understanding the physics and manufacturing capabilities in integrating these components.

2.1 Inductors and Transformers

RF inductors and transformers are typically realized as planar spirals, although many variations are possible for creating symmetric structures useful for differential circuits and baluns. In the quest to minimize the series resistive losses of the device, designers and device engineers have employed 3D layouts by either connecting multiple metal layers in parallel to minimize resistance with a slight hit in inductance (due to non-unity coupling factor) or in series in order to boost the inductance value. Due to the various options in device layout, it is difficult to analytically predict device behavior with compact equations, even DC inductance. Additionally, at high frequency skin effect and proximity effects in addition to electrically induced substrate losses further complicate the device behavior. For conducting substrates or at high frequencies, the skin-effect equation must also be solved in order to predict magnetically induced reflected inductance and bulk eddy current losses [1]. Additionally, the electrically-induced substrate losses are a strong function of contact placement and/or shielding [2].

Despite these difficulties, some work in the compact modeling of inductors and transformers has been done [3] [4] [5]. In reality, a more important issue for compact modeling of inductors and transformers is not to pre-

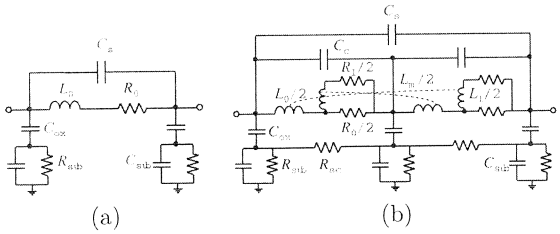

Figure 1: (a) A simple Π equivalent circuit model of an inductor with substrate parasitics and interwinding capacitance. (b) 2-Π model with skin and proximity effect loss modeling.

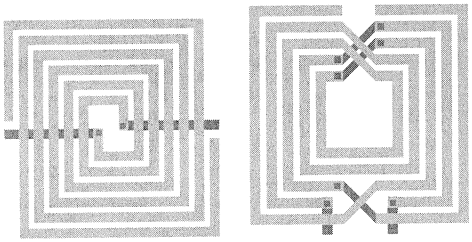

Figure 2: (a) The layout of a simple planar transformer. (b) The layout of a balun with symmetric center tap points.

dict electrical behavior but to model electrical behavior over a wide frequency range with a simple equivalent circuit model. The simple Π model shown in Fig. 1a has been a popular approach, with modifications to model substrate losses and dielectric relaxation. This model fails to capture the effects of non-uniform current flow in the metalization due to skin and proximity effects. A frequency-dependent resistor only works for AC analysis. A modified 2-Π model [5] shown in Fig. 1b is a good way to capture this effect for both transient SPICE simulation and AC simulation. The 2-Π section additionally models the distributed characteristics at high frequency.

Transformers are modeled in an analogous fashion, since most transformer structures consist of two inductors in close proximity, as shown in Fig. 2a. Other topologies are possible, such as symmetric baluns shown in Fig. 2b. An important difference is the interwinding capacitance. In an inductor, the interwinding capacitance plays a minor role whereas for a transformer capacitive coupling perturbs the phase balance.

2.2 Capacitors and Varactors

Capacitors have played an important role in analog and RF circuits. Poly caps and MOS capacitors have been fairly standard and well-modeled, whereas (metal-insulator-metal) MIM caps are usually optional in most silicon processes. MIM devices offer high density linear high-quality capacitor by employing metal and/or poly, and a thin dielectric. MIM capacitors can also be realized as interdigitated finger capacitors. These capacitors are fairly dense due to lithographic dimensions of metal layers.

The quality factor of a MIM capacitor is crucial to model correctly. Back-plate parasitics are an important consideration, especially the substrate losses of an unshielded capacitor. A circuit designer can shield the capacitor to prevent substrate injection and losses but at the penalty of higher back-side parasitics. For an unshielded structure, a simple resistor in series with the back-plate capacitance can model substrate losses fairly well. Scaling this resistor is not trivial since the substrate current path is a function of substrate contact placement and substrate profile. At low frequencies, for instance, a back-side package ground is an effective connection for substrate currents. At high frequencies, or for an insulating back-side contact, most of the currents are constrained to exit through the substrate contacts near the device.

At high frequency it is important to properly model the distributed effects of the parallel plate capacitor. The impedance to ground is given by

$$Z = \sqrt{\frac{R}{j\omega C}} \coth\left(\sqrt{j\omega RC}\right) \qquad (1)$$

where C is the total capacitance of the plates, R is the resistance of the top and bottom plate in series, and ω is the excitation frequency, assumed harmonic. The above formula assumes negligible inductance in the device and a one-dimensional profile similar to a transmission line. For a high-quality device, this simplifies to the familiar expression $R/3 + \frac{1}{j\omega C}$. Fortunately, the high-Q loss can be modeled by a frequency-independent resistor.

Varactors and MOS capacitors are also important elements used in RF and microwave circuits. The varactor is often a reverse-biased junction diode. Substrate parasitics and accurate noise models are an important addition for high-frequency circuits. MOS capacitors, on the other hand, can be modeled through the active device equations and we will defer discussion to section 5.

2.3 Transmission Lines

Transmission lines are used as key building blocks in microwave circuits, as they can play the role of inductors, capacitors, impedance matching networks, and other circuitry realized as lumped elements in the RF frequency range. Transmission lines of appreciable electrical length are too large to realize on-chip at RF and analog frequencies and typically only appear in microwave circuits.

Microwave transmission lines are generally realized using microstrip or coplanar varieties, although many

other variations are possible. The dominant mode for signal transmission is usually quasi-TEM mode. It is inadvisable to use the substrate as the return path. For highly resistive substrates, a back-side ground can in principal act as the return path of a TEM-mode transmission line where the substrate would serve as a lossy dielectric [6]. For moderately conductive substrates, though, the return current would in fact flow in the substrate and the losses would be prohibitively high. Instead, both the microstrip and the coplanar line support return currents near the conductor to minimize losses.

Due to the distribution nature of the structure, the transmission line is difficult to model in transient simulation ODE solvers such as SPICE. They can be handled easily in the frequency domain and thus fit nicely into harmonic balance simulation tools. Electrically short transmission lines can be modeled as cascaded Π sections as a discrete approximation to the Telegrapher's equation. This approach can model the attenuation constant due to dielectric and ohmic losses. The loss mechanisms of transmission lines are similar to those already discussed in section 2.1. In this regard the microstrip line has the added advantage of self-shielding since the capacitive substrate losses are not excited if the return current is kept at zero potential and the fringing fields of the top conductor terminate mostly on the bottom conductor. On the other hand, the coplanar line is unshielded but may result in lower magnetically induced losses if the gap spacing is smaller than the distance to substrate.

2.4 Resistors

Most IC resistor structures can be modeled as distributed RC lines, similar to the MIM capacitor. The parasitic capacitance stems from the coupling to the substrate for a thin-film or poly resistor or it is due to the depletion capacitance of a diffusion resistor. MOS transistors biased in triode also act as bias-dependent resistors. In theory an accurate MOS device compact model can handle this case but care needs to be exercised to properly handle non-quasistatic effects.

3 INTERCONNECT

RC interconnect extraction is a standard component in the design flow of high-performance digital and analog ICs. The RC parasitics are usually computed in a heuristic fashion, avoiding the 3D solution of Poisson's equation. A key missing ingredient in the extraction process is the absence of inductance modeling and proper accounting for losses. Inductance extraction is difficult since the "return path" is often not known. For example, consider an inverter shown Fig. 3 driving a distant inverter. Since the drive is single-ended, the return path is not known. In fact, there are myriad

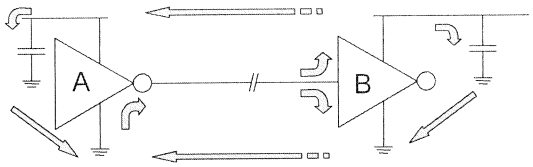

Figure 3: An inverter driving a distant inverter through a signal line has a complicated return path involving the ground and supply tree as well as the substrate and off-chip paths.

paths from the ground at inverter B to the ground at inverter A. The current will flow through the path of least impedance and so the contribution of the return current at low frequency will be different from high frequency. The presence of a conductive substrate further complicates the situation. For a digital circuit clocked at several GHz, this inductance can affect the rise-time of the signal arriving at B. For an RF and microwave circuit, this inductance can de-tune critical components such as tanks.

Losses in interconnect are also important to model properly. As discussed in section 2.1, the losses arise due to skin and proximity effects, as well as magnetically induced eddy-current losses. Electrically induced substrate losses are important as well and will be discussed in section 4.

Signal coupling through interconnect is another important issue. While lossless capacitance coupling is captured by today's IC extraction tools, the actual coupling between lines has two components, coupling through the SiO_2 and coupling through the lossy substrate. Analytic formulations of Poisson's equations can compute these coupling terms in a frequency-dependent matter [7].

Inductive coupling is not currently extracted by commercial tools. Due to the absence of magnetic monopoles, such coupling can be long range (as opposed to short range capacitive coupling) and difficult to trace. In a mixed signal environment, such inductive coupling can give rise to many unwanted effects such as frequency spurs in synthesizers, LO leakage and isolation issues, and general stability issues with amplifiers. Today the practical solution is to isolate and shield as much as possible, yielding non-optimal density and excessive design time.

4 SUBSTRATE COUPLING

Substrate coupling occurs as a result of the conductive nature of silicon and the lack of perfect isolation between devices and the substrate. Most devices are only isolated capacitively from the substrate. At high frequency, therefore, signals are injected and received by devices through the conductive substrate [8]. The trends of single chip integration pose serious challenges

as noisy digital circuits are placed on the same substrate as sensitive analog circuitry.

As discussed in previous sections, in the compact modeling of passive and active devices, care must be taken to include the losses due to the substrate. The coupling, though, is very difficult to properly model due to the layout dependence and sheer magnitude of the problem size. Semi-analytic approaches have been proposed [8] [9] [10] and commercial tools are available to extract substrate parasitics, although the process is time-consuming.

A further complication is that many passive devices already contain some substrate parasitics and extracting these parasitics double counts the loss component. One solution is to only use the built-in compact model substrate resistance value during the schematic phase of the design (pre-layout) and terminate these resistors to ground, thus ignoring the coupling. Post-layout the resistors can be replaced by the extracted values that include the coupling terms.

5 ACTIVE DEVICES

At lower microwave frequencies, the CMOS MOSFET, Si BJT, and SiGe HBT are important devices, having almost entirely displaced other technologies with the exception of niche markets (such as power amplifiers). The SOI MOSFET is also an important device with significant applications in radiation hard environments. Starting with BSIM version 4, many high frequency effects are modeled in the core and extrinsic transistor, such as the gate-induced resistance of the channel as well as the distributed resistance of the poly, the substrate resistance network, the non-quasi-static AC model, and the holistic noise model. These improvements were a large step in the compact modeling of RF effects in transistors.

Ultra-short channel length devices, though, bring new issues to the table. Enhanced noise models are needed to accurately model flicker noise due to new dielectric materials and excess noise stemming from non-equilibrium thermal conditions in the channel.

While devices for analog circuits are typically characterized by the unity current-gain frequency f_T, the maximum frequency of oscillation, f_{max}, is a much more important parameter in RF and microwave circuits. f_{max} is a strong function of device geometry and device parasitics, and can be estimated by

$$f_{max} \approx \frac{f_T}{2\sqrt{R_g\left(g_m C_{gd}/C_{gg}\right) + \left(R_g + r_{ch} + R_s\right) g_{ds}}} \tag{2}$$

It is interesting to note that the effect of gate resistance on f_{max} can be reduced by scaling the width of the transistor W through a multi-finger layout. The drain and source resistances, though, do not scale and pose as challenge for next-generation technologies. A compact high frequency model for the FET must therefore be capable of predicting these losses and capacitances over bias and temperature in a smooth and accurate fashion.

When FETs are used as capacitors, the accuracy of the CV-curve is important, especially the change with temperature. Voltage-controlled oscillators use MOS capacitors as varactors and large amplitude signal swings across the capacitor can exercise the entire range of capacitance from accumulation, sub-threshold, to moderate and strong inversion. An accurate model in the entire region is necessary to accurately predict phase noise and distortion in a voltage-controlled oscillator.

6 CONCLUSION

In this paper we have highlighted important issues unique to the compact modeling of devices at microwave and RF frequencies. Transistors require extra care to properly account for non-quasistatic effects, losses, and excess noise. Single chip integration necessitates careful modeling of coupling and isolation through the substrate, interconnect, and package.

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