A Physics-Based Compact Model for Nano-Scale DG and FD/SOI MOSFETs

Jerry G. Fossum, Lixin Ge, and Meng-Hsueh Chiang
University of Florida
Gainesville, FL 32611-6130, U.S.A.

ABSTRACT

A process/physics-based compact model (UFDG) for double-gate (DG) MOSFETs is overviewed. The model, in essence, is a compact Poisson-Schrödinger solver, including accountings for short-channel effects, and is applicable to nano-scale fully depleted (FD) SOI MOSFETs as well as generic DG devices in ultra-thin Si films. The utility of UFDG is demonstrated by using it in Spice3 to design and characterize thin Si-film MOSFETs and to project extremely scaled DG and FD/SOI CMOS performances.

Keywords: Compact model, predictive circuit simulation, nano-scale CMOS, DG MOSFET, FD/SOI MOSFET.

1. INTRODUCTION

Interest in DG and FD/SOI MOSFETs is growing now because of the palpable scaling limit (L_{gate} ~ 50nm) of bulk-Si and (partially depleted) PD/SOI CMOS. DG MOSFETs can potentially be scaled to the end of the SIA ITRS [1], where L_{gate} ~ 10nm, because short-channel effects (SCEs) are suppressed via the thin Si-film channel, rather than by extreme channel doping densities and profiles. For the same reason, conventional FD/SOI MOSFETs, with a single (front) gate and a thick underlying (back) oxide (BOX), which are much easier to fabricate, can be scaled to L_{gate} < 50nm, but with limits subject to the pragmatic thickness of the Si film (t_{Si}). In order to effectively design nano-scale DG and FD/SOI CMOS, as well as assess performance potentials, a truly physics-based compact model for circuit simulation is needed. In this paper, we overview such a model, UFDG [2]-[4], and we demonstrate its utility via predictive device and circuit simulations.

2. THE UFDG MODEL

The UFDG model is based on the generic DG device structure shown in Fig. 1. Although Gf is assumed to be the predominate gate in the formalism, the model can be applied to DG MOSFETs having symmetrical or asymmetrical gates [5], or to the single-gate FD/SOI MOSFET [6] with thick BOX (t_{oxb} >> t_{oxf}). To allow truly physical modeling of the intrinsic MOSFET, the formalisms for weak (V_{GfS} < V_{TW}) and strong (V_{GfS} > V_{TS}) inversion are separated, with moderate-inversion channel current and terminal charges, and their voltage-derivatives, being continuously defined by spline functions based on solutions at the bias-dependent boundaries V_{TW} and V_{TS} [3].

In addition to the SCEs, UFDG physically accounts for (a) the carrier-energy quantization in the thin Si-film channel, (b)

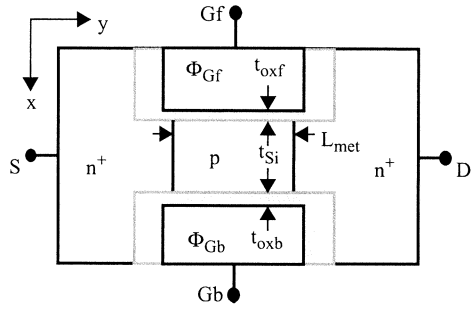

Fig. 1. DG nMOSFET structure. For an asymmetrical design, the gate work functions (Φ_{Gf}, Φ_{Gb}) and/or oxide thicknesses (t_{oxf}, t_{oxb}) are unequal; for an FD/SOI device, t_{oxb} >> t_{oxf}. Note that L_{eff} is not necessarily equal to the metallurgical channel length L_{met} due to the S/D doping-density gradient in y.

the quasi-ballistic (or ballistic) carrier transport along the channel, (c) the associated terminal charges (for transient and AC simulations), and (d) the unavoidable parasitics. For weak inversion, Poisson's equation in the 2D (n-)channel region,

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} \cong \frac{qN_{CH}}{\varepsilon_{Si}} \qquad (1)$$

where N_{CH} is the doping density, is first solved by assuming a second-order polynomial function in x for the electric potential $\phi(x, y)$ and using the (four) bias (V_{GfS}, V_{GbS}, and V_{DS})-dependent boundary conditions to evaluate the y-dependent coefficients [7]. The quantization is then accounted for by increasing this classical solution for ϕ by a $\Delta\phi_{QM}$, derived from the 1D (in x) Schrödinger equation and dependent on t_{Si}, N_{CH}, and the transverse electric field (ε_x) [3]. The weak-inversion current, assumed to be predominantly diffusion, is characterized by integrating the electron (for the nMOSFET) density (n) over the Si film and defining an effective channel length based on the derived $\phi(x, y)$ [7].

For strong inversion, the 2D effects are less severe but the quantization effects are more significant, and dependent on t_{Si} as well as ε_x. Thus, an iterative, self-consistent solution, dependent on V_{GfS} and V_{GbS}, of the 1D (in x) Schrödinger and Poisson equations in the thin Si-film channel of the generic DG MOSFET is derived. A classical solution from Poisson's equation, approximated as

$$\frac{d^2 \phi}{dx^2} \cong \frac{qn}{\varepsilon_{Si}} , \qquad (2)$$

is derived first, using the general boundary conditions for the front and back surface potentials, ϕ_{sf} and ϕ_{sb}, and a smoothing-function approximation for (ϕ_{sf} - ϕ_{sb}), the back-to-front integral of the electric field [2]. The classical solution facilitates making an approximation (for η in (3)) regarding

inversion-charge partitioning between the front and back gates, as well as an initial guess for the iterative quantum-mechanical solution. The analytical solution of the Schrödinger equation (i.e., the eigenfunctions $\psi_j(x)$, or wavefunctions, which describe the carrier distribution in the Si film, and the eigenvalues E_j, which define the quantized 2D subband energy levels) is derived using a variational approach and is linked to Poisson's equation via Newton-Raphson iteration. The generic nature of the model results from the use of a general expression for the eigenfunctions:

$$\psi_j(x) = \frac{a_j}{2}\sqrt{\frac{2}{t_{Si}}}\sin\left(\frac{(j+1)\pi x}{t_{Si}}\right)\left(e^{-b_j x/t_{Si}} + \eta e^{-b_j (t_{Si}-x)/t_{Si}}\right)$$

$$\text{w/ } j = 0, 1, 2, \ldots \qquad (3)$$

η ($0 \le \eta \le 1$) reflects the bias-dependent inversion-charge partitioning mentioned above; $\eta = 1$ for the symmetrical DG device if $V_{GfS} = V_{GbS}$. The eigenfunctions are used to define n(x) in Poisson's equation, which is solved for the electric potential $\phi(x)$. Then $\psi_j(x)$ and $\phi(x)$, via operational integrations over the Si-film thickness, define expectation values for kinetic and potential energies of the electrons, the sum of which is minimized to complete the characterization of E_j and $\psi_j(x)$. The iterative-solution loop is closed by the characterization of the inversion charge density in all the significant (we assume the first four) 2D subbands:

$$-Q_i = \frac{4\pi q k_B T}{h^2}\left[g m_d \sum_j \ln\left(1 + \frac{n_i^2}{N_c N_{CH}}\exp\left(\frac{q\phi_{sf} - E_j}{k_B T}\right)\right)\right] + \frac{4\pi q k_B T}{h^2}\left[g' m_d' \sum_j \ln\left(1 + \frac{n_i^2}{N_c N_{CH}}\exp\left(\frac{q\phi_{sf} - E_j'}{k_B T}\right)\right)\right]$$

$$\text{w/ } j = 0, 1 \, . \qquad (4)$$

The quantization modeling (of ψ_j, E_j, ϕ, Q_i, and the implied gate capacitance C_G) has been broadly verified via SCHRED [8], a self-consistent numerical Poisson-Schrödinger solver as exemplified in Figs. 2-6.

The 1D Schrödinger-based solution (4) is perturbed by V_{DS}, and, with accounting for bias-dependent electrical channel length L_{eff} [2], a source-to-drain integration (in y) of the Q_i-defined current expression, including diffusion and

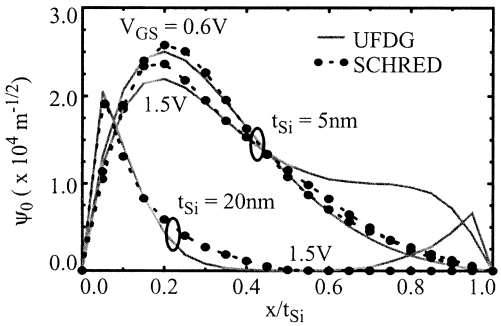

Fig. 2. UFDG- and SCHRED-predicted lowest-energy subband wavefunctions versus normalized position in the Si film of asymmetrical DG nMOSFETs having n^+ and p^+ polysilicon gates with t_{oxf}=t_{oxb}≡t_{ox}=1.5nm.

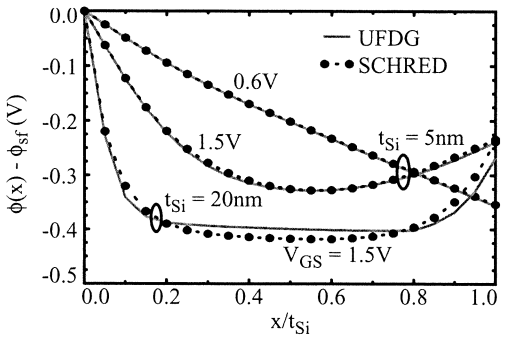

Fig. 3. UFDG- and SCHRED-predicted electric potentials versus normalized position in the Si film of the noted asymmetrical DG nMOSFETs.

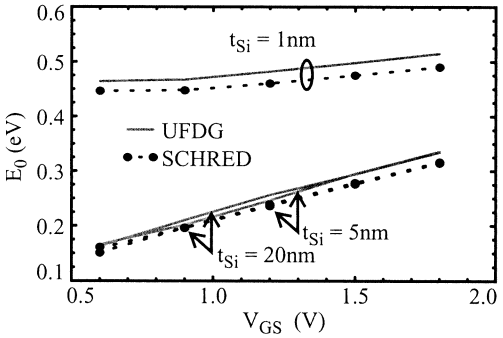

Fig. 4. UFDG- and SCHRED-predicted lowest ground-state energy versus gate voltage for asymmetrical DG nMOSFETs with different Si-film thicknesses.

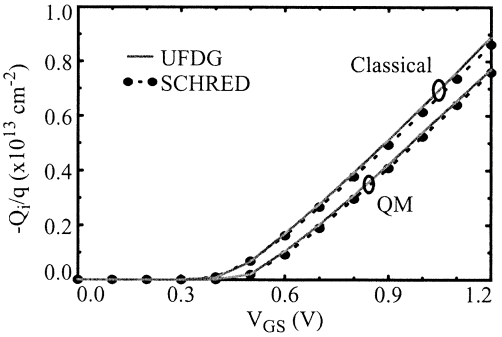

Fig. 5. Integrated inversion-electron density versus gate voltage predicted by UFDG and SCHRED (QM), contrasted to the modeled classical dependences, for the noted t_{Si}=5nm asymmetrical DG nMOSFET.

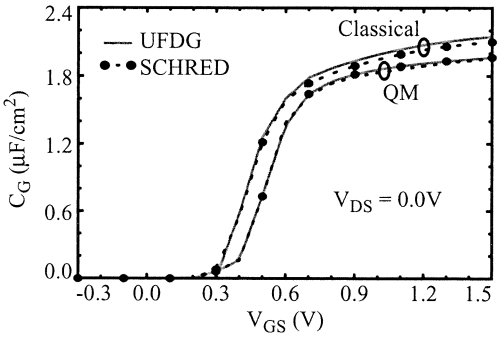

Fig. 6. UFDG- and SCHRED-predicted (QM) intrinsic gate capacitance (without the overlaps) versus gate voltage, contrasted to the modeled classical dependences, for the noted t_{Si}=5nm asymmetrical DG nMOSFET.

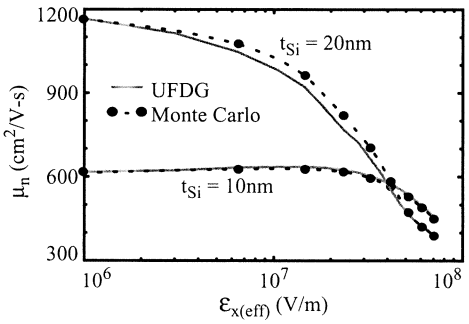

Fig. 7. Electron mobility versus effective transverse electric field in DG nMOSFETs from UFDG, supported by Monte Carlo simulations [9]; t_{ox}=1.0nm, T=300^{o}K. Note that $\varepsilon_{x(eff)}$~-Q_i/ε_{Si} in asymmetrical devices, whereas $\varepsilon_{x(eff)}$~-$Q_i/2\varepsilon_{Si}$ in symmetrical devices. The simulations accounted for both phonon and surface-roughness (Δ_m=0.1nm, l=1.5nm) [9] scatterings. The model is similarly supported for thinner t_{Si} for which volume-inversion effects are important [9], [10].

drift components, yields the channel current, $I_{CH}(V_{GfS}, V_{GbS}, V_{DS})$. The Schrödinger-based solution is also used in the carrier mobility model, which accounts for phonon and surface-roughness scatterings [3]. The derived $\psi_j(x)$ are used to characterize the form factor for the former and the matrix element for the latter, giving the proper mobility dependences on t_{Si} and ε_x as verified by Monte Carlo transport simulations exemplified in Fig. 7. The benefit of volume inversion [9], [10] for sufficiently thin t_{Si} is faithfully predicted by the mobility model. The carrier transport in UFDG is modeled as quasi-ballistic via an accounting for velocity overshoot derived from the Boltzmann transport equation and its moments [11]. The ballistic-current limit, defined by Q_i and the thermal injection velocity at the source [3], is used to define a smoothing function for I_{CH} that properly limits the current.

The network representation of UFGD is shown in Fig. 8. Note that in addition to I_{CH}, the parasitic BJT current, and the associated recombination/generation currents, are included, as is GIDL current, which in fact can be quite significant in DG DG MOSFETs [12]. The UFDG terminal charging currents are described as

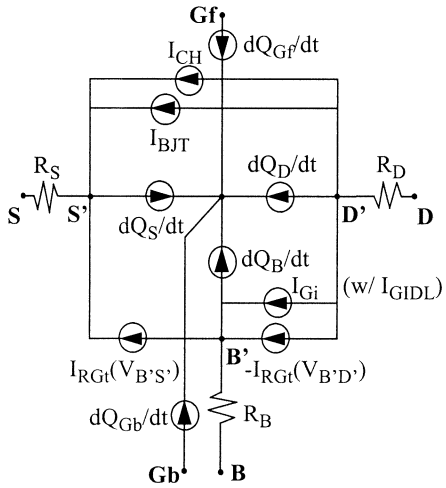

Fig. 8. Network representation of the UFDG model.

$$\frac{dQ_j}{dt} = \sum_i \frac{\partial Q_j}{\partial V_{iS}} \frac{dV_{iS}}{dt} \quad , \; i = Gf, Gb, D, B \qquad (5)$$

where j here signifies each of the five terminals (Gf, Gb, S, D, and B, the latter being the body even though it normally floats); each Q_j is defined by properly integrating charge components, physically linked to the I_{CH} modeling, over the channel region [2]. Thus, all transcapacitances are properly modeled. Further, parasitic overlap capacitances, front and back, and series resistances, including gate-gate resistance which can possibly undermine the DG MOSFET performance in transient operation [12], are included in the model as well.

The UFDG model is process/physics-based, meaning that its key parameters relate directly to the device structure or physics. Because of this basis, the number of model parameters is small relative to those of empirical compact models, and the parameters can be evaluated straightforwardly [2], in contrast to the complex measurement-based extraction of empirical parameters. Hence, verification of UFDG can be done straightforwardly based on numerical simulation of particular device structures [2], [3], as exemplified in Figs. 2-7. We stress that the UFDG simulations were done with model cards defined exclusively from the device structure, or domain, and the physical modeling utilized in the device simulator.

3. UFDG APPLICATIONS

Using the classical version of UFDG (Ver. 1.0 [2]), we previously showed significant speed superiority of L_{eff} = 50nm DG CMOS over a single-gate counterpart [13]. Here, we use UFDG-2.0 to show that the quantization effects can actually enhance the speed superiority. Using UFDG in Spice3, we simulated CMOS-inverter ring oscillators comprising asymmetrical DG MOSFETs with n^+ and p^+ polysilicon gates and $V_{GfS} = V_{GbS} \equiv V_{GS}$. Although the poly gates yield relatively high threshold voltages as revealed in Fig. 9, the predicted propagation delay is much shorter than that of the single-gate (V_{GbS} = 0) counterpart circuit, especially at low V_{DD}, and the DG advantage is substantively enhanced by the quantization as illustrated in Fig. 10. The DG speed superiority is attributed mainly to the nearly ideal subthreshold slope, yielding very high I_{on} relative to the that of the SG devices, as noted in [13] but dramatically enhanced here because the quantization effects are more severe in the SG devices (see Fig. 9). We stress here, based on UFDG-2.0 predictions and projections, that I_{on} in a DG MOSFET, with asymmetrical or symmetrical gates, can be much higher than just twice the current in the SG counterpart device at low V_{DD} (see Fig. 9). This high current, and the low intrinsic C_G of DG MOSFETs (see Fig. 6 and [3]) underlie the remarkable speed superiority, and in fact suggest that the DG CMOS technology can be made *pragmatic* by trading off added parasitics for eased processing while retaining outstanding performance.

As noted, UFDG is applicable to conventional FD/SOI MOSFETs as well as DG devices. Here we use UFDG to

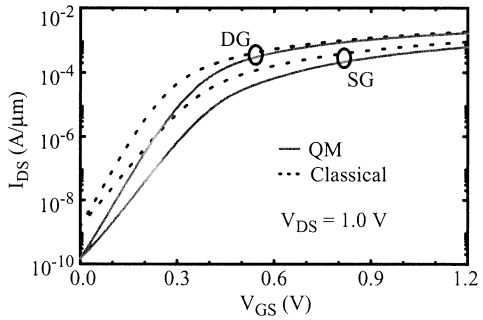

Fig. 9. UFDG-predicted current-voltage characteristics for asymmetrical DG and SG (asymmetrical DG structure with V_{GbS}=0) nMOSFETs, with (QM) and without the quantization modeling; L_{eff}=50nm, t_{Si}=10nm, t_{ox}=3nm. Note the more severe QM effect on the SG-device current, which is due to higher ε_x.

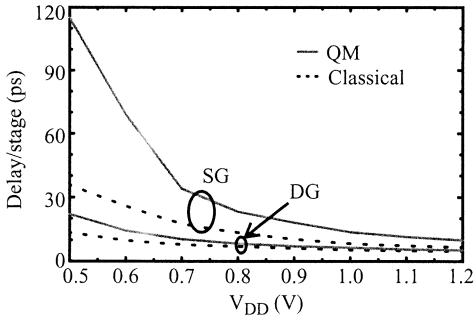

Fig. 10. Predicted propagation delays versus supply voltage from UFDG/Spice3 simulations of unloaded 9-stage CMOS-inverter ring oscillators comprising asymmetrical DG and SG (V_{GbS}=0) MOSFETs, with (QM) and without the quantization modeling; L_{eff}=50nm, t_{Si}=10nm, t_{ox}=3nm. Gate-source/drain overlaps of 40% of L_{eff} were assumed for all gates, front and back. Note the QM enhancement of the DG speed superiority.

check the scalability and project the performance of FD/SOI CMOS. We roughly calibrated UFDG to numerical simulation-based designs of FD/SOI CMOS devices scaled along the SIA ITRS [1] to L_{gate} = 9nm [6]. The enhancement-mode devices were designed with thick BOX and low N_{CH} ($10^{15}cm^{-3}$) for acceptable I_{off}, including in the L_{min} devices. For high performance, we found that a common gate with midgap work function Φ_G = 4.6V may suffice, but extremely thin t_{Si} (and t_{oxf}, or EOT [1]) is required, which limits the scalability [6]. For the L_{gate} = 28nm generation, UFDG/Spice3 unloaded ring-oscillator simulations, including parasitics, yield the propagation delay/stage (t_d) plotted in Fig. 11 versus Φ_G. The predicted nominal speed is outstanding; and its sensitivity to Φ_G is small, thus implying some gate-selection flexibility. This design flexibility is subject to the I_{off}-Φ_G sensitivity, but as shown in Fig. 11, this sensitivity is not too restrictive.

4. SUMMARY

The process/physics-based UFDG model, in essence a compact Poisson-Schrödinger solver applicable to nano-scale DG and FD/SOI MOSFETs, has been overviewed. Its truly physical nature was exemplified, and the afforded straightforward evaluation of its single small set of parameters, related to device structure, was demonstrated in

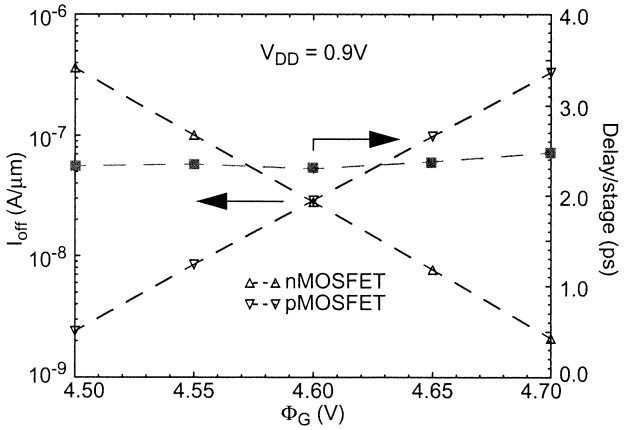

Fig. 11. Predicted propagation delays versus gate work function from UFDG/Spice3 simulations of unloaded 9-stage CMOS-inverter ring oscillators comprising FD/SOI MOSFETs; L_{gate}=28nm w/ 20% source/drain overlap, t_{Si}=7nm, t_{oxf}=1.1nm.

model verifications based on numerical device simulations. Its predictive capability was demonstrated via UFDG/Spice3 simulations that projected outstanding speed superiority for scaled DG CMOS over a single-gate counterpart, and for FD/SOI CMOS scaled to 28nm via use of a single midgap gate.

ACKNOWLEDGMENTS

This work was supported by Motorola, AMD, and the SRC. Significant contributions were made by current and former graduate students, including Ping Yeh, Yan Chong, Keunwoo Kim, Vishal Trivedi, and Murshed Chowdhury.

REFERENCES

1. *International Technology Roadmap for Semiconductors*. Semiconductor Industry Assoc., San Jose, CA, 2001.
2. M.-H. Chiang, Ph.D. Dissertation, Univ. Florida, Gainesville, 2001.
3. L. Ge, Ph.D. Dissertation, Univ. Florida, Gainesville, 2002.
4. *UFDG MOSFET Model User's Guide*. SOI Group (http://www.soi.tec.ufl.edu), Univ. Florida, Gainesville, May 2002.
5. K. Kim and J.G. Fossum, *IEEE Trans. Electron Devices*, vol. 48, p. 294, Feb. 2001.
6. J. G. Fossum, V. P. Trivedi, and K. Wu, *Proc. IEEE Internat. SOI Conf.*, p. 135, Oct. 2002.
7. P. C. Yeh and J. G. Fossum, *IEEE Trans. Electron Devices*, vol. 42, p. 1605, Sept. 1995.
8. D. Vasileska and Z. Ren, *SCHRED-2.0 Manual*. Purdue Univ., W. Lafayette, IN, Feb. 2000.
9. F. Gámiz, et al., *Proc. 10th Int. Symp. SOI Technology and Devices*, vol. ECS 2001-3, Mar. 2001.
10. L. Ge and J. G. Fossum, *IEEE Trans. Electron Devices*, vol. 49, p. 287, Feb. 2002.
11. L. Ge, J. G. Fossum, and B. Liu, *IEEE Trans. Electron Devices*, vol. 48, p. 2074, Sept. 2001.
12. J. G. Fossum, K. Kim, and Y. Chong, *IEEE Trans. Electron Devices*, vol. 46, p. 2195, Nov. 1999.
13. J. G. Fossum, L. Ge, and M.-H. Chiang, *IEEE Trans. Electron Devices*, vol. 49, p. 808, May 2002.