Carrier Transit Time Optimization of a High Speed Bipolar Transistor Using Numerical Device Simulation

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ABSTRACT

The doping profile of a high speed silicon NPN bipolar junction transistor (BJT) was optimized using numerical device simulation (TCAD). A technique was employed in which the transient charge storage in the device was related to its carrier transit time, thereby providing a graphic demonstration of the impact of high carrier injection effects on the speed performance of the device. This knowledge enabled the engineering of a selectively implanted collector (SIC), which dramatically improved the switching frequency of the transistor over an identical device with a low-doped epi collector. The debiasing effect of the intrinsic collector resistance was also investigated for both devices. A comparison to preliminary measured electrical data is made for the transistor with the SIC.

Keywords: bipolar transistor, profile optimization, device simulation, charge storage, carrier transit time

1 INTRODUCTION

The optimization of bipolar transistors for high speed applications requires knowledge of the trade-off between several competing factors, including emitter-base junction charging time, base transit time, base-collector capacitance, high injection degradation, and collector debiasing [1]. Numerical device simulation (TCAD) is an effective tool in assisting with this optimization because the relative merits of different structures and doping profiles can be assessed virtually, without the need for physical prototypes, and also because the device simulator allows direct access to fundamental physical quantities that cannot be easily measured.

This paper demonstrates the application of a commercially available numerical device simulator [2] to optimizing the carrier transit time of a silicon NPN bipolar junction transistor (BJT). Structure and doping optimization of BJTs is not new [3], but the approach of analyzing transient charge storage using numerical device simulation is relatively novel and not widely practiced [4]. A technique for determining the debiasing effect of the intrinsic collector resistance is also demonstrated in this work.

2 METHODOLOGY

A two-dimensional device structure (Fig. 1) was constructed from analytical doping profiles using a meshing tool [5]. The intrinsic emitter, base, and collector profiles were chosen to meet the desired performance criteria. Since a selectively implanted collector (SIC) was included to improve the high injection efficiency of the transistor, structures both with and without the SIC were studied in detail. The remaining profiles, such as the buried layer, substrate, and buried layer contact, were adjusted to match existing secondary ion mass spectroscopy (SIMS) data.

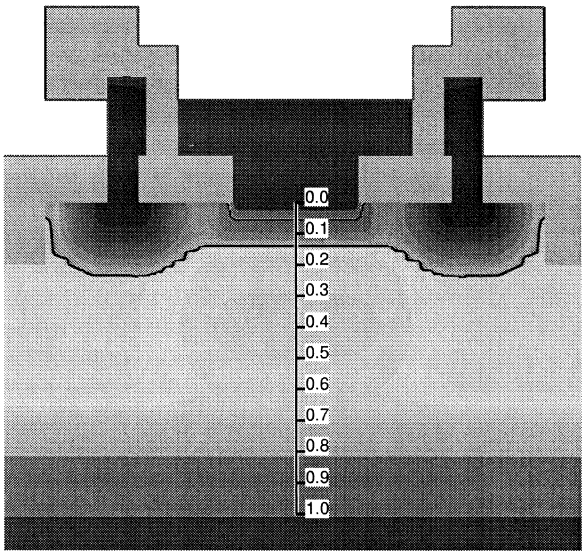

Figure 1: Two-dimensional NPN bipolar device structure.

The device simulator was first calibrated to an existing BJT technology by suitably altering minority carrier lifetimes, surface recombination velocities, and mobilities in order to ensure a good match to DC and AC measurements. A hydrodynamic electron transport model using a parameter-adjusted Masetti mobility was employed, along with a Slotboom and de Graff band-gap narrowing model, and both Shockley-Read-Hall and Auger carrier recombination enabled. A Caughey-Thomas velocity saturation model was used with a carrier temperature

driving force for electrons and a quasi-Fermi level gradient driving force for holes.

Standard DC and AC simulations were performed including both forward and reverse Gummel and output characteristics, small-signal analysis over both bias and frequency, and junction capacitance over bias. In addition, the solution variables at several bias points in the forward active region of operation were sampled along a vertical cutline through the center of the emitter (see Fig. 1) in order to investigate high carrier injection, charge storage, and collector debiasing effects.

3 RESULTS

Two different high injection mechanisms (base conductivity modulation and the Kirk effect) were simultaneously studied by examining the hole concentration as a function of forward bias (Fig. 2). By subtracting the equilibrium hole concentration from the hole concentration

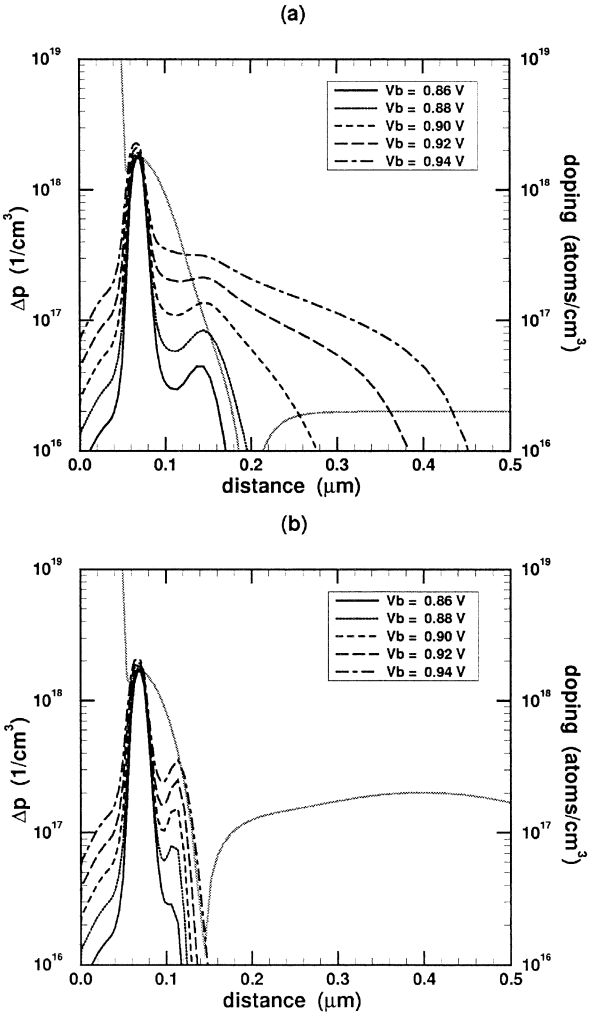

Figure 2: Modulation of the hole concentration from equilibrium under forward bias conditions for devices (a) without a SIC and (b) with a SIC.

under forward bias conditions, the carriers responding to electron injection were separated from the carriers generated by ionized acceptor atoms. The onset of base conductivity modulation is indicated by a differential hole concentration approaching the acceptor doping level, whereas the onset of the Kirk effect is indicated by a spreading of the holes into the collector space-charge region. In particular, the addition of the SIC (Fig. 2b) effectively suppresses the base push-out as compared to the device without the SIC (Fig. 2a). Eliminating this phenomenon has important implications when considering the high speed switching performance of the transistor.

The frequency of unity current gain ($f\tau$) is inversely related to the total transit time for a carrier through the device [1]. Although $f\tau$ can be obtained directly from a small-signal analysis, no insight is gained into the factors limiting the transit time response. Instead, a spatial distribution of the dynamic charge storage was extracted from a series of DC solutions. First, the modulation of the electron carrier distribution (Δn) was calculated by subtracting two solutions at incrementally different forward bias points (ΔV_{be} = 1 mV). The modulation of electron current density (ΔJ_c) was also calculated directly from these solutions. The dynamic charge storage time (S) along a cutline through the active center of the device was then calculated in terms of these variables using

$$S(x) = q\left(\frac{\Delta n(x)}{\Delta J_c(x)}\right), \tag{1}$$

where q is the charge of an electron. The quantity S has units of time per unit length and represents the storage or delay time associated with a given region in the device (Fig. 3). Therefore, the total carrier transit time (τ) is just the integral of the dynamic charge storage time along the current path through the device (Fig. 4):

$$\tau = \int_a^b S(x)\,dx\,. \tag{2}$$

The benefits of the SIC can clearly be seen. The charge storage region widens with increasing forward bias in the non-SIC device (Fig. 3a), resulting in a monotonically increasing carrier transit time with a minimum of only 10ps (Fig. 4a). In contrast, the SIC device has a more confined charge storage region (Fig. 3b), resulting in a carrier transit time which reaches a minimum approaching 5ps at a V_{be} of 0.88 to 0.90 volts (Fig. 4b). This transit time corresponds to an $f\tau$ of 29 GHz, which compares well with the value obtained directly through a small-signal simulation of the device.

The final quantity of interest is the Ohmic drop or debiasing of the collector due to series resistance under high injection. Although the device simulator directly gives the electrostatic potential resulting from a solution of

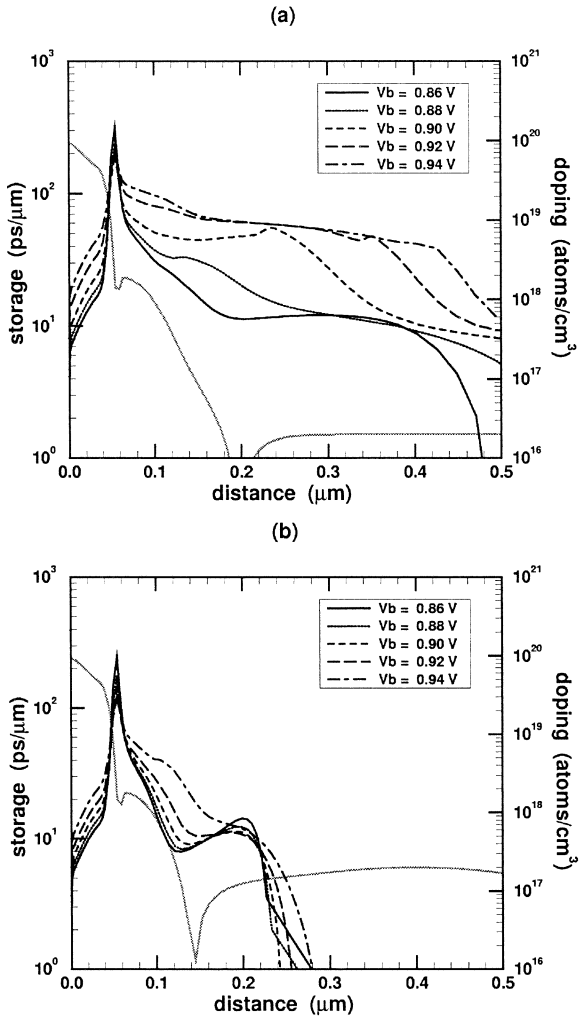

Figure 3: Dynamic charge storage time under forward bias conditions for devices (a) without a SIC and (b) with a SIC.

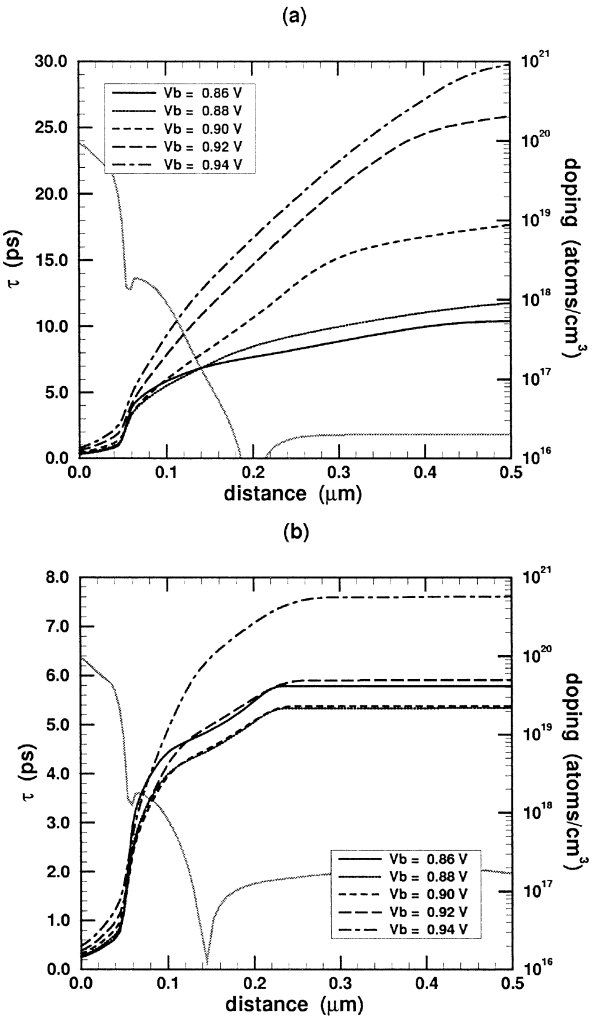

Figure 4: Integrated carrier transit time under forward bias conditions for devices without a SIC (a) and with a SIC (b).

Poisson's equation, this quantity is not equal to the true Ohmic drop because it includes the built-in potential from gradients in the doping concentration. Therefore, the correct expression for the Ohmic drop (ΔV_c) must subtract the built-in equilibrium potential (Fig. 5):

$$\Delta V_c(x) = V_c - \left[\psi(x; V_b, V_c) - \psi(x; 0, 0)\right], \qquad (3)$$

where V_c is the voltage applied to the collector terminal, and $\psi(x; V_b, V_c)$ is the solution to Poisson's equation at the specified bias point. The corresponding collector resistance (R_c) is then given by

$$R_c(x) = \frac{\Delta V_c(x)}{I_c}, \qquad (4)$$

where I_c is the total collector current. Once again, the non-SIC device shows severe high injection limitations. The Ohmic drop near the base-collector junction is close to 0.8 Volts, driving the transistor into quasi-saturation and degrading the speed performance of the device (Fig. 5a). In the SIC device, the Ohmic drop is reduced to less than 0.4 Volts, indicating that the more heavily doped collector can adequately handle the current under high injection conditions (Fig. 5b).

A comparison was made to measured DC and AC electrical data for the transistor with the SIC. The forward Gummel characteristics are presented in Fig. 6a, and the $f\tau$ response over forward bias at two different collector voltages is presented in Fig. 6b. The agreement between simulation and measurement is fairly good considering the fact that the process is still under development and that discrepancies between simulation and measurement are to be expected. This discrepancy should diminish as the process matures. A similar comparison was made for the transistor without the SIC with similar results. In particular, a lower forward saturation current (I_s) and $f\tau$ were observed as expected.

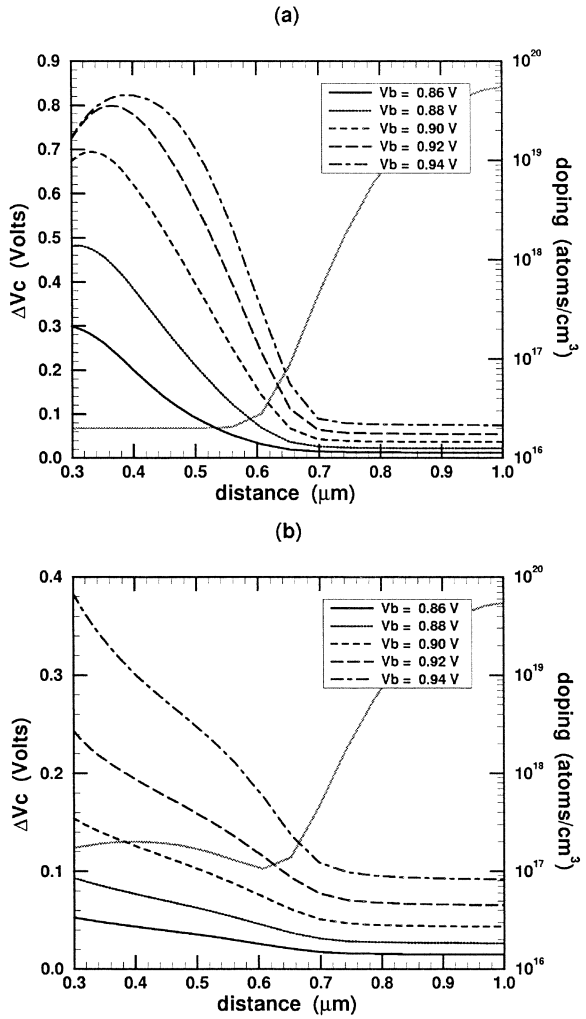

Figure 5: Ohmic potential drop in the intrinsic collector under forward bias conditions for devices without a SIC (a) and with a SIC (b).

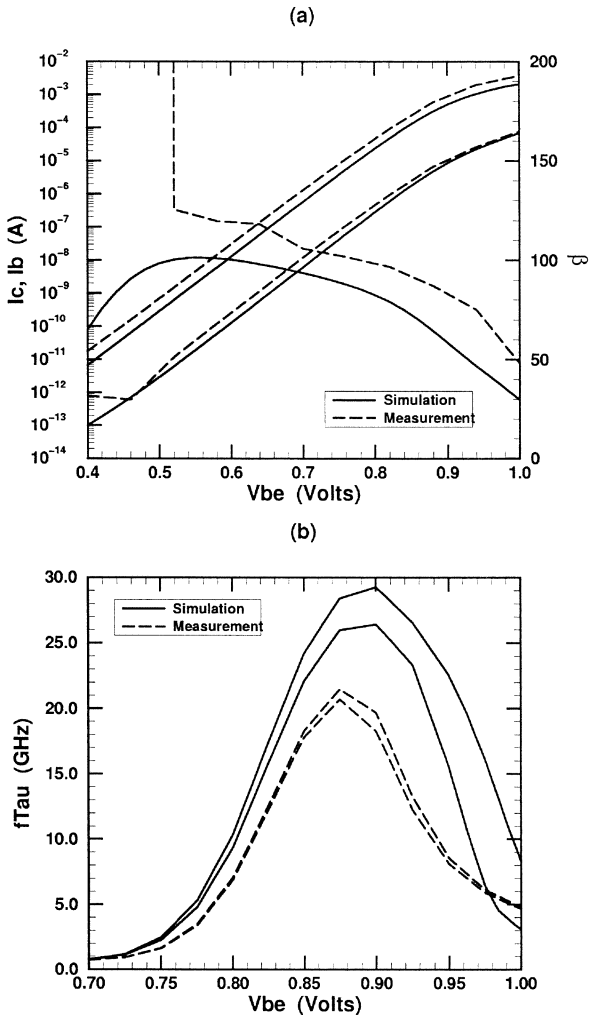

Figure 6: Comparison of simulation to measurement for the forward Gummel characteristics (a) and the $f\tau$ response over forward bias (b) of a device with a SIC.

4 CONCLUSIONS

A methodology for using numerical device simulation to optimize the carrier transit time of a high speed bipolar transistor has been presented. In addition to performing routine DC and AC analyses, the behavior of internal quantities that cannot be easily measured, such as the electrostatic potential and carrier concentrations, can be studied under different bias conditions. By quantifying these physical effects, a greater insight can be gained into the factors that limit the performance of a device.

The significance of a selectively implanted collector was demonstrated in several ways. First, the onset of base push-out (Kirk effect) under high injection conditions was successfully suppressed by the inclusion of a SIC in the device. The suppression of this effect correlated directly with a reduction in the dynamic charge storage and total carrier transit time, resulting in a device with a higher switching speed ($f\tau$). Finally, the reduction in collector resistance brought the transistor out of quasi-saturation during heavy forward bias, further improving its high speed capabilities. The TCAD and related tools described in this paper have directed and accelerated the development of this technology.

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