Threshold Voltage Shifts in Narrow-Width SOI Devices Due to Quantum Mechanical Size-Quantization Effects*

Shaikh S. Ahmed and Dragica Vasileska

Department of Electrical Engineering and Center for Solid State Electronics Research
Arizona State University, Box 875706, Tempe, AZ 85287-5706, USA.
shaikh.ahmed@asu.edu, vasileska@asu.edu

ABSTRACT

We have investigated the role of quantum mechanical space-quantization effects on the operation of a narrow-width SOI device structure. The presence of a two-dimensional carrier confinement gives rise to larger average displacement of the carriers from the interface proper and lower sheet electron density in the channel region. This, in turn, results not only in a significant increase in the threshold voltage but also in its pronounced channel width dependency. In this work, we have used classical 3D Monte Carlo particle-based simulations. Quantum mechanical space-quantization effects have been accounted for via an *effective potential* scheme that has been quite successful in describing bandgap widening effect and charge set back from the interface.

Keywords: SOI devices, narrow channel effect, effective potential, 3D Monte Carlo Simulation.

1 INTRODUCTION

1.1 Motivation

The aggressive downscaling of classical CMOS devices and the associated short-channel effects are accelerating the emergence of new technologies including both new materials and advanced structures. With these efforts, Silicon-On-Insulator (SOI) devices are found to be advantageous over their bulk silicon counterparts in terms of reduced parasitic capacitances, reduced leakage currents, increased radiation hardness, as well as inexpensive fabrication process. IBM launched the first fully functional SOI mainstream microprocessor in 1999 predicting a 25-35% performance gain over bulk CMOS. As we approach the 0.1 μm generation and beyond, SOI is expected to be the technology of choice for system-on-a-chip applications which need high-performance CMOS, low-power, embedded memory, and bipolar devices [1].

1.2 Device Structures in SOI System

Silicon-On-Insulator (SOI) devices can be classified into two broad categories: partially-depleted (PD) and fully-depleted (FD) SOI devices. With significant number of investigations, it has been shown that FD-SOI technology has the advantages over PD-SOI technology with regard to lower junction capacitance and better subthreshold swing.

It has also been reported that in both PD and FD-SOI devices there occurs a threshold voltage increase that depends upon both the impurity concentration and the SOI thickness because the inversion layer is very thin but as wide as normal gate electrode. However, in an ultra-narrow SOI MOSFET proposed by Majima *et al.* [2], and schematically shown in Fig. 1, the threshold voltage depends not only on the SOI thickness but also on the channel width, because horizontal carrier confinement also takes place in the narrow channel.

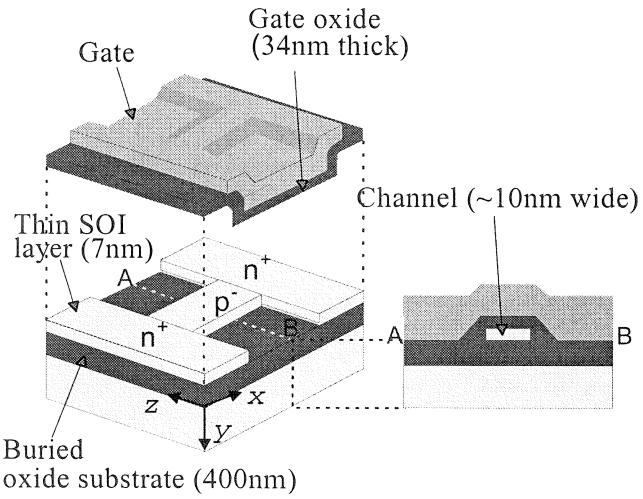


Fig. 1. Device structure of ultra-narrow channel FD-SOI device structure.

Due to the experimental evidence of threshold voltage shift and the observation of Coulomb-blockade effects in the narrowest-width devices from Fig. 1, it is the goal of this paper to investigate transfer and output characteristics of narrow-width FD-SOI MOSFETs schematically shown in Fig. 1. For this purpose, we rely on the validity of the effective potential approach due to Ferry [3], according to which the effective potential seen by electrons is represented as a convolution of the Hartree potential obtained from solving Poisson's equation and a Gaussian function. In other words,

$$V_{eff}(x) = \frac{1}{\sqrt{2\pi}a_0} \int_{-\infty}^{\infty} V(x') \exp\left(-\frac{(x-x')^2}{2a_0^2}\right) dx' \quad (1)$$

where $V(x')$ is the actual potential, and a_0 is the spatial spread of the wavepacket. The effective potential accounts for the *size of the electron* and its associated wavepacket, which feels the presence of barriers, etc. at a distance. From this Ansatz, the actual particle is treated as point-like in the presence of the effective potential associated with its wave-like nature, leading back to a classical particle simulation scheme. In our calculations, we have used $a_0 = 0.7$nm along the confining directions and a_0 = 1nm along the channel. The inclusion of the effective potential approach calculation into our 3D Monte Carlo particle based simulator gives rise to an increase of the required CPU time by about 10% for both equilibrium and nonequilibrium conditions as it depends upon the mesh size used in solving the 3D Poisson equation. It is worth noting that in some previous investigations we have demonstrated that the effective potential approach can be successfully used for the case of two-dimensional carrier confinement effects in narrow width wires, by showing that the simulation results for the line electron density obtained by using the effective potential approach and the self-consistent solution of the 2D Schrödinger-Poisson problem agree very well with each other [Ref. 4].

2 SIMULATION RESULTS

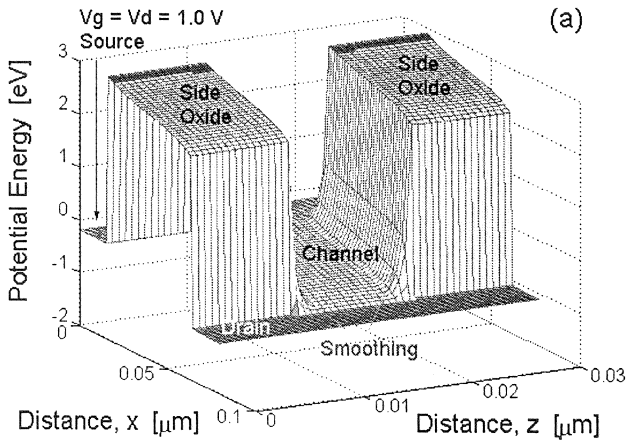
The device structure we simulate consists of a thick silicon substrate, on top of which is grown 400 nm of buried oxide. The thickness of the silicon on insulator layer is 7 nm, with p^- region width of 10 nm. The channel length is 50 nm and the doping of the p^- layer is 10^{16} cm^{-3}. On top of the SOI layer sits gate-oxide layer, the thickness of which is 34 nm. The doping of the source/drain junctions equals 10^{19} cm^{-3}, and the gate is assumed to be a metal gate with workfunction equal to the semiconductor affinity. The use of the low source-drain doping is justified by the fact that most of the carriers we are simulating are residing in the source/drain regions and the reduction of the source/drain doping leads to a smaller ensemble of carriers that needs to be simulated. Even though this device structure has top oxide thickness of 34 nm, it serves as a proof of concept that a two-dimensional quantization effect can give rise to significant threshold voltage shift in nano-scale SOI device structures.

As already mentioned, we employ a classical 3D Monte Carlo particle-based simulator to obtain the device transfer and output characteristics, where effective potential approach has been used to incorporate, in a very efficient manner, for the quantum mechanical size quantization effects that are not otherwise included into the simulator. Regarding the Monte Carlo transport kernel, the explicit inclusion of the longitudinal and transverse masses in the silicon conduction band is important and this is done in the program using the Herring-Vogt transformation [5]. Intravalley scattering is limited to acoustic phonons. For the intervalley scattering, we include both *g*- and *f*-phonon processes [6]. At present, impact ionization, Coulomb scattering and surface- roughness scattering are not included in the model. They are omitted as they tend to mask the role of space-quantization effects on the overall device performance.

We use the Incomplete Lower-Upper decomposition method for the solution of the 3D Poisson equation. After solving for the potential and convolving it with a Gaussian, the electric fields are calculated and used in the free-flight portion of the Monte Carlo transport kernel. However, the charges obtained from the EMC simulation are usually distributed within the continuous mesh cell instead of on the discrete grid points. The particle mesh method (PM) is used to perform the switch between the continuum in a cell and discrete grid points at the corners of the cell. Two PM-methods have been implemented in the present version of the code: the Nearest-Grid-Point (NGP) scheme and the Cloud-in-Cell (CIC) scheme. The cloud-in-cell scheme (CIC) produces a smoother force interpolation, but introduces self-forces on non-uniform meshes.

The device current is determined by keeping track of the charges entering and exiting each terminal; the net number of charges over a period of the simulation is then used to calculate the terminal current. The method is quite noisy, due to the discrete nature of the electrons and requires long simulation times, on the order of 2 to 3 ps.

In Fig. 2, we show the conduction band profile for the bias conditions $V_G = V_D = 1$V. The channel length equals 50 nm and the channel width is 10 nm. One can see that the effective potential shifts the conduction band edge upwards along the width and the depth of the device. It, therefore, accounts for the so-called band-gap widening effect, which leads to a reduction of the carrier density at the interface proper. Also, the electrons are moved away from the interface because of the additional perpendicular electric field in the vicinity of the Si-SiO_2 interface. In Fig. 3, we plot the electron density in the active region of the device. Including V_{eff} into the model results in a non-uniform channel with reduced electron density.



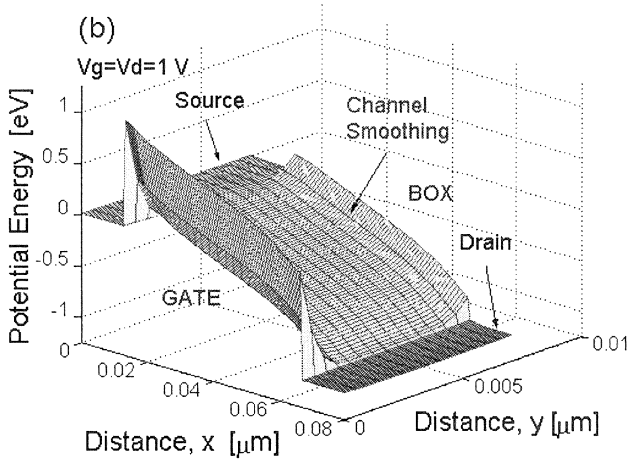
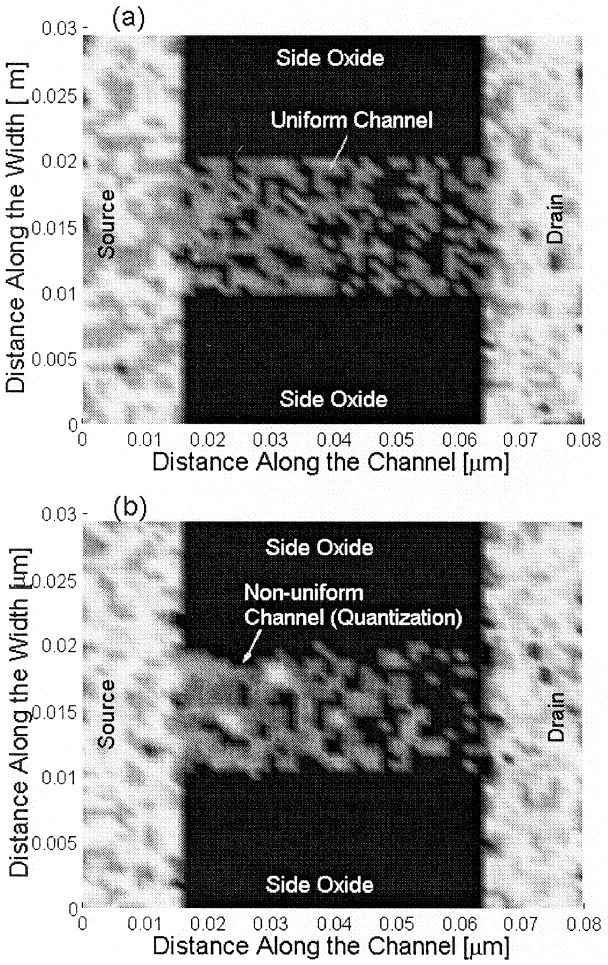


Fig. 2. Conduction band profile along (a) the width (X-Z plane) and (b) the depth (X-Y plane) of the device for the case when V_{eff} calculation is included in the model.

As shown in Fig. 3(c), the upward shift of the conduction band edge leads to approximately half an order of magnitude decrease in the electron density, which is consistent with previous quantum-mechanical simulations [Ref. 4].



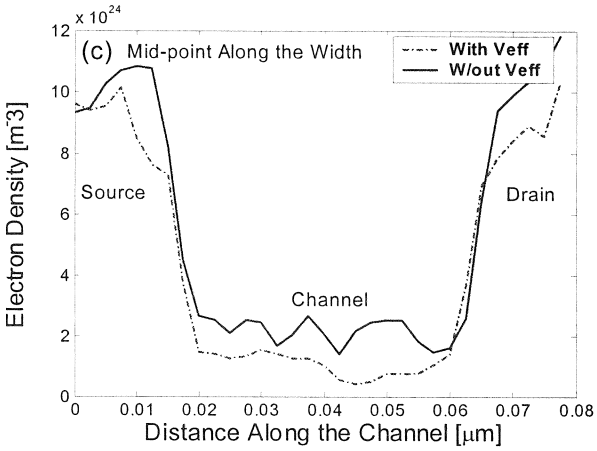


Fig. 3. Electron density distribution in the active region (a) without V_{eff} (b) with V_{eff} showing the charge set back, and (c) Electron density along the channel with and without V_{eff}. We have used $V_D = V_G = 1.0$ V in these simulations.

The device output characteristics are shown in Fig. 5(a) for gate voltage V_G equal to 1.0 V and 1.2 V, with and without V_{eff}. The device channel width equals 10 nm. There are three noteworthy features in this figure: with V_{eff}, the drive current is reduced, the threshold voltage (V_{th}) is increased, and the transconductance is degraded. The inclusion of V_{eff} reduces the drain current I_D, due to two factors: the reduced sheet density and, the reduced average carrier velocity (Fig. 4), the former being predominant. Also, since the slope of the I_D-V_D curve in the linear region is proportional to V_G-V_{th}, we see that for a given V_G, the inclusion of V_{eff} increases V_{th}. Finally, if for a given V_D we analyze the current increase between V_G equal to 1.0 V and 1.2 V, which is roughly proportional to transconductance, it is clear that transconductance is lower with V_{eff} included. This is to be expected due to the charge set back depicted in Figs. 3(b) and 3(c). Also noticeable in the device operation is a pronounced DIBL effect due to the low doping concentration of the thin silicon film.

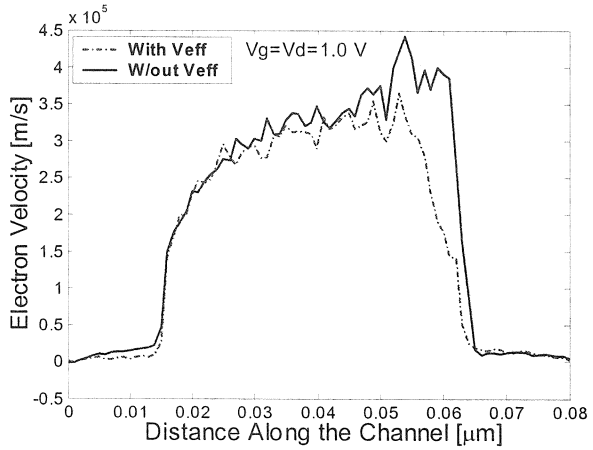


Figure 4. Average electron velocity for $V_D = V_G = 1.0$ V. The device width equals 10 nm.

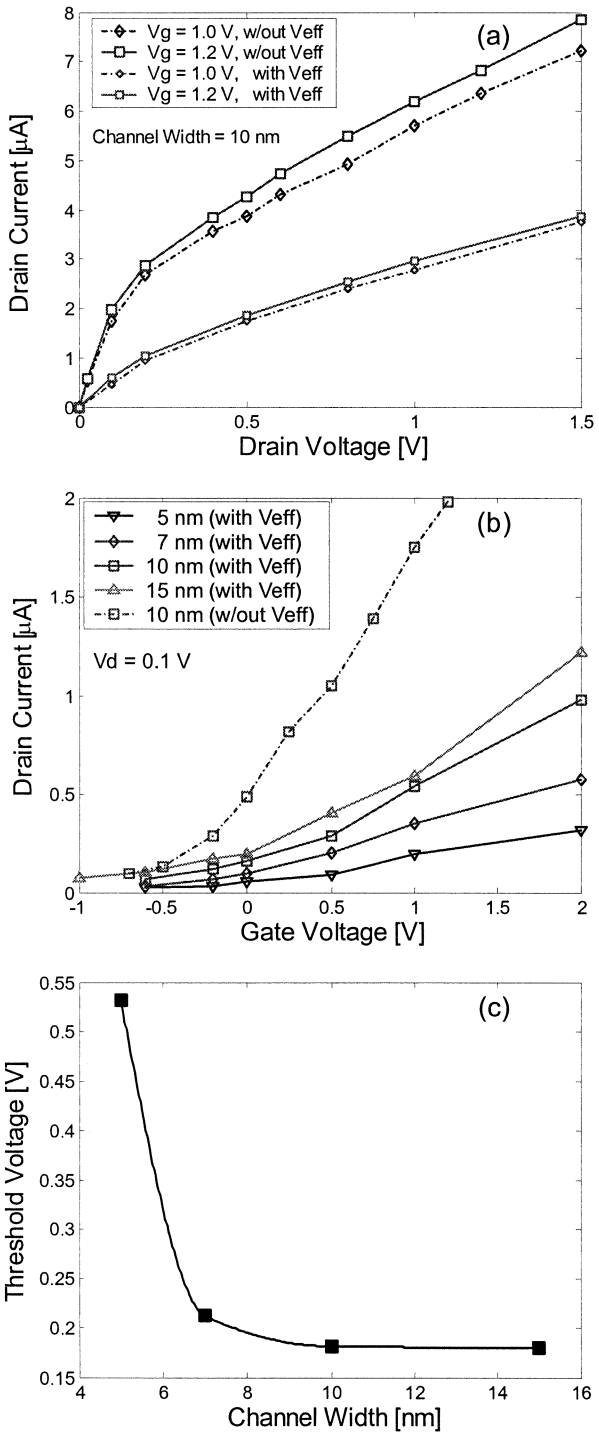


Fig. 5. (a) Output characteristics for V_G = 1.0 V and 1.2 V (b) Transfer characteristics of devices with 5, 7, 10 and 15 nm channel width for V_D = 0.1 V and (c) Variation of threshold voltage with channel width.

The quantization of charge in the inversion layer produces an expected increase in the threshold voltage of the device. This observation is more clearly seen from the results shown in Fig. 5(b), where we plot the drain current I_D as a function of the gate voltage V_G, for a drain voltage of V_D = 0.1 V. If we take as a criterion for determining the threshold voltage as being the gate voltage for which the drain current equals 10 μA/μm, we obtain a shift of approximately 300 mV when space-quantization effects are included in the model. Again, important is the fact that the threshold voltages for devices with different widths are not same. The channel width dependency of the threshold voltage has been shown in Figure 5(c). We observe a sharper increase in the threshold voltage at narrowest channel widths due to a strong quantum mechanical carrier confinement therein.

3 CONCLUSION

In this work, we have utilized the effective potential approach to successfully simulate two dimensional space quantization effects in a model of a narrow-channel SOI device structure. The effective potential provides a set back of the charge from the interface, and a quantization energy within the channel. Both of these effects lead to an increase in the threshold voltage. We find a threshold voltage shift of about 300 mV when the effective potential is included in the model for a device with 10 nm channel width. Also, there exists a pronounced channel width dependency of the threshold voltage that has been termed as the *quantum mechanical narrow channel effect*. The increase in the threshold voltage gives rise to a significant on-state current reduction, which depends upon the gate voltage bias. Larger degradation is observed for larger gate voltage.

REFERENCES

* This work has been supported by the Office of Naval Research.

[1] G. G. Shahidi, "SOI technology for the GHz era", *IBM J. Res. & Dev.* Vol. 46 No. 2/3, pp. 121-131, March/May 2002.

[2] H. Majima, H. Ishikuro, and T. Hiramoto, "Experimental evidence for quantum mechanical narrow channel effect in ultra-narrow MOSFETs", *IEEE Electron Dev. Lett.*, Vol. 21, pp. 396-398, 2000.

[3] D. K. Ferry, "The onset of quantization in ultra-submicron semiconductor devices", *Superlattices and Microstructures*, Vol. 27, pp. 61-66, 2000.

[4] R. Akis, S. Milicic, D. K. Ferry, and D. Vasileska, "An effective potential method for including quantum effects into the simulation of ultra-short and ultra-narrow channel MOSFETs", *in Proc. of the 4th Int. Conf. on Modeling and Simulation of Microsystems*, Hilton Head Island, SC, March 19-21, 2001, pp. 550-553.

[5] C. Herring and E. Vogt, "Transport and deformation-potential theory for many-valley semiconductors with anisotropic scattering", *Phys. Rev.*, Vol. 101, pp. 944-961, 1956.

[6] C. Jacoboni and L. Reggiani, "The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials," *Rev. Modern Phys.*, Vol. 55, pp. 645-705, 1983.