

Modelling of gain control in SiGe HBTs and Si bipolar transistors by Ge incorporation in the polysilicon emitter

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Abstract

This paper reports a theory for the base current in which Ge is incorporated in the polysilicon emitter. The competing influences of the Ge and the interfacial layer at the polySiGe/Si interface are investigated theoretically using an effective surface recombination velocity for the polySiGe emitter. A comparison with measured results is made and good agreement obtained. A Ge content of 19% gives a base current reduction by a factor of approximately four.

1 Introduction

To achieve high values of f_T and f_{max} in SiGe HBT's, it is necessary to minimise delay times in the base and collector of the transistor [1-3]. The base delay is minimised by using a narrow basewidth and large Ge gradient across the base to create a built-in electric field [1]. Such aggressive Ge profiles give very high values of gain β [3]. The collector delay is minimised by increasing the collector doping to decrease the transit time and to suppress the Kirk effect. Unfortunately high collector doping concentrations have the disadvantage of degrading the common emitter breakdown voltage BV_{CEO} of the transistor [4].

The trade-off between BV_{CEO} and β can be understood from the following well known equation:

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}} \quad (1)$$

This equation shows that if the gain of the transistor is too high, the common emitter breakdown voltage is degraded. To address this problem, a method is needed of reducing the gain without modifying the base Ge and B profiles.

In this paper a theory is developed for the base current of a bipolar transistor in which Ge is incorporated in the polysilicon emitter. This polysilicon emitter will allow the gain of a SiGe HBT to be controlled independently of the

Ge and B profiles in the base. An issue that needs to be addressed in polySiGe emitters is the competing influence of the Ge, which gives increased base current, and the interfacial layer, which gives reduced base current. The theory is used to quantify these two competing mechanisms and a comparison is made with measured devices.

2 Theory

In order to explain the above dependence of base current on Ge content in the polySiGe emitter, a theory has been developed for polySiGe emitters. The approach used defines an effective surface recombination velocity for the polySiGe emitter analogous to that used by Yu et al [6] for polySi emitters.

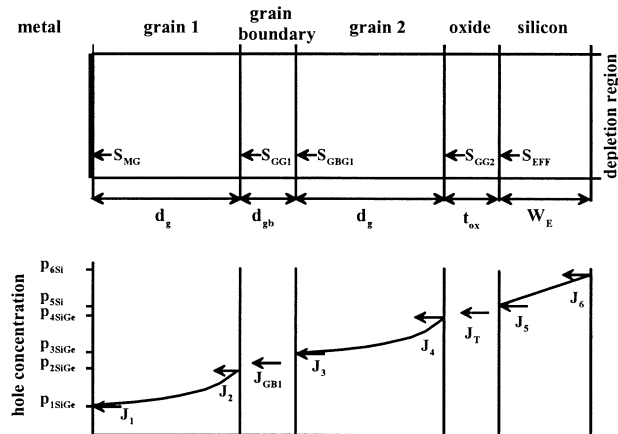


Figure 1: Schematic illustration showing the definition of effective surface recombination velocities.

An effective surface recombination velocity is defined at each interface in the polySiGe emitter, as illustrated in figure 1. The current at each interface is then written in terms of these recombination velocities. For example, the current density J_1 adjacent to the metal contact is given by:

$$J_1 = qS_M p_{1SiGe} \quad (2)$$

where S_M is the surface recombination velocity at the metal contact and p_{1SiGe} is the hole concentration in the SiGe layer adjacent to the metal contact.

Following the work of Yu et al [6], an equation for the current density J_4 at the left of the interfacial oxide layer can be defined:

$$J_4 = qS_p p_{4SiGe} \quad (3)$$

where S_p is an effective surface recombination velocity given by:

$$S_p = a_g - \frac{b_g^2}{a_g + S_{GB1}} \quad (4)$$

The parameters a_g and b_g depend on the physical properties of the polySiGe grains and are given by:

$$a_g = \frac{D_{pSiGe}}{L_{pSiGe}} \coth\left(\frac{d_g}{L_{pSiGe}}\right) \quad (5)$$

and

$$b_g = \frac{D_{pSiGe}}{L_{pSiGe}} \operatorname{csch}\left(\frac{d_g}{L_{pSiGe}}\right) \quad (6)$$

where d_g is the grain width, and L_{pSiGe} and D_{pSiGe} are the hole diffusion length and hole diffusivity in the polySiGe grain. The recombination velocity after the grain boundary shown in figure 5 is given by:

$$S_{GB1} = a_{gb} - \frac{b_{gb}^2}{a_{gb} + S_{G1}} \quad (7)$$

$$a_{gb} = \frac{D_{gbSiGe}}{d_{gb}} + S_{gbSiGe} \quad (8)$$

$$b_{gb} = \frac{D_{gbSiGe}}{d_{gb}} \quad (9)$$

where d_{gb} is the grain boundary width, and D_{gbSiGe} is the hole diffusivity in the polySiGe grain boundary and S_{gbSiGe} is the recombination velocity at the grain boundary interface. S_{G1} is then given by:

$$S_{G1} = a_g - \frac{b_g^2}{a_g + S_M} \quad (10)$$

Transport across the interfacial oxide layer is assumed to be by tunnelling, and the band diagram is illustrated in figure 2.

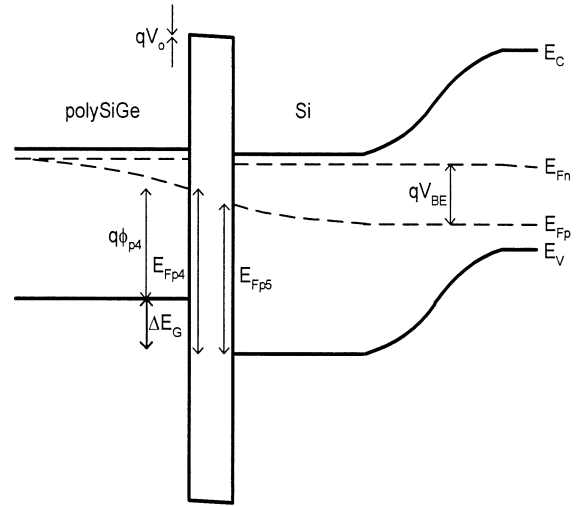


Figure 2: Band diagram of a polySiGe emitter

Using this band diagram, and noting that the energy E_{Fp4} contains the bandgap difference between Si and SiGe ΔE_G , the following equation for the effective surface recombination velocity S_{pl} of the polySiGe emitter can be derived:

$$S_{pl} = S_l + \left(\frac{1}{T_l} + \frac{F}{S_p + S_l} \right)^{-1} \quad (11)$$

where the parameter F represents the effects of the Ge:

$$F = \frac{N_{vSi}}{N_{vSiGe}} \exp\left(-\frac{\Delta E_G}{kT}\right) \quad (12)$$

In these equations T_l models tunnelling through the interfacial layer and S_l recombination at the polySiGe/Si interface.

In practical polySiGe emitters, there will be a conflict between increased base current from the presence of the Ge and decreased base current from the interfacial layer. To illustrate this interaction, figure 3 shows a graph of the modelled value of S_{pl} as a function of interfacial layer thickness. In calculating the value of S_{pl} , the parameter values in [6] were used. At high values of interfacial layer thickness, T_l is small and hence $S_{pl} \approx S_l$ in equation 11. Consequently, the Ge in the polySiGe layer has no effect on the value of S_{pl} . At low values of interfacial layer thickness, T_l in equation 11 is large, so S_{pl} approaches a value of $F^{-1}(S_p + S_l) \approx F^{-1} S_p$. In this situation the polySiGe layer has a strong effect on the value of S_{pl} .

3 Transistor Fabrication

Silicon bipolar transistors were fabricated with polySiGe emitters with Ge contents in the range 0 to 33%. The in-situ phosphorus doped poly SiGe layer was deposited at a temperature of 540°C after an ex-situ HF etch. The polySiGe emitter was completed by annealing for 30s at either 900 or 800°C. SIMS measurements were made to characterise the germanium, phosphorus and oxygen profiles in the polySiGe emitter, and Gummel plots were measured to characterise the electrical properties of the resulting bipolar transistors.

4 Results

Figure 5 shows cross-sections of a polySi and a polySi_{0.9}Ge_{0.1} emitter.

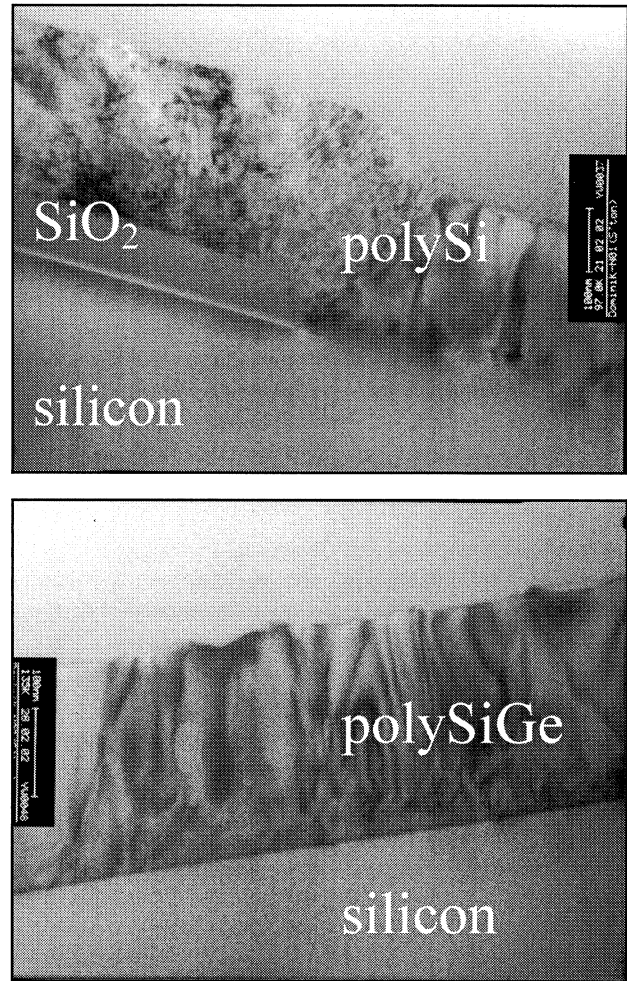


Figure 5: TEM cross-sections of a polySi and a polySi_{0.9}Ge_{0.1} emitter annealed for 10s at 900°C

The grain size in the polySi and polySi₉₀Ge₁₀ emitter device is on average 100nm.

Figure 6 compares measured Gummel plots for transistors with polySi and polySiGe emitters given an anneal of 30s at 900°C. The collector characteristics are ideal with ideality

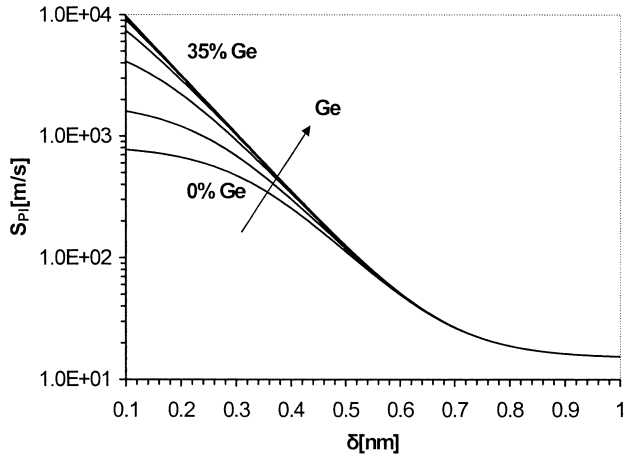


Figure 3: Modelled effective surface recombination velocity S_{PI} as a function of interfacial layer thickness for Ge contents of 0 to 35% in 5% steps.

The base current can be calculated to[7]:

$$I_B = \frac{qAn_{iSi}^2}{\frac{N_{DEFF}W_E}{D_{peSi}} + \frac{N_{DEFF}}{S_{PI}}} \exp\left(\frac{qV_{BE}}{kT}\right) \quad (13)$$

where N_{DEFF} is the effective doping in the single-crystal silicon emitter, W_E is the junction depth and D_{peSi} is the hole diffusivity in silicon.

Figure 4 shows base currents for different interfacial oxide thicknesses. For these simulations a Si emitter thickness of 200nm was assumed. The increase in I_B achieved by Ge incorporation in the polySi emitter is very rapid at low Ge concentrations, but saturates at high Ge concentrations. This is illustrated in figure 4 for thin interfacial oxide layers. For an interfacial oxide thickness of 0.1nm, S_{PI} saturates for Ge concentrations greater than approximately 20%. In practice there is therefore little benefit to be obtained by increasing the Ge concentration above 20%.

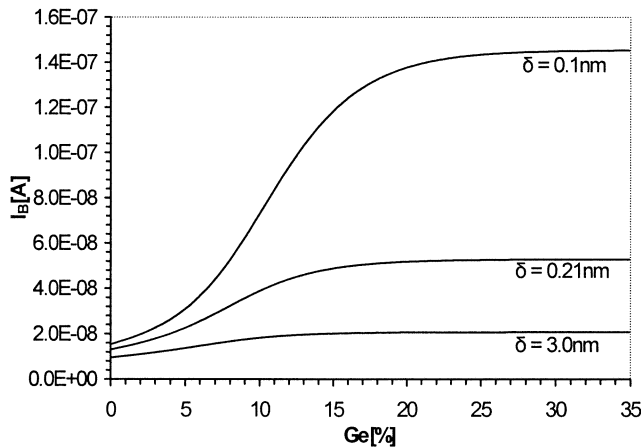


Figure 4: Modelled I_B as a function of Ge content for different interfacial oxide layer thicknesses

factors of 1.07 and the base characteristics near-ideal with minimum ideality factors of 1.20, 1.14 and 1.13 at $V_{BE}=0.6V$ for 0, 10 and 19% Ge respectively. The base current increases with Ge content, rising by a factor of 2.9 on going from 0 to 10% and by a factor of 4.0 on going from 0 to 19%.

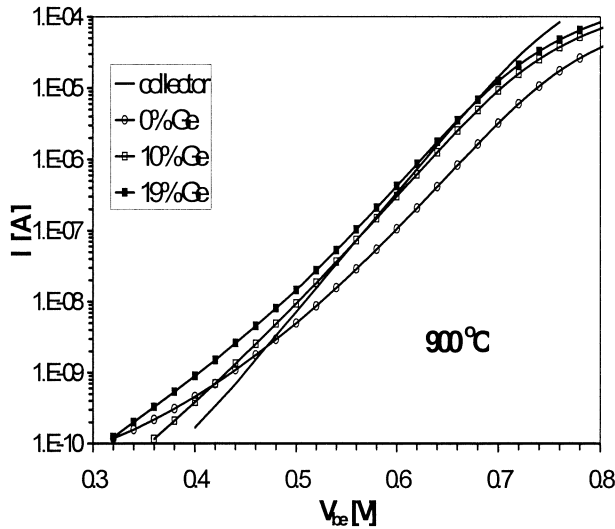


Figure 6: Gummel plots of transistors with polySi and polySiGe emitters annealed for 30s at 900°C.

5 Discussion

In this section a comparison is made of measured and predicted values of base current. SIMS profiles were used to measure the doping and Ge concentration in the polysilicon and the oxygen dose at the polySi/Si interface, from which the interfacial layer thicknesses were calculated. A grain size of 100nm was assumed, as seen in figure 5. The non-ideality of the base characteristics in figure 6 were corrected using the method of Hamel et al. [8].

Table 1 compares the modelled and measured values of base current for three different Ge concentrations.

Ge content	Modelled I_B [A]	Corrected I_B [A]
0%	3.8×10^{-8}	4.2×10^{-8}
10%	7.2×10^{-8}	1.3×10^{-7}
19%	1.6×10^{-7}	1.8×10^{-7}

Table 1: Modelled versus measured base currents

The modelled values of base currents are in excellent agreement with the measured values. Bigger increases in the value of I_B could be obtained by using a thinner interfacial layer. For example, an interfacial layer thickness of 0.1nm would give an increase in I_B by a factor of 8.8 for 20% Ge according to figure 4.

6 Conclusions

A theory has been developed for the base current of a bipolar transistor with polySiGe emitter. The theory is compared with experimental data and gives good agreement. If used in the emitter of a SiGe HBT, the polySiGe emitter could be used to adjust the gain independently of the base profile, and hence optimise the trade-off of gain and BV_{CEO} .

7 Acknowledgement

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8 References

- [1] G.Freeman, D.Ahlgren, D.R.Greenberg, R.Groves, F.Huang, G.Hugo, B.Jagannathan, S.J.Jeng, J.Johnson, K.Schonenberg, K.Stein, R.Volant, S.Subbanna; "A 0.18 μ m 90GHz f_T SiGe HBT BiCMOS, ASIC-compatible, copper interconnect technology for rf and microwave applications"; IEDM Technical Digest (1999)
- [2] J.Böck, T.F.Meister, H.Knapp, D.Zöschg, H.Schäfer, K.Aufinger, M.Wurzer, S.Boguth, M.Franosch, R.Stengl, R.Schreiter, M.Rest, L.Treitingner; "SiGe bipolar technology for mixed digital and analogue RF applications"; IEDM Technical Digest, pp745-748 (2000)
- [3] K.Washio, M.Kondo, E.Ohue, K.Oda, R.Hayami, M.Tanabe, H.Shimamoto, T.Harade; "A 0.2 μ m self-aligned selective epitaxial growth SiGe HBT featuring 107GHz f_{max} and 6.7ps ECL"; IEEE Transactions on Electron Devices, vol 48, pp1989-1994 (2001)
- [4] B.Martinet, H.Baudry, O.Kermarrec, Y.Campidelli, M.Laurens, M.Marty, T.Schwartzmann, A.Monroy, D.Bensahel, A.Chantre; "100GHz SiGe:C HBTs using non-selective epitaxy"; Proc. European Solid State Device Research Conf. pp97-100 (2001)
- [5] J.-h. Sim, C.H.Choi, K.Kim; "Elimination of parasitic bipolar-induced breakdown effects in ultra-thin SOI MOSFETs using narrow-bandgap-sources (NBS) structure"; IEEE Transactions on Electron Devices, vol 42, pp1495-1502 (1995)
- [6] Z.Yu, B.Ricco, R.W.Dutton; "A comprehensive analytical and numerical model of polysilicon emitter contacts in bipolar transistors"; IEEE Trans. Electron Devices, vol 31, p773 (1984)
- [7] P.Ashburn; "Design and realization of bipolar transistors"; pp55, Wiley (1988)
- [8] J.S.Hamel, D.J.Roulston, C.R.Selvakumar; "Experimental Method for Extraction of Emitter Injection Limited Gain in Bipolar Transistors"; Solid-State Electronics vol 35, No 7, pp. 1021-1022 (1992)