Simulation of Device-Structure Dependence of Surface-Related Kink Phenomena in GaAs FETs

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ABSTRACT

The kink (or an abnormal increase in output conductance with the drain voltage) in GaAs FETs can occur due to a space-charge effect originated from generated hole capturing by surface states around the gate. Here, device-structure dependence of kink phenomena in GaAs MESFETs is studied particularly by simulating structures that are intended to reduce the surface-state effects at the source side, such as a recessed-gate structure and a structure with n^+-source region.

Keywords: GaAs MESFET, kink, surface state, impact ionization, recessed-gate structure

1 INTRODUCTION

To understand high-voltage phenomena in GaAs MESFETs and HEMTs, such as drain-to-source breakdown, is very important for realizing high-performance microwave power devices and ICs, which are now receiving great interest, particularly for mobile communication applications. In relation to this, recently, an abnormal increase in output conductance with the drain voltage ("kink") is often observed at relatively low-voltage regions. This phenomenon is unfavorable for power device applications. The kink in GaAs MESFETs was firstly correlated to a sidegating effect [1], and hence it was discussed in terms of substrate-related effects [1]-[4]. On the other hand, the surface-related factors, such as surface states, should also affect the breakdown [5] and the kink phenomena. However, few works have been reported on how the surface properties affect the kink phenomena in GaAs MESFETs [6].

In a previous work [6], we showed that the kink could arise due to impact ionization of holes and the following hole trapping by surface states around the gate. But, it is not clear which side (source or drain) of surface states mainly determine the kink. So in this work, we have studied device-structure dependence of surface-related kink phenomena, particularly by analyzing device structures that are intended to reduce surface-state effects at the source side.

2 PHYSICAL MODEL

Fig.1 shows modeled device structures analyzed here. Fig.1(a) is a simplified planar structure. Fig.1(b) is a recessed-gate structure, where the distance between the gate and the recess edge at the source side L_{rs} is varied as a parameter. For shorter L_{rs}, the surface-state effects at the source side are expected to be smaller. Fig.1(c) is a structure with n^+-source region. In this structure, the surface depletion layer at the source side becomes thinner, so that the surface-state effects are expected to be smaller at the source side.

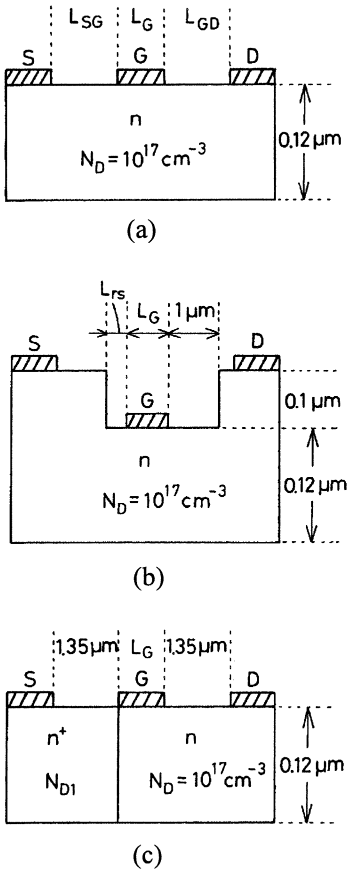

Fig.1 Device structures analyzed in this study. (a) planar structure, (b) recessed-gate structure, (c) structure with n^+-source region.

As a surface-state model, we adopt Spicer's unified defect model [7], and assume that the surface states consist of a pair of a deep donor and a deep acceptor. The surface states are assumed to distribute uniformly within 5 Å from the surface, and their densities are typically set to 10^{13} cm^{-2} (2x10^{20} cm^{-3}). As to their energy levels, the following cases based on experiments are considered as in a previous work [6]:

a) Sample 1: $E_{SD} = 0.925$ eV, $E_{SA} = 0.8$ eV [7],
b) Sample 2: $E_{SD} = 0.87$ eV, $E_{SA} = 0.7$ eV [5],[8]

where E_{SD} is energy difference between the bottom of conduction band and the deep donor's energy level, and E_{SA} is energy difference between the deep acceptor's energy level and the top of valence band.

Basic equations to be solved are Poisson's equation, continuity equations for electrons and holes and rate equations for the deep levels [6],[9]. They are expressed as follows.

1) Poisson's equation

$$\nabla^2 \psi = -\frac{q}{\varepsilon}(p - n + N_D + N_{SD}{}^{+} - N_{SA}{}^{-}) \tag{1}$$

2) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n + G - (R_{n,SD} + R_{n,SA}) \tag{2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \bullet J_p + G - (R_{p,SD} + R_{p,SA}) \tag{3}$$

where

$$R_{n,SD} = C_{n,SD} N_{SD}^{+} n - e_{n,SD}(N_{SD} - N_{SD}^{+}) \tag{4}$$

$$R_{n,SA} = C_{n,SA}(N_{SA} - N_{SA}^{-})n - e_{n,SA} N_{SA}^{-} \tag{5}$$

$$R_{p,SD} = C_{p,SD}(N_{SD} - N_{SD}^{+})p - e_{p,SD} N_{SD}^{+} \tag{6}$$

$$R_{p,SA} = C_{p,SA} N_{SA}^{-} p - e_{p,SA}(N_{SA} - N_{SA}^{-}) \tag{7}$$

3) Rate equations for the deep levels

$$\frac{\partial}{\partial t}(N_{SD} - N_{SD}{}^{+}) = R_{n,SD} - R_{p,SD} \tag{8}$$

$$\frac{\partial}{\partial t} N_{SA}{}^{-} = R_{n,SA} - R_{p,SA} \tag{9}$$

where $N_{SD}{}^{+}$ and $N_{SA}{}^{-}$ represent ionized densities of surface deep donors and surface deep acceptors, respectively. C_n and C_p are the electron and hole capture coefficients of the deep levels, respectively, e_n and e_p are the electron and hole emission rates of the deep levels, respectively, and the subscript (SD, SA) represents the corresponding deep level.

G represents a carrier generation rate by impact ionization, and is expressed as

$$G = (\alpha_n \mid J_n \mid + \alpha_p \mid J_p \mid)/q \tag{10}$$

where α_n and α_p are ionization rates for electrons and holes, respectively, and are given by [10]

$$\alpha_n = A_n \exp\{-(B_n / \mid E \mid)^{1.6}\} \tag{11}$$

$$\alpha_p = A_p \exp\{-(B_p / \mid E \mid)^{1.75}\} \tag{12}$$

where E is the electric field. A_n = 2.994x10^5 cm^{-1}, A_p = 2.215x10^5 cm^{-1}, B_n = 6.848x10^5 V/cm and B_p = 6.570x10^5 V/cm [10].

The above equations are put into discrete forms and are solved numerically.

3 PLANAR STRUCTURE

Fig.2 shows an example of calculated drain characteristics of the planar GaAs MESFET with the gate length L_G of 0.3 μm. Here, the Sample 1-type surface states are assumed, and their densities are 10^{13} cm^{-2}. The kink arises due to impact ionization. Because the gate current is lower than the drain current by two or three orders of magnitudes, the increase in drain current is not due to direct gate breakdown but due to a space-charge effect originated from generated hole capturing by surface states around the gate [6]. When the gate voltage V_G becomes positive, the onset voltage for the kink seems to become higher. This is because when V_G is positive, the barrier at the Schottky gate is lowered, and hence an energy barrier is formed at the interface between the gate and the surface-state layer.

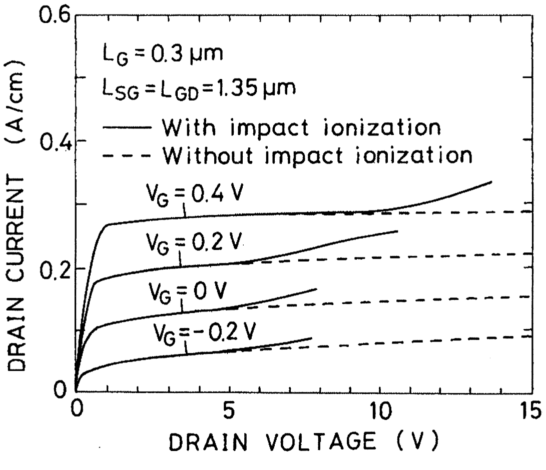

Fig.2 Example of calculated drain characteristics of planar GaAs MESFET. L_G = 0.3 μm.

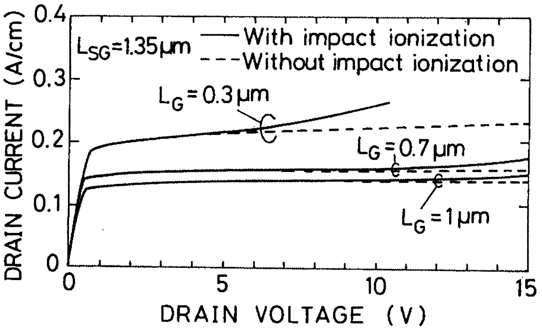

Fig.3 Calculated I_D-V_D curves of planar GaAs MESFETs as a parameter of L_G.

Fig.3 shows calculated drain characteristics of the planar GaAs MESFETs as a parameter of L_G. As L_G becomes longer, the onset voltage for the kink becomes higher and the kink behavior becomes weaker. These are because for longer L_G, generated holes between the gate and the drain are absorbed into the gate, and do not reach the surface-state layer between the gate and the source, resulting in weaker surface-state effects at the source side.

4 STRUCTURES WITH LESS SURFACE-STATE EFFECTS

Here, we describe cases for the structures expected to have less surface-state effects. First we treat a recessed-gate structure shown in Fig.1(b). In the recessed-gate structure, effects of surface states on the same planes as the source (drain) electrode should become smaller as the recess depth becomes deeper. In this study, to study the surface-state effects at the source side, the distance between the gate and the recess edge at the source side L_{rs} is varied as a parameter. Fig.4 shows calculated drain characteristics of recessed-gate GaAs MESFETs as a parameter of L_{rs}. Here the Sample 2-type surface states are assumed, and their densities are 10^{12} cm^{-2}. It is seen that the onset voltage for the kink is not so much affected by the values of L_{rs}, but the increase rate of drain currents due to impact ionization becomes relatively small for shorter L_{rs}. This is because the surface-state effects at the source side are weakened for shorter L_{rs}.

Next, we discuss a structure shown in Fig.1(c), where an n^+-region is formed at the source side. In this structure, the surface depletion layer due to surface states becomes thinner in the n^+-region, so that the surface-state effects are expected to be smaller. Fig.5 shows calculated drain characteristics of the structure with n^+ source as a parameter of its donor density N_{D1}. As N_{D1} becomes higher, the onset voltage for the kink becomes higher. This is understood that the surface-state effects at the source side are weakened for higher N_{D1} because of the thinner surface depletion region.

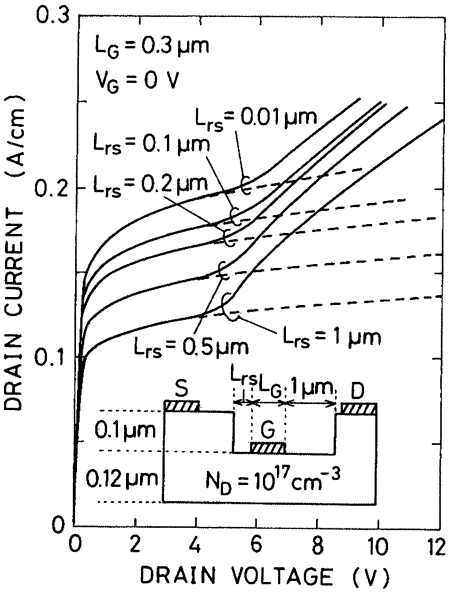

Fig.4 Calculated I_D-V_D curves of recessed-gate GaAs MESFETs as a parameter of L_{rs}.

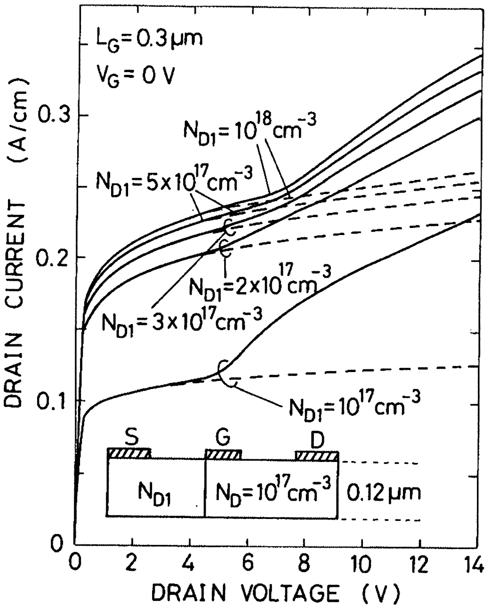

Fig.5 Calculated I_D-V_D curves of a structure with n^+-source region as a parameter of its donor density N_{D1}.

In the above structures, the kink behavior is shown to be weakened, as expected. However, we can't say that the kink is suppressed so significantly. This may indicate that carrier generation at the gate-to-drain region is primarily important in the kink phenomena.

5 CONCLUSION

Device-structure dependence of surface-state-related kink phenomena in GaAs MESFETs has been studied by two-dimensional simulation. It has been shown that in the planar structure the kink becomes weakened for longer gate length, because the surface-state effects at the source side are weakened. Structures expected to have less surface-state effects at the source side, such as the recessed-gate structure and the structure with n^+-source region, have also been simulated. The kink behavior has been weakened also in these structures, but the suppression of kink is not so significant, indicating that carrier generation at the gate-to-drain region may be primarily important in the kink phenomena.

REFERENCES

[1] A. Harrison, "Backgating in submicrometer GaAs MESFET's operated at high drain bias", *IEEE Electron Device Lett.*, vol.13, pp.381-383, 1992.

[2] K. Horio and K. Satoh, "Two-dimensional analysis of substrate-related kink phenomena in GaAs MESFET's", *IEEE Trans. Electron Devices*, vol.41, pp.2256-2261, 1994.

[3] M. R. Wilson, P. Zdebel, P. Wennekers and R. Anholt, "Understanding the cause of IV kink in GaAs MESFET's with two-dimensional numerical simulation", in *Proceedings of GaAs IC Symposium*, 1995, pp.109-112.

[4] J. Haruyama, H. Negishi, Y. Nishimura and Y. Nashimoto, "Substrate-related kink effects with a strong light-sensitivity in AlGaAs/InGaAs PHEMT", *IEEE Trans. Electron Devices*, vol.44, pp.25-33, 1997.

[5] C. L. Li, T. M. Barton and R. E. Miles, "Avalanche breakdown and surface deep-level trap effects in GaAs MESFET's", *IEEE Trans. Electron Devices*, vol.40, pp.811-816, 1993.

[6] K. Horio and A. Wakabayashi, "Numerical analysis of surface-state effects on kink phenomena of GaAs MESFETs", *IEEE Trans. Electron Devices*, vol.47, pp.2270-2276, 2000.

[7] W. E. Spicer, P. W. Chye, P. R. Skeath, C. Y. Su and I. Lindau, "New and unified model for Schottky barrier and III-V insulator interface states formation", *J. Vac. Sci. Technol.*, vol.16, pp.1422-1433, 1979.

[8] H. H. Wieder, "Surface Fermi level of III-V compound semiconductor-dielectric interfaces", *Surface Sci.*, vol.132, pp.390-405, 1983.

[9] Y. Mitani, D. Kasai and K. Horio, "Analysis of surface-state and impact-ionization effects on breakdown characteristics and gate-lag phenomena in narrowly-recessed-gate GaAs FETs", *IEEE Trans. Electron Devices*, vol.50, no.1, 2003.

[10] G. E. Bulman, V. M. Robbins, K. F. Brennan, K. Hess and G. E. Stillman, "Experimental determination of impact ionization coefficients in (100) GaAs", *IEEE Electron Device Lett.*, vol.EDL-4, pp.181-185, 1983.