Single Transistor AND Gate

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ABSTRACT

In pass-transistor logic circuits, an AND gate is implemented by two MOSFETs in series. We believe that it can be replaced by a single double-gate SOI MOSFET, in this way we can reduce the gate delay, and also shrink the area at the same time. Furthermore, this implementation is not limited to the pass-transistor AND gate, it applies to any CMOS logic circuits with stacking transistor structures, such as NAND, NOR and XOR.

1 INTRODUCTION

SOI MOSFET has many advantages over bulk MOSFET, such as lower parasitic capacitances, radiation hardness, less short-channel effect, low power, high temperature and compatibility with lower voltage supplies [1-5]. Furthermore, the double-gate SOI structure opens a door for many novel devices by the coupling of the two gates [6]. If the silicon film is very thin, the depletion regions from the front and back gates can merge at certain applied gate bias. Therefore, the threshold voltage depends on the bias voltages of the two gates. If the same voltage is applied to both gates simultaneously, the depletion regions are equally partitioned; a threshold voltage can be obtained as V_{tdg}. On the other hand, if the voltage is applied only to one gate, and keeping the other gate grounded (for NMOS), the two depletion regions are asymmetric; therefore, the threshold voltage V_{tsg} is larger than V_{tdg}. The SOI can be designed in a way such that the double-gate threshold voltage V_{tdg} is less than V_{dd} and the single-gate threshold voltage V_{tsg} is greater than V_{dd}. If the two gates are connected with two logic inputs (A and B), the conducting condition of this gate is that both A and B are high. In this way, an AND pass-transistor logic gate is implemented with a single transistor.

2 SIMULATION AND ANALYSIS

A simplified double-gate NMOS structure is investigated: the active silicon layer is uniformly doped to 10^{17} cm^{-3}, and a symmetric structure is assumed, i.e. the gate oxide layer and the n^+ poly-gate are identical on both sides. One of the critical parameters in determining the threshold voltage is the oxide thickness, which is simulated in the range from 10 nm to 100 nm. In the device structure of our design, there is a correlation between the thickness of the silicon film and that of the gate oxide. Their relationship is determined in the following way: when one gate is grounded and the other one is biased to V_{tsg}, which is the conventional threshold voltage, the two depletion regions come in contact. Therefore, the thickness of the silicon film is designed to be equal to the sum of the two depletion regions; the simulated result is shown in Fig. 1.

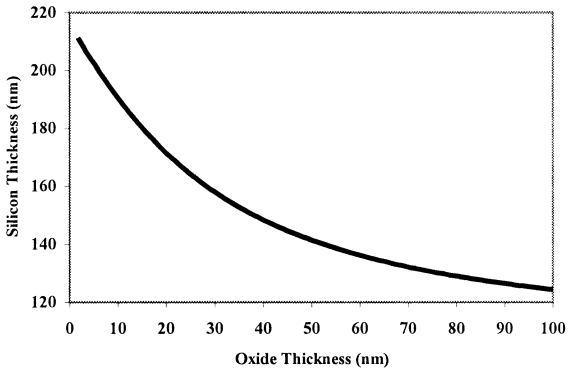


Fig. 1 Correlation between silicon film and oxide.

Now let the two gates be shorted together and a common gate bias is applied. There are three distinctive stages in the process of increasing the bias. In the first stage, the depletion regions keep approaching each other symmetrically at the center of the silicon film. At $V_g=V_{fd}$ the two depletion regions meet at the middle of the silicon layer. However, the surface potential is smaller than that required to form a conducting channel, i.e. $\phi_s < 2\phi_{fp}$. This situation is illustrated in Fig. 2. Up to this point the applied gate bias can be divided into two parts: one part contributes to the change of the surface potential, and the other part to the increased electric field in the oxide. With further increased gate bias it enters the second stage, where the silicon film is fully depleted and the inversion charge is negligible. Therefore, the shape of the band profile of the silicon film will not change; neither does the electric field in the oxide. The only response is that the level of the whole frozen band profile shifts following the increased gate bias.

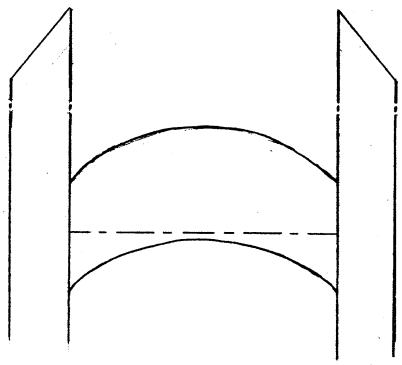


Fig. 2 Band profile of a completely depleted double-gate SOI MOSFET.

When $\phi_s = 2\phi_{fp}$ it comes to the third stage, where considerable inversion charge begins to populate the conducting channels. In this case the increased gate bias causes the electric field in the oxide to increase, as well as the carrier concentration in the conducting channels.

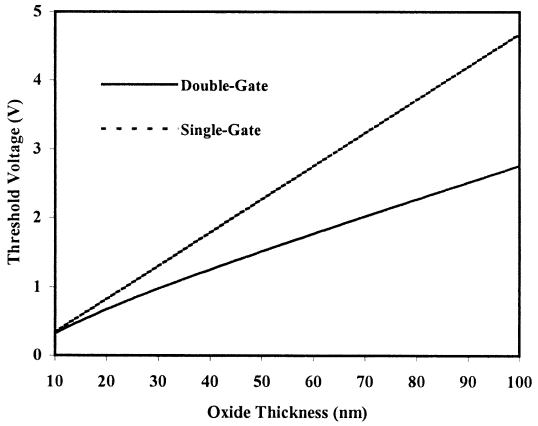


Fig. 3 Threshold voltage of double-gate and single-gate SOI MOSFETs.

Fig. 3 shows the simulated result. The solid line stands for the threshold voltage when bias is commonly applied to the double-gate; and the dashed line corresponds to the threshold voltage when the bias is applied to a single gate, while leaving the other one grounded. In the case with 60 nm oxide, V_{tsg} = 2.75V, and V_{tdg} = 1.77 V. Let's set the power supply voltage to be V_{dd}=2.3V, the MOSFET can be turned on if V_{dd} is applied to both gates, and it is still in the off-state if V_{dd} is applied to only one gate. In this way the pass-transistor AND function is realized. However, the required power supply voltage is higher than that in the current technology. If the oxide thickness is reduced to 30 nm, V_{tsg} = 1.30V, and V_{tdg} = 0.98 V, the required power supply voltage is then lowered to V_{dd}=1.15V.

3 APPLICATIONS

This AND gate can be used in any circuit that has a series conbination of two MOSFETs of the same type. The simplest examples are the NAND and NOR gates, which have the series combination of NMOS and PMOS transistors, respectively. Fig. 4 shows these gates that are implemented with the double-gate MOSFETS.

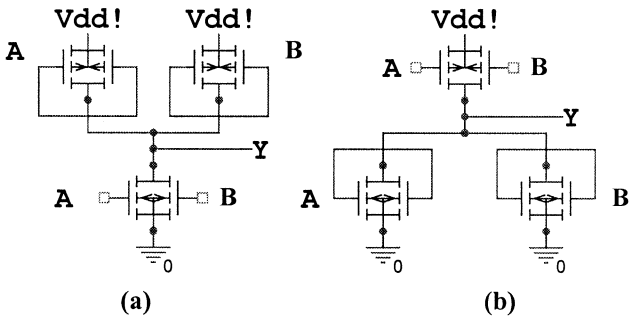


Fig. 4 Double-gate MOSFET NAND gate (a) and NOR gate (b).

In circuit (a) the pull-down network is replaced with a sigle double-gate MOSFET; while in circuit (b) the pull-up network is implemented with a sigle double-gate MOSFET. This new circuit structure can simplify designs and enhance the performance, especially in the case where a long chain of series MOSFETs is involved. Fig. 5 shows a NOR gate with four inputs.

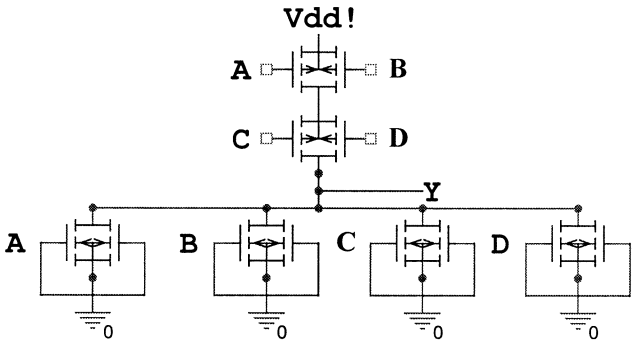
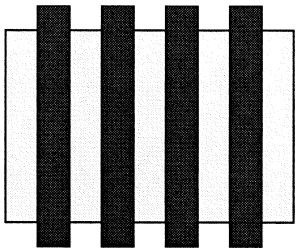


Fig. 5 A NOR gate with four inputs.

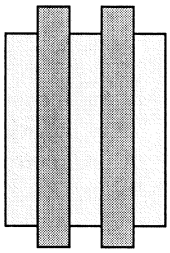
The conventional NOR gate with four inputs need four P-MOSFETs in series; this weak pull-up structure can cause large delay. With the double-gate MOSFET the length of

the series transistor chain can be cut by half, the performance can be enhanced considerably in this way.

The layouts of the pull-up network of the NOR gate with four inputs are depicted in Fig. 6; part (a) is the layout implemented with conventional MOSFETs and part (b) is that with the double-gate MOSFET scheme. From this layout it is obvious that the double-gate scheme occupies less area than the conventional layout. However, there is some overhead with the double-gate scheme, the interconnection to the bottom gate also takes some area.



(a)



(b)

Fig. 6 (a) Layout in bulk CMOS process,
(b) Layout in double-gate process.

4 DISCUSSION

This design and analysis is only limited to the concept stage, there are many issues needed to be taken into account before it can be successfully implemented. First of all, there are severial different device structures of advanced SOI MOSFETs [7,8], which are under active research. The double-gate MOSFET structure for this single transistor AND gate suffers from the problem of higher cost from the complexity of fabrication. On the other hand, the process tolerance of this proposed device structure is pretty low, as it requires accurate control of the thicknesses of the gate oxides and silicon layer. However, the emanation of SOI material offers a rich variety of nonconventional device structures [9]. It is not only an extension of the conventional MOSFET, but also its new characeristics and functionalities provide us the opportunity to investigate noval circuit configurations.

5 CONCLUSION

A pass-transistor AND function is implemented with a single double-gate SOI MOSFET. It is illustrated that this device can be applied to conventional NAND and NOR gates; but it can also be applied in many logic circuits. Especially in the situations when a long chain of series MOSFETs is needed. With this implementation, the chip area and gate delay can be reduced significantly at the same time.

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