Design Optimization of Micromachined High Aspect Ratio 3D On-chip Solenoid Inductor

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ABSTRACT

This paper presents the simulation works done by using *Sonnet EM™* on high-aspect-ratio 3D on chip solenoid inductor. In order to discover the dependence of inductor performance on different dielectric materials covering the substrate, via heights, via separation distances, conductor dimensions, a variety of designs have been demonstrated and their behaviors under different circumstances have been characterized. In conclusion, we found that high-aspect-ratio 3D solenoid inductors provide better RF performance than previously fabricated low-aspect-ratio 3D solenoid and dome-shape spiral inductors.

Keywords: optimization, high-aspect-ratio, 3D, solenoid, inductor

1 INTRODUCTION

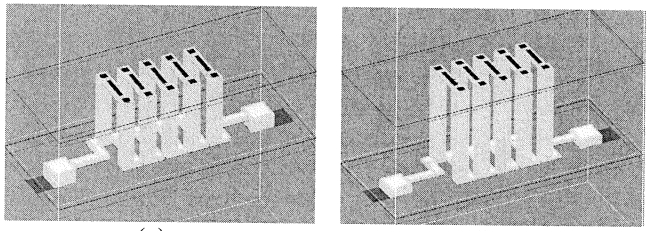
Recently, there have been many investigations in the micromachining research community to realize on-chip passive components for radio frequency (RF) applications. We have worked on micromachined inductors including 3D arch-shape air-core solenoid inductors and dome-shape spiral inductors [1,2]. The measured peak Q factor values for 2- ~ 5-turn arch-shape inductors are in the range of 15 ~ 18, with effective inductances in the range of 0.6 ~ 0.8nH. Spiral inductors offer higher inductances and Q values, but they occupy relatively larger area than solenoid inductors.

In order to realize on-chip inductors with smaller chip area, larger inductance, higher Q factor and self-resonant frequency (SRF), the design of the conventional solenoid inductor has to be optimized. Several key factors will affect inductor's performance at ultra high frequency (GHz) range, which include ohmic loss of conductors, skin effect, parasitic capacitances [3], and Eddy current loss in substrate [4].

In this paper, we propose high aspect ratio 3D air-core solenoid inductor geometry for improved RF performance and we report the simulation works done by using *Sonnet EM™* for such inductors. Fabrication of such inductors is currently under way.

2 INDUCTOR SIMULATION

Extensive simulation works were carried out using *Sonnet EM™* on high aspect ratio (4:1 and 8:1) on-chip air-core solenoid inductors. Figure 1 shows a drawing of 5-turn high aspect ratio solenoid inductor used in *Sonnet EM* simulation. We have simulated different inductor structures to understand the dependence of inductor performance on the number of turns, via height, separation distance between the vias of adjacent turns, and the isolating material used. Material used in the simulation is same as those of previously fabricated inductors by authors that use copper as conductors, and silicon wafer as substrate [1,2].



(a) (b)

Figure 1. Drawing of 5-turn high aspect ratio inductors used in Sonnet EM™ simulation: (a) 4:1; and (b) 8:1 ratio

2.1 Number of Turns

To understand the effect of the number of turns on inductor characteristics, simulations of 2- ~ 8-turn inductors built on 30μm thick BCB (benzocylobutene, $\varepsilon_r \approx 2.65$) isolation layer were carried out. Peak Q factor, inductance, and SRF for each inductor were extracted.

The simulation results show that with increasing number of inductor turns, Q factor and SRF decrease, while inductance values increase in a rather linear manner (Figure 2). Increasing number of turn means longer conducting

path, which causes higher series resistance and consequently more electrical energy dissipation. Also, enlarged conductor-to-conductor area induces higher series capacitance and larger conductor bottom contact area with the substrate would increase Eddy current losses as well.

Although inductor with more turns has higher inductance and capacitance values will have lower SRF, it does not represent an exact parabolic decay as the theoretical formula indicates. In conclusion, if all other conditions (substrate material, via height, conductor dimension, etc.) remain the same, increase in the number of inductor turns will enhance the inductance but lower the Q factor and SRF.

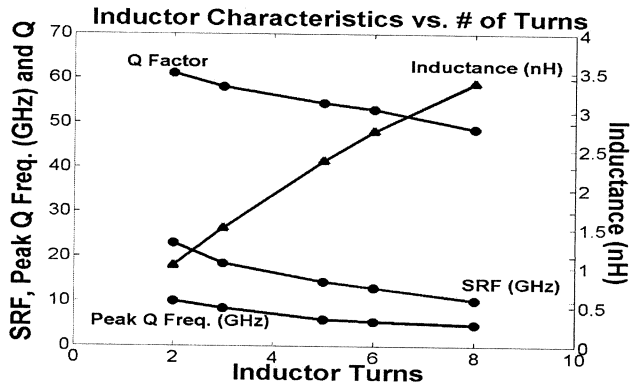


Figure 2. Plot of inductor characteristics as a function of inductor turns

2.2 Dielectric Layers

In our previous work [1,2], inductors were suspended in air with an assumption that air gap would enhance the RF performance. We investigated this effect by applying different dielectric materials including air ($\varepsilon_r = 1$), BCB (benzocylobutene, $\varepsilon_r \approx 2.65$), and spin-on glass ($\varepsilon_r \approx 3.9$) underneath the inductor. Simulations of 2- ~ 5-turn inductors with 200 and 400μm tall via and dielectric material thickness of 30μm have been completed (Figure 3, 4). As expected, the data drawn have demonstrated that Q factors and SRF would drop with higher dielectric constant of the isolation material. This is due to the fact that higher dielectric constant would create more undesired electric fields to be linked to the substrate, which results in higher Eddy current to flow in the substrate. From Figures 3 and 4, both Q factor and SRF decrease in a linear behavior with increasing ε_r. From this, we can infer that an inductor suspended in air would enhance RF performance than those sitting directly on common dielectric materials, but the amount of improvement will not be significant, 7.1 % in Q factor and 9.8 % in SRF when compared to inductors sitting on spin-on-glass.

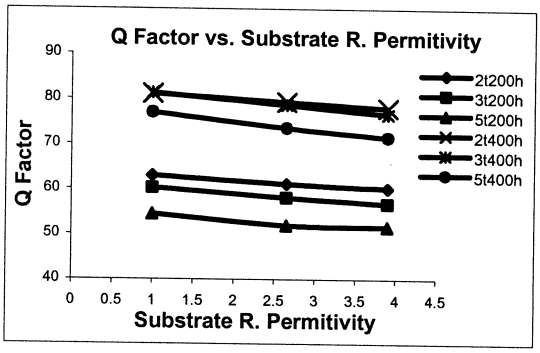


Figure 3. Plot of Q factor as a function of dielectric layer relative permitivity

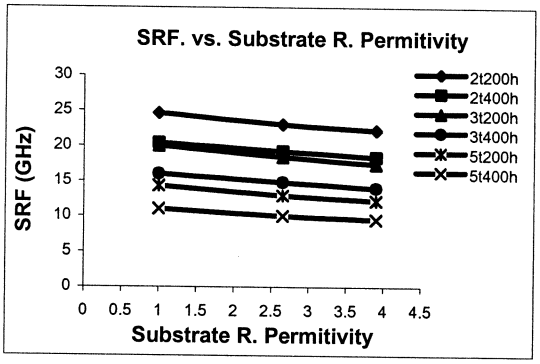


Figure 4. Plot of SRF as a function of dielectric layer relative permitivity

2.3 Air Gap Distance

Another set of simulation has been carried out to quantize the effect of different air gap separation distances between the inductor and the substrate in order to achieve the desired performance. Simulations on a 3-turn solenoid inductor with various air-gap distances in the range of 0-100μm have been performed. The simulated inductor characteristics are shown in Figure 5. It can be observed that inductor with no air-gap has lower Q value than those suspended in air. Nonetheless, major characteristics of the inductor are not improved much as the separation distance increases. From this plot, we can conclude that, for 3-turn inductor with 200μm tall vias, the 10μm air gap is sufficient to minimize the Eddy current loss in the substrate and the capacitive effect between the structure and the substrate. Similarly, simulations are underway to determine the optimal thickness of dielectric layers other than air.

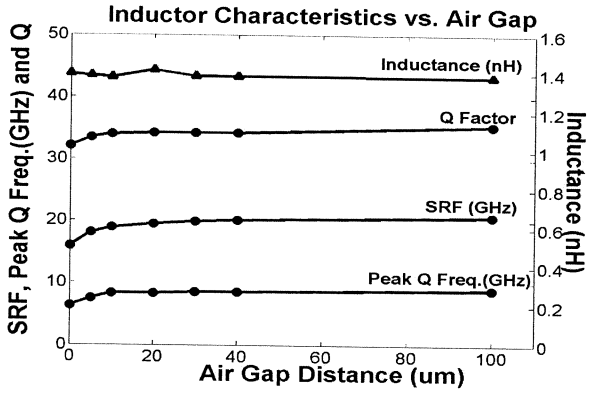


Figure 5. Plot of inductor characteristic as a function of air gap distance

2.4 Via Heights

Simulations were also performed to observe the dependence of the inductor characteristics on via heights. A 2-turn inductor, suspended 30μm in air, with various via heights of 100 ~ 400μm were simulated. It was observed that Q factor and inductance grow while SRF and peak Q frequency decrease linearly with increase in via height (Figure 6). The increase in the Q factor and inductance can be attributed to the fact that an increased via height results in an increased core size and consequently in an increase in the magnetic flux linkage between the inductor turns. This also results in the gradual decrease in the SRF.

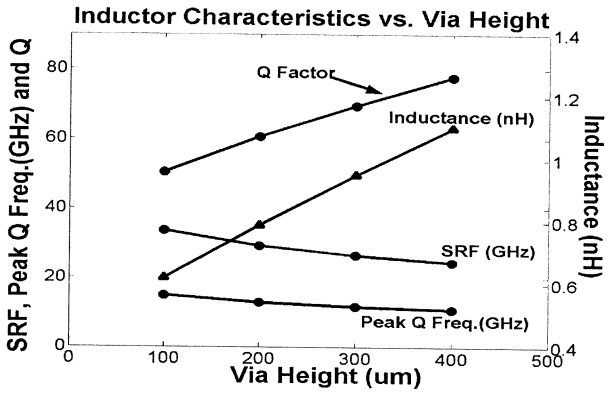


Figure 6. Plot of inductor characteristics as a function of inductor's via height

2.5 Via Separation Distance

The distance between vias of adjacent turns also presents an interesting case to study. Simulations were carried out with varying via separation distances ranging from 30 to 140μm. From the data plotted, we observe an increase in the Q factor and inductance (~10%) when vias were spaced closer to each other (Figure 7). These were due to the increase in the mutual coupling between the adjacent turns of the inductor. The marginal increase in the Q factor and inductance value is because of the increase in the series resistance due to the proximity effect which causes mutually induced Eddy currents between adjacent turns. There was also a slight increase in the SRF, because of the decrease in the capacitance between the adjacent turns. Also, as via distance goes above 90μm, we observe that the reduction in inductance value is quite negligible, since, with this separation, it would be the self-inductance of the conductor that contributes most to the total inductance.

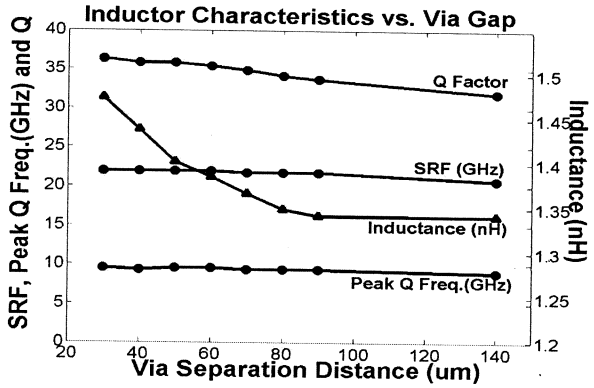


Figure 7. Plot of inductor characteristics as a function of via separation distance

3 OPTIMAL INDUCTOR GEOMETRY

Having observed the effects of various individual factors, simulations were performed to decide the optimal geometry for the 3D air core on-chip solenoid inductor. In these designs, 30μm thick BCB was used as the isolation layer, the conductor thickness and width were 20μm and via dimension was 30×20μm. With a given core area of 0.04 mm^2, the length, width and height of the inductor core were varied.

In the first layout (Figure 8*a*), both via height and the core length were 200μm and the separation between the vias was 10μm. The geometry provides relative higher Q factor and SRF due to the factors discussed above, such as relative tall vias and condensed turns (Figure 9).

In the second layout (Figure 8*b*), via height was changed to 400μm and the core length was 100μm. As we observed before, the increased via height resulted in higher inductance and Q factor (Figure 9, 10).

In the third layout (Figure 8*c*), via height and the core length were 200μm but the distance of via separation was increased to 50μm. As expected from the previous deductions, decreased the mutual coupling between the turns causes reduction in the inductance but the Q factor remains in a similar level. We also observe that this yields slightly better SRF among four layouts, since the total capacitance, the sum of the conductor-to-conductor capacitance and conductor to substrate capacitance, is reduced.

In the final layout (Figure 8*d*), via height was 100μm while the core length was 400μm. The longer core length caused a notable decrease in the Q factor due to the increased interference of the flux with the substrate, as more area of the bottom conductor is exposed to the substrate. The increase in the total capacitance led to the substantial decrease in the SRF for this geometry. However, the longer length of the conductor caused increase in the mutual coupling and thus enhanced inductance.

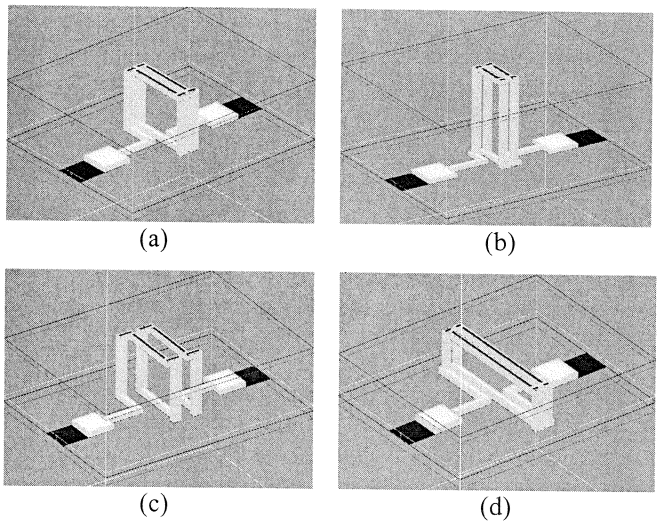


Figure 8. 2-turn inductor with different geometry with same core cross sectional area of 0.04mm² (a) 200×200μm; (b) 100×400μm; (c) 200×200μm, via distance 50μm; and (d) 400×100μm conductor length and via height

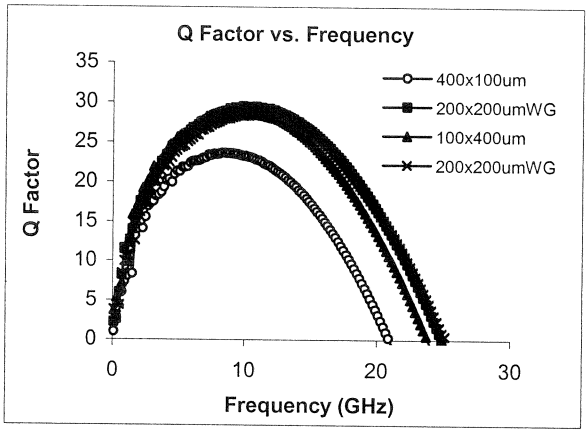


Figure 9. Plot of Q factor as a function of frequency for different layouts above

From these observations it can be summarized that layout in Figure 8*b* yielded the best RF performance. Hence, we conclude that the second layout is highly suitable for RF applications that require both high Q factor and SRF.

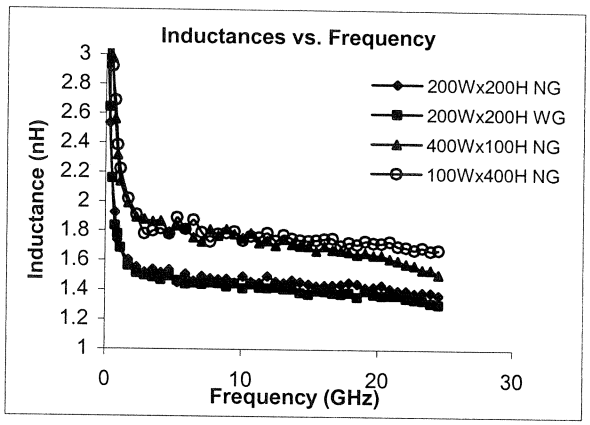


Figure10. Plot of inductance as a function of frequency for different layouts above

4 CONCLUSION

The dependence of inductor performance on various factors related to design, materials used and geometry was studied from simulations done using Sonnet. It was found that increasing the number of turns increased the inductance linearly and decreased the SRF and the Q-factor. An inductor suspended in air over the substrate was observed to have a better Q-factor and SRF compared to those built on the substrate or on other materials with higher dielectric constant. In the case of air as the dielectric material, a 30um gap was found sufficient to obtain the desired improvement in the Q-factor. Increase in the via height was found to increase the Q-factor and the inductance value and this motivated us to propose that High Aspect Ratio inductors with tall via structures are more suited for high performance RF applications than other geometries which have the same core area, but different core heights and lengths.

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