Very Large Scale Integration of MOEMS Mirrors, MEMS Angular Amplifiers and High-voltage, High-density IC Electronics for Photonic Switching

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ABSTRACT

The demand for communication bandwidth together with advances in MEMS (micro-electro-mechanical systems) technology has spurred rapid development in the field of MOEMS (micro-optical-electrical mechanical systems). One exciting opportunity is in the area of photonic switching. MOEMS mirror arrays are being used at the core of all-optical cross-connects, enabling switches that are "transparent" to network protocols, wavelengths, and bandwidth requirements. Advanced vertical integration techniques at the wafer level have been developed to enable the scalability of these arrays to support high port-count (>4096), low-cost photonic switches.

Keywords: MOEMS, MEMS, photonic switching, optical, mirror, telecom

1 INTRODUCTION

One critical factor affecting the ability to develop larger port-count switches is the scalability of the MOEMS mirror array. As the number of mirrors in an array grows by x, the number of control lines grows by nx, where n is the number of control signals for each mirror (typically 3 or 4). Passive array technology does not scale well beyond 128-256 mirrors because the density of interconnects and bond pads becomes impractical. Additionally, the space and power requirements of external drive electronics makes it difficult to design a compact, cost effective system that is appealing to the customer.

To address the need for scalable technology, Transparent Networks (Milpitas, CA) has developed a series of techniques to enable the fabrication of a highly integrated MOEMS mirror array. They are the vertical integration of a mechanical amplifier, an augmentation of a standard CMOS foundry process, and the integration of the MEMS array with the CMOS driver at the wafer level.

The first array developed based on this approach was a 1200 mirror configuration, integrating on a single chip 4800 15-bit D/A converters with a serial interface and 4800 MEMS based angular amplifiers with a gain greater than 4, reducing the electrostatic drive requirement to 120V for a 1x1 mm mirror with ±8° tilt.

2 MEMS ANGULAR AMPLIFIER

The MOEMS mirrors are fabricated in a bulk micromachining process. In addition to some of the inherent advantages of bulk micromachining such as the high fracture stress of silicon, lack of fatigue during actuation, minimal thermal mismatch of materials, etc., the bulk process enables the vertical integration of Transparent's unique virtual pivot design, the Nasiri platform [1].

Unlike some other mirror drive designs such as dual-gimbal suspension [2,3] or in-plane comb drives [4,5] that require a large amount of expensive chip real estate, the Nasiri platform fits almost entirely under the area of the mirror itself. This leads to a great advantage in the packing density of the mirror as shown in Figure 1.

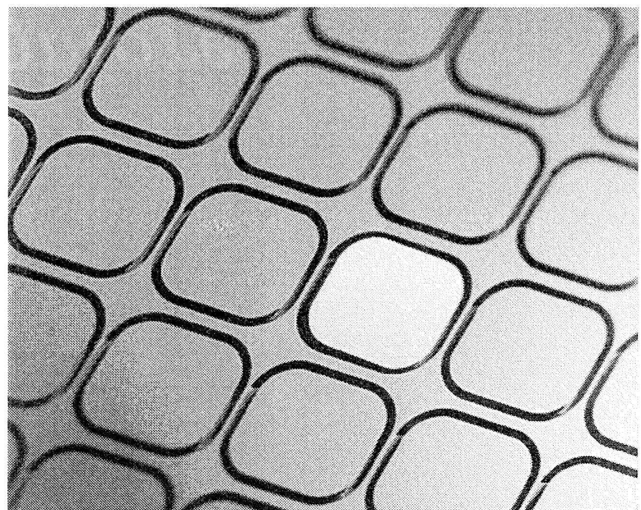

Figure 1 - High density, highly scalable MOEMS mirror array

The Nasiri platform is fabricated in a single bulk silicon layer. The MEMS structure incorporates the electrostatic torsional actuator and a mechanical linkage that forms a virtual pivot at the base of the mirror. By controlling the configuration of the mechanical linkage, it is possible to design it as a mechanical angular amplifier where the mirror tilt is amplified by some factor greater than that of the actuator. In the current revision, the amplification factor is greater than 4. This proportionally reduces the drive

voltage required for a desired angle range of the mirror. In the current design, the mirror moves ±8° over the 120-volt range of the standard HV-CMOS process (Figure 2) and a 3σ distribution of the MEMS processes.

Another advantage of this structure is that the specific configuration of the linkage can be tailored to shape the dynamic response of the mirror. Extensive use of modeling and finite element analysis has enabled exploration of the linkage dependencies. Parameters such as qualify factor, resonant frequency, and compliance can be selected within the attainable design space.

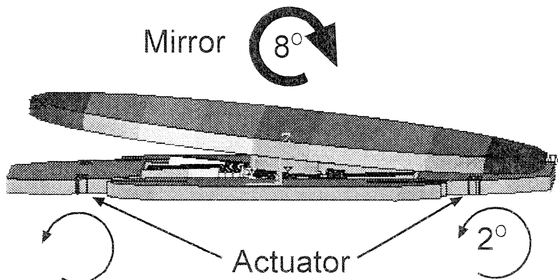

Figure 2 - Image of mirror over Nasiri platform. The virtual pivot, spring structure amplifies the deflection of the mirror relative to the actuator.

In the TNI process, first the mirror structures are defined in bulk silicon using one or more steps of deep reactive ion etching (DRIE). Shown in Figure 3 is the backside of the mirror array.

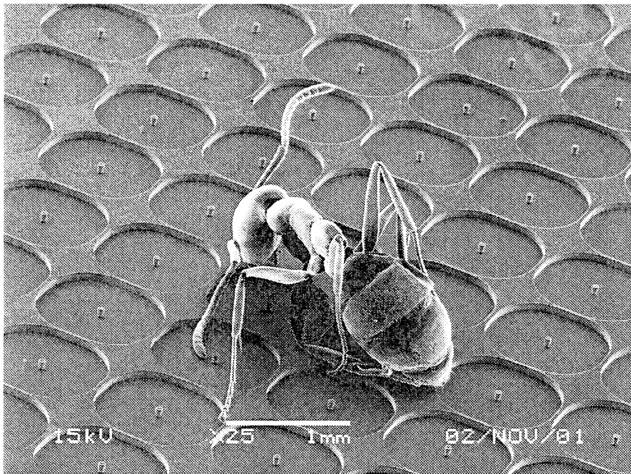

Figure 3 – TNI lab technician puts finishing touches on the backside of a mirror.

The mirror wafer is then fusion bonded to a second wafer, the actuator wafer. The actuator wafer is reduced to the desired thickness using a custom grind and polish. Metal is deposited to facilitate the wafer bonding (described below), and then a DRIE is used again to pattern the actuator, mechanical linkage/amplifier and mirror base structures.

After the mirror array has been bonded to the CMOS layer, the mirror surface is thinned down in the same manner as the actuator. The mirror surface is then coated and patterned with a reflective metal layer (Ti/Au) that has been stress controlled to minimize mirror curvature. Finally the mirror is released by DRIE

It should be pointed out that it is necessary to optimize each DRIE recipe individually. Each step has a different primary specification such as uniformity, precision, or substrate heating, and the etch recipe used must be tailored to meet that requirement.

3 INTEGRATED DRIVE ELECTRONICS

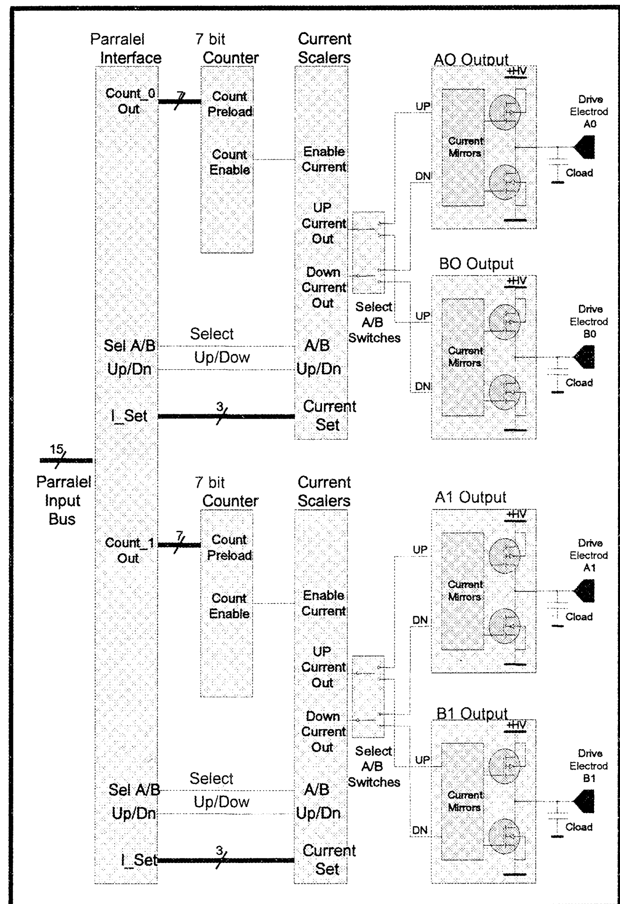

Figure 4 - Mirror Drive Cell

The block diagram for the mirror drive cells is shown in Figure 4. Each cell contains high voltage drive transistors that can either charge or discharge the output capacitor. One pair of output drivers controls the mirror's horizontal axis, and the other controls the vertical axis. Charging of the horizontal axis is done for the first half-cycle of the 10kHz update rate, while charging of the vertical axis takes place during the second half-cycle.

Selected drive architecture enabled using high voltage transistors operating only in the ON or OFF state, significantly reducing power consumption. The entire chip dissipates only 1 W. The temperature increase due to self-heating is only a fraction of a degree centigrade.

The mirror charge or discharge current is set by a programmable current source within the cell. This current source can be selected to output current scaled from 1 to 128 times the externally selected current level (7 bit dynamic range). A 7-bit counter controls the length of charging time.

In addition to the timer control bits and the current source control bits, there is one bit that controls whether the capacitor will be charged or discharged. By combining various charging times with current source levels it is possible to charge the capacitor voltage with a dynamic range of 14 bits in either the charge or discharge direction, for a total dynamic range of 15 bits.

4 HIGH-VOLTAGE, HIGH-DENSITY AUGMENTED INTEGRATED CIRCUIT

The CMOS base is fabricated separately in a standard foundry process. The process is a 1.2 μm mixed-signal process with support for high voltage transistors, which could be sourced from a number of different vendors. The particular process used supports up to 120 V. Each cell is almost completely self-contained, having sufficient drive and addressing electronics to require a minimal amount of peripheral support. This makes it possible to design a stitchable layout that is scalable to a high port count (>4096) with a very high fill factor. Approximately 90% of a column is optically active.

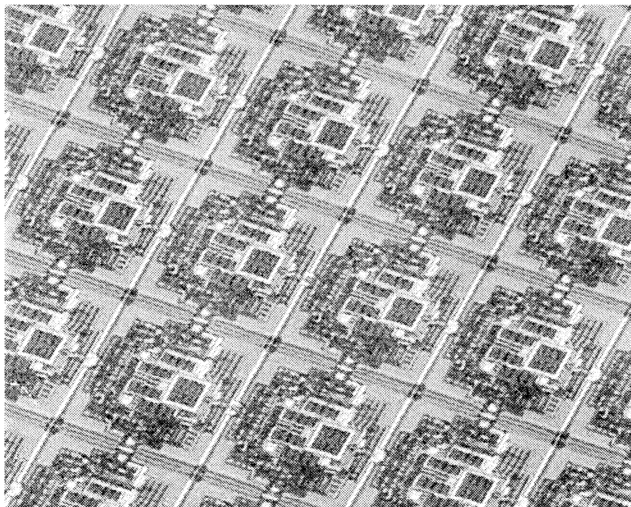

Figure 5 – Scalable, stitchable CMOS pattern for individual mirror cells.

The array of mirror cells is shown in Figure 5. The chip contains digital to analog converters, high voltage amplifiers, address decoders and other supporting circuitry. This functionality reduces the number of bond pads necessary to just over 700 for an array of 1024 mirrors, a reduction of approximately 6-fold from a passive addressing scheme.

The standard process, however, does not have sufficient interconnect support for the mechanical and electrical requirements of the MOEMS mirror array. Because the chip is both larger and more complex than is typically fabricated in this process (>2 million transistors, 40 x 50 mm), the number of standard metal layers does not provide sufficient utility for the desired routing.

In addition, a unique requirement of the TNI MEMS mirror is that the angular amplifier under the mirror needs a mechanical clearance. The vertical space required is about 20 μm, which is more than could be supported by removing the metals and dielectrics of the standard process.

To meet these requirements, three additional metal layers were added using a thick dielectric. The interconnects support greater than 200 V and have a long track record of reliability in the packaging industry [6,7]. The layers were added using benzocyclobutene (BCB). The process was a modification of the standard multi-layer metal process used in bump bonding.

The thickness of the BCB-metal layers (~7 μm each) was designed to also support the mechanical clearance required by the mirror. Together with the controlled gap of the wafer bond (section 5), it was only necessary to remove the upper metal layer to have sufficient clearance for the angular amplifier. The CMOS die after the multi-layer metal processing is shown in Figure 6.

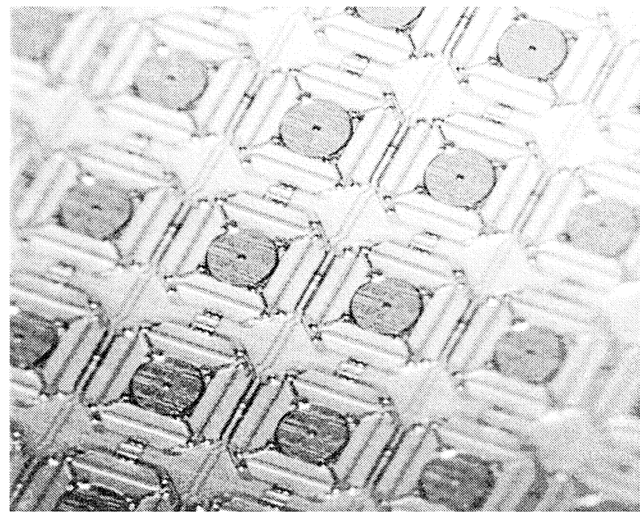

Figure 6 - Mirror cell array following the addition of an organic multilayer dielectric

5 VERTICAL INTEGRATION

The last critical component for successful integration is wafer bonding to unite the MOEMS mirror array and the augmented CMOS drive. The constraints on the bonding process are many. It must meet reliability requirements for a twenty year expected lifetime. It cannot change properties as it ages and it must not outgas within the hermetically sealed optical cross-connect. Both of these constraints argue against organic adhesives. It must be CMOS compatible, which rules out any high-temperature methods. It must be compatible with all subsequent processing and packaging chemistries and temperatures. The bonding

process must also not damage the delicate MEMS structures under the mirror.

A special wafer-wafer solder bonding technique has been developed which meets all of these requirements. First the CMOS wafer is sputtered with a seed layer of titanium and copper, equivalent to the under-bump metalization (UBM) used in the packaging industry. The "bump" layer is then electroplated, first with a copper spacer layer and then with a solder layer. The backside of the MOEMS mirror array is patterned with titanium, nickel and gold. In the last step, the wafers are aligned and then bonded during a tightly controlled thermal cycle.

The result is a metal-metal solder bonded wafer stack. In addition to a reliable mechanical bond between the MOEMS array and the CMOS, the solder bond also serves as an electrical contact to bias the actuator array. A virtual overlay of the resulting layers is shown in Figure 7.

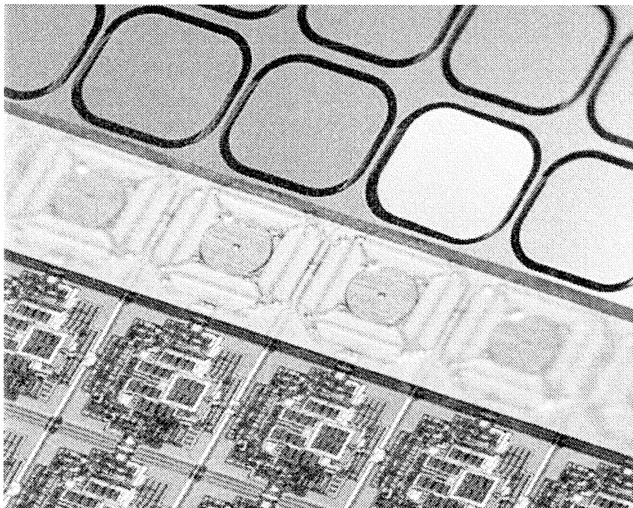

Figure 7 - A virtual cutaway showing the juxtaposition of the major components that have been vertically integrated into the MOEMS mirror array.

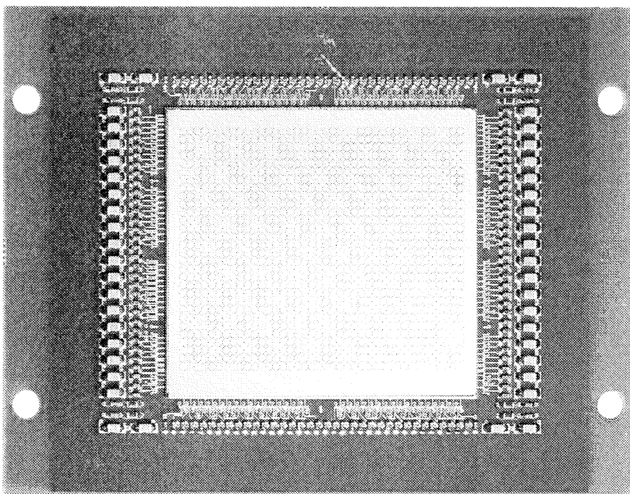

Figure 8 - Packaged MOEMS mirror array

6 CONCLUSION

The development of several key technologies that are critical to the world's first very large scale integration of a MOEMS mirror array are also directly applicable to the integration of other incompatible processes. For telecommunication applications, this may involve the integration of planar photonic integrated circuits with micromechanics and microelectronics. These techniques, together with a carefully designed, unit-cell approach to the mirror drive cell enable an extremely flexible and scalable architecture.

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