

Process for Extremely Thin Silicon-on-Insulator Wafer

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ABSTRACT

We observe hydrogen platelets buildup into single crystalline silicon caused by hydrogen plasma processing. The platelets are aligned along a layer of lattice defects formed in silicon before the plasma processing. The buried defect layer is formed by either silicon-into-silicon or argon-into-silicon implantation. We discuss the platelet nucleation, growth, and merge phenomena, and discuss applicability of the plasma hydrogenation to silicon-on-insulator wafer process of layer transfer type.

Keywords: SOI, hydrogen, silicon, implantation, platelets, plasma.

1 INTRODUCTION

Smart-cut™ is a process [1] that allows manufacturing silicon-on-insulator high quality (SOI) wafers in big quantities that was not possible before with preceding SOI processes as SIMOX. However, the Smart-Cut™ is still expensive because it requires hydrogen implantation in high dose $5 \times 10^{16} \text{ cm}^{-2}$ [1]. Moreover, the dose should be implanted at very low ion beam current (less than 80 microamperes [2], less than $4 \times 10^{13} \text{ ions/cm}^2/\text{s}$ [3], less than 0.1 mA [4,5]). Many attempts are known to reduce the dose and/or increase the dose rate. Most of the attempts use double-specie implantation, like helium-then-hydrogen [6,7,8] proving that the total dose required can be reduced to $2 \times 10^{16} \text{ cm}^{-2}$ in the best case. It has been suggested by Usenko et al. [9,15] to reduce the total cost of the layer transfer process by diffusing hydrogen to a buried trap layer in silicon. Here we are continuing that approach while using plasma for the hydrogenation.

The International Technology Roadmap for Semiconductors 2001 [16] projects that the cap Si layer for SOI starting wafers will be 20 to 100 nm in thickness by 2004 to support processing of fully-depleted CMOS circuits. Smart-Cut™ provide an inherent Si film thickness of about 500 nm and a minimum thickness of about 200 nm [17]. The thickness of the delaminated layer in the Smart-Cut process depends on the energy of implantation of hydrogen. When the energy of the H implant is reduced below 20 keV to achieve thin delaminating thickness problems arise [7]. Attempts have been reported to obtain thin (<200 nm) cap Si layer of SOI wafers. Terreault et al. [7, 18, 19] used low energy hydrogen implantation (5 to 8 keV) in a regular Smart-cut to get a thinner top SOI layer.

They concluded keV range hydrogen implant is infeasible for layer transfer. Maleville et al. [20] reports 70 nm top Si SOI using touch polishing of an initial 500 nm layer. Srikrishnan [21] forms (by implantation) an etch stop layer inside of the transferred with Smart-Cut silicon film with a subsequent etching. Popov [22] reports a layer-by-layer oxidation (of the film transferred with Smart-cut) with subsequent stripping in diluted HF for thinning of the layer. All listed approaches increase SOI wafer production cost and degrade thickness uniformity. Our work here reports the plasma hydrogenation as a post process following a low level implant to create the desired cap layer of thickness less than 100 nm.

2 EXPERIMENTAL

Si wafers, variously doped, <100> orientation, were implanted with Si at 180 keV, $2 \times 10^{15} \text{ cm}^{-2}$. Some samples were implanted with argon at 180 keV, $1 \times 10^{15} \text{ cm}^{-2}$. Then the as-implanted samples were processed with RF hydrogen plasma during ~1 hour with 300 W RF power, 1 mTorr hydrogen pressure. The samples were kept at 200°C during first ½ hour, and then the sample temperature was increased to 300°C. Some wafers were annealed at 550°C to initiate blistering. The wafer surfaces were analyzed with atomic force microscope. Infrared absorption measurements were performed using both transmission and multiple internal reflection geometries [23] to gain access to both bonding and stretching vibrations of trapped hydrogen. The processing conditions are summarized in the Table I. Layer transfer experiments were also performed. Pre-bonding, cleavage, and post-bonding steps were performed as in the Smart-cut process. The thickness of transferred layers was measured with a Dektak profilometer near wafer edges where the layer transfer fails.

3 RESULTS

Figs.1, 2 show surface of a wafer processed with the self-implantation+hydrogenation, and annealed at 550°C. The surface is covered with features with lateral dimensions about 0.2 micron and vertical dimension about 5 nanometers. Additional layer transfer experiments show successful layer transfer Fig.3 even for much shorter plasma processing time than needed to develop the surface relief Figs.1, 2. Infrared measurements (of plasma processed unannealed samples before layer transfer) Fig. 4 show high hydrogen peaks.

TABLE I.

Wafer		
Diameter	100 mm	
Growth	Czochralski	
Dopant	Boron	
Resistivity	1 Ohm cm	
Implantation		
Specie	Silicon+	Argon++
Energy	180 keV	395 keV
Dose	2x10 ¹⁵ cm ⁻²	1x10 ¹⁵ cm ⁻²
Hydrogenation		
Source	RF plasma	
Plasma power	300 Watts	
Temperature, 1st step	200oC	
Duration, 1st step	½ hour	
Temperature, 2nd step	350oC	
Duration, 2nd step	1 hour	

The layer transfer occurs in cases of proper selection of implantation conditions and plasma hydrogenation conditions. A typical edge profile of the transferred layer is

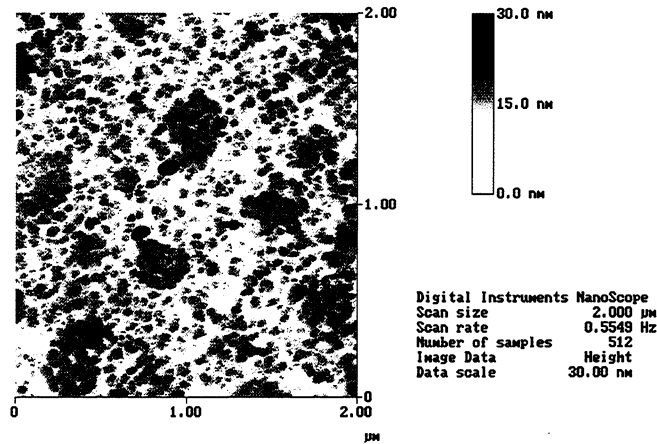


Fig. 1. Surface relief developed on self-implanted silicon wafer after plasma hydrogenation, (area of view 2x2 μm²).

shown on Fig.3. The thickness of the transferred layer is 75 nm. Similar results are obtained for some other heavier ions that penetrate less deeply.

Infrared absorption measurements Fig.4 taken on samples processed under 300°C (300°C during the 2nd plasma immersion step indicate that hydrogen is primarily located on internal surfaces, with some H still in monovacancy-type defects such as VH and VH₃). This finding is consistent with previous studies [23]. Further studies are under way to characterize the nature and location of hydrogen incorporated in the silicon as function of processing conditions.

4 DISCUSSION

Hydrogen in atomic form is known for its high diffusivity in silicon and its ability to combine with many

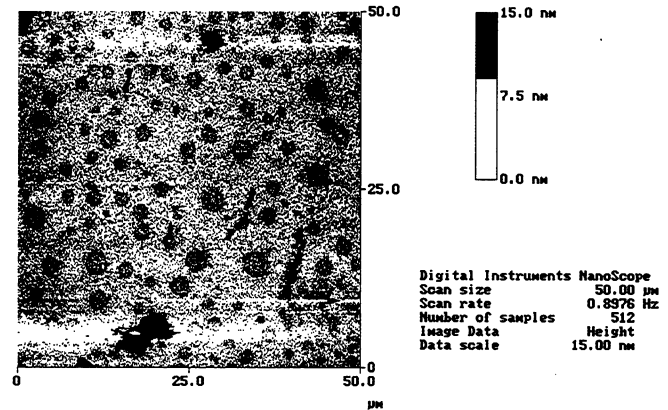


Fig. 2. Surface relief developed on self-implanted silicon wafer after plasma hydrogenation, (area of view 50x50 μm²).

types of defects in crystalline silicon. It is known since 1987 that plasma hydrogenation of regular single crystalline silicon results in formation of hydrogen platelets [24,25]. Because of lack of defects in silicon bulk and low hydrogen solubility in silicon, the platelets in [24,25] are found in near-surface defect-rich regions only. To control the process of hydrogen platelet distribution in silicon, an additional step of forming of defect-rich layer is needed. To accumulate the hydrogen in the desired part of the wafer we need to pre-form defects that readily interact with hydrogen. Silicon-into-silicon implantation allows forming a dense defect layer at desired depth under the surface. Low-soluble gas (He, Ar, Ne, Kr, Xe) implantation is another option to form the trap layer. Using of heavier implants like xenon will allow to reach extremely thin transferred layers ~tens of nanometers. For example, SRIM simulation gives Rp for 50 keV xenon is about 30 nm.

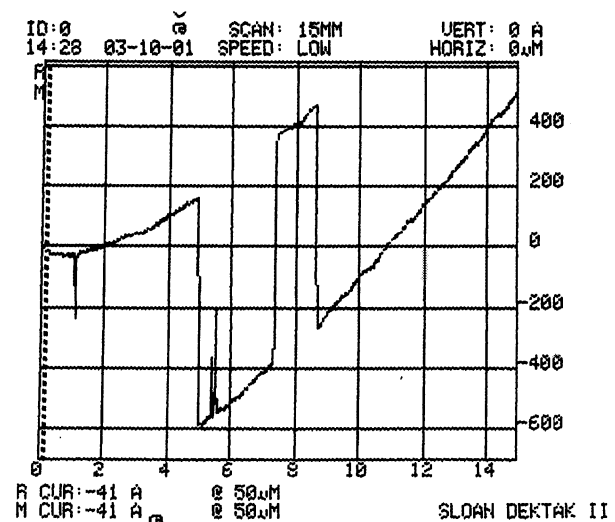


Figure 3. Profile near the edge of transferred layer.

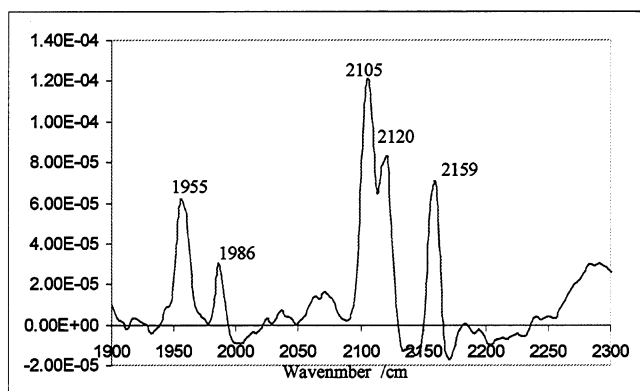


Fig.4. IR spectra of hydrogenated sample. 1955 and 1986 relate to Si-H, and 2105, 2120, 2159 peaks relate to molecular hydrogen attached to internal surfaces in Si.

The RF plasma causes a platelet nucleation and growth along a layer at a depth of about R_d (depth of maximum of vacancy type defects) of the defect-inducing implant. Lower temperature step the plasma process is for nucleation, and 300°C step for fast platelet growth, similar as in [24, 25]. A significant difference we found comparing hydrogenation results for self-implanted, and argon-implanted samples is that for the self-implanted samples the first low temperature step is required to get blistering, while for the argon-implanted samples the low temperature step can be skipped. A possible explanation is that the argon-implanted samples already contain the platelet nuclei in form of argon microbubbles, while in the self-implanted samples the platelet nuclei should be first formed from vacancy clusters. As compared to surface relief observed on surface of heavy hydrogen implanted wafers [1, 7, 8, 18, 23], the features Fig.1,2 have about 10X smaller lateral and 100X smaller vertical dimensions.

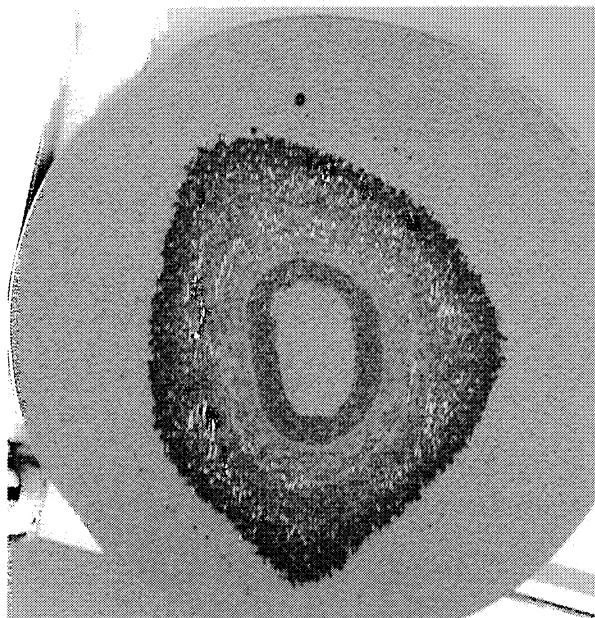


Fig.5. Typical wafer blistered during implantation. Implantation conditions: H_2^+ at 100 keV, 0.3 mA.

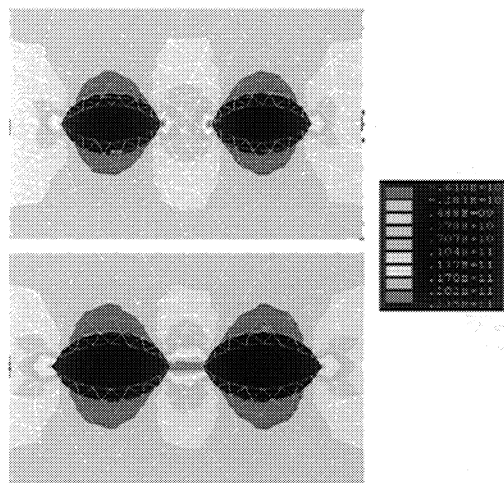
An inherent delaminating thickness for either Smart-cut or the trap-filling processes is controlled by implantation depths [1, 7, 8]. For Smart-cut the depth is the R_d of hydrogen implant while for the trap-filling process is R_d of heavier ions used. Correspondingly, the 200-2000 nm, and 20-200 nm layers are transferred. Therefore, the trap-filling process is advantageous for making thin SOI.

Experiments with blistering were widely used elsewhere to understand phenomena involved in the Smart-cut [3, 9, 14] process. At the level of hydrogen implantation required in Smart-cut (i.e. about $5 \times 10^{16} \text{ cm}^{-2}$), the silicon surface easily blisters during implantation (Fig.5), even without an additional annealing. The silicon wafer surface can be also blistered after RF plasma hydrogenation. An interesting feature is that the minimum hydrogenation time in RF plasma required for blistering is several times longer, than the time required for successful layer transfer. Typical blistering picture after RF plasma hydrogenation and subsequent anneal is shown on Fig.1 and Fig.2. We suppose, that in blistering experiments there are much higher hydrogen loss due to outdiffusion than for the case of layer transfer. These hydrogen losses may be due to the proximity of surface, or due to a difference in the type of the traps binding the hydrogen. When the hydrogen-rich layer (either obtained by trapping of by implantation) evolves into a quasi-continuous cleavage plane, the hydrogen atoms or molecules detraps from one defect, diffuse to another defect with higher bonding energy, and get trapped again. In a case of high dose hydrogen implantation the higher mechanical stress is expected, so we expect more weakened silicon bonds, and higher bonding energy for hydrogen attaching to those sites.

In Smart-cut, to keep the large amount of hydrogen inside the silicon wafer, the local temperature under the beam should not substantially exceed room temperature. This restriction severely limits the maximum hydrogen ion beam current during the implantation step in the Smart-cut process. For similar process work reported elsewhere [2-4] and by ourselves [5], the hydrogen beam current is limited to 0.1 mA using conventional implanters to prevent blistering of wafers in the implanter. At this beam current hydrogen implantation for Smart-cut will take 24 hours to fully implant 300 mm.

At the beginning of plasma hydrogenation, atomic hydrogen diffuses through silicon and attaches to broken bonds in a layer damaged by implantation [11]. The next step in hydrogen evolution is to form nuclei of hydrogen platelets. It happens at temperatures lower than 250°C as previously found by Johnson et al. [24,25]. Further hydrogenation increases the platelet size and can be done at higher temperatures. Higher temperature during the second stage of hydrogenation is also needed to allow Oswald ripening during which time bigger platelets grow at the expense of smaller ones [24,25]. By collecting the hydrogen from the hydrogen-rich layer, the platelets transform into micro bubbles [23]. The neighbouring

As we have shown above, hydrogen dose rate severely limits Smart-cut. Higher implant rates might be acceptable using implanters with a special cooling system, but there



are no published data yet that confirms efficiency of the cooling for the Smart-cut. Also, the cooled wafer surface effectively adsorbs residual gases from the implantation chamber, and that adsorbed species immediately undergo ion mixing by continuing hydrogen implantation. Finally it results in heavy contamination in the cap layer of the SOI substrate. In our process, neither high dose implantation nor hydrogen implantation are needed, thus making our process potentially advantageous. Also, the typical implantation doses needed to form the trap layer is lower than 10^{15} cm^{-2} , that might result in better crystalline quality of the cap layer in the final SOI wafer as compared to the Smart-cut.

5 CONCLUSION

RF plasma hydrogenation of a buried trap layer formed with low dose ion implantation has been demonstrated for forming SOI with a thin cap layer. Experiments described here indicate that the trap-filling process can provide a 10X reduction in SOI cap layer thickness.

6 ACKNOWLEDGMENT

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REFERENCES

- [1] B. Aspar, H. Moriceau, E. Jalaguier, et al. *Journ. Electronic Materials*, 30, 834 (2001).
- [2] K. Henttinen, I. Suni, S. S. Lau, *Applied Physics Letters*, 76, 2370 (2000).

- [3] Y. Zheng, S. S. Lau, T. Höchbauer, et al., Journal of Applied Physics, 89, 2972 (2001).
- [4] K. Henttinen, T. Suni, A. Nurmela, et al., Nucl. Instr. and Meth. in Phys. Res. B, 190, 761 (2002).
- [5] A.Y.Usenko, W.N. Carr, B. Chen, Y. Chabal, in: 2002 IEEE/SEMI Advanced Semiconductor Manufacturing Conf. Proc., p.6-10 (2002).
- [6] A. Agarwal, T. E. Haynes, V. C. Venezia, and O. W. Holland, Applied Physics Letters 72 1086 (1998).
- [7] C. Qian, B. Terreault and S. C. Gujrathi, Nucl. Instr. and Meth. in Phys. Res. B, 175-177 711 (2001).
- [8] Q.-Y. Tong, R. Scholz, U. Gösele, T.-H. Lee, L.-J. Huang, Y.-L. Chao, and T. Y. Tan, Appl. Phys. Lett. 72, 49 (1998).
- [9] A.Y. Usenko, and W.N. Carr, in: Silicon-on-Insulator Technol. and Devices X, ed. by S. Cristoloveanu, PV 2001-3, The Electrochem. Soc., Pennington, NJ, pp.33-38 (2001).
- [10] A.Y.Usenko, W.N. Carr, Materials Research Society Symposium Proceeding Vol.681E, pp.I3.3.1-I3.3.6, (2001).
- [11] A.Y.Usenko, W.N. Carr, in: Proceedings of 2000 IEEE SOI Conference, Wakefield, MA, Oct.2000, pp.16-17 (2000).
- [12] A.Y. Usenko, , US Patent 6,368,938.
- [13] A.Y. Usenko US Patent 6,352,909.
- [14] A.Y. Usenko, W.N. Carr US Patent No.6,346,459.
- [15] A.Y. Usenko, US Patent No. 6,344,417.
- [16] The International Technology Roadmap for Semiconductor, 2001, Front End Processes, p.7, (2001).
- [17] General Specification for: customized UNIBOND® Wafers, SOITEC, 2002.
- [18] C. Qian and B. Terreault, Journal of Applied Physics, V. 90, pp. 5152-5158 (2001).
- [19] C. Qian, B. Terreault, Materials Res. Soc. Symp. – Proceedings, 585, 177 (2000).
- [20] C. Maleville; E. Neyret; L. Ecartot; E. Arene; T. Barge; A.J. Auberton, in: 2001 IEEE International SOI Conference, pp. 155 –156 (2001).
- [21] K.V. Srikrishnan, US Patent 5,882,987, March 16, 1999.
- [22] V. P. Popov, I. V. Antonova, V. F. Stas, et al., Materials Sci. and Engineering B73 82–86 (2000).
- [23] M. K. Weldon, V. E. Marsico, et al., J. Vac. Sci. Technol. B 15, 1065 (1997).
- [24] N. H. Nickel, G. B. Anderson, N. M. Johnson, and J. Walker, Phys. Rev. B 62, 8012-8015 (2000).
- [25] N. M. Johnson, F. A. Ponce, R. A. Street, and R. J. Nemanich, Phys. Rev. B 35, 4166 (1987).