Wafer-Level High Density Multifunctional Integration (HDMI) for Low-Cost Micro/Nano/Electro-Opto/Bio Heterogeneous Systems

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ABSTRACT

A technology platform demonstrating wafer-level high density multifunctional integration (HDMI) based upon three-dimensional (3D) technology is described, which offers the potential for future low-cost integration of information processing and sensor/actuator technologies. This HDMI scheme alleviates processing and material constraints associated with system-on-a-chip (SoC) electronic integration, while providing the capability of extension to opto-electronic, bio-molecular and other micro/nano heterogeneous system applications. Process development results obtained to date are discussed, and approaches to heterogeneous integration using this novel technology platform are outlined.

Keywords: High Density Multifunctional Integration (HDMI), 3D integration, heterogeneous systems, system-on-a-chip (SoC), system-in-a-package (SiP).

1 INTRODUCTION

Wafer-scale high density multifunctional integration (HDMI) based upon three-dimensional (3D) technology as depicted in Fig. 1 has many advantages including high-performance electrical interconnection, high packing density, and heterogeneous technology integration [1]. The potential for incorporating any planar technology with Si IC (information/data processing) is of extreme interest, with many approaches for electronic 3D being pursued [1-4]. While they all have electronic interconnect advantages analyzed elsewhere [5] to meet semiconductor roadmap limitations [6], they differ in processing requirements and extendibility to non-electronic HDMI.

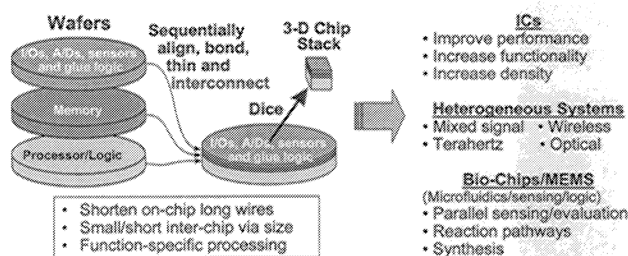

Fig. 1. High density multifunctional integration (HDMI): using a 3D platform for future IC chips and heterogeneous systems, formed by monolithic wafer alignment, bonding, thinning and inter-wafer interconnection.

In our approach fully processed wafers (with multilevel interconnects) are aligned and bonded with a dielectric glue, followed by top-wafer thinning to < 10 μm using backside grinding, polishing and etching. Subsequently, a copper damascene inter-wafer interconnect is formed using high-aspect-ratio (HAR) etching, copper deposition and chemical-mechanical planarization (CMP).

The final structure for a three-wafer stack depicted in Fig. 2 includes four major processing challenges, namely wafer-scale alignment accuracy, bonding integrity, wafer thinning and leveling control, and inter-wafer via formation. The electronic HDMI technology platform processing approach and status of our development are presented in the next section followed by extensions to non-electronic HDMI applications.

2 BEOL-COMPATIBLE PROCESSING FOR ELECTRONIC HDMI

The IC back-end-of-the-line (BEOL) compatible processing is split into two areas: (1) well-established baseline wafer bonding and thinning and (2) inter-wafer interconnection, employing material and processing strategies analogous to those used in advanced on-chip interconnects.

2.1 Wafer Bonding and Thinning

Wafer-to-wafer bonding has been studied using various dielectric glues with both blanket wafers and patterned wafers. The wafer bonding is conducted in a vacuum chamber of an EV Group (EVG) 501 bonder at conditions (e.g., temperature) compatible with BEOL processes.

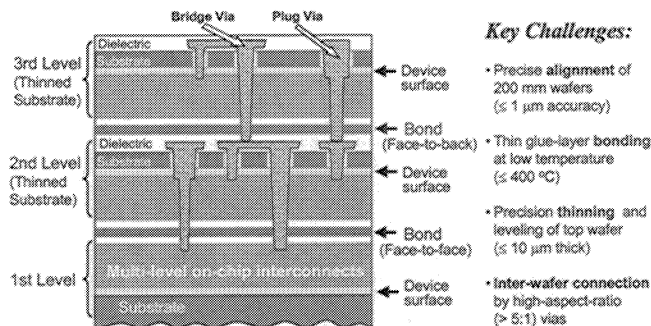

Fig. 2. Schematic of a monolithic HDMI test vehicle using wafer bonding, showing bonding interface, vertical inter-chip vias (plug- and bridge-type), and "face-to-face" and o-back" bonding.

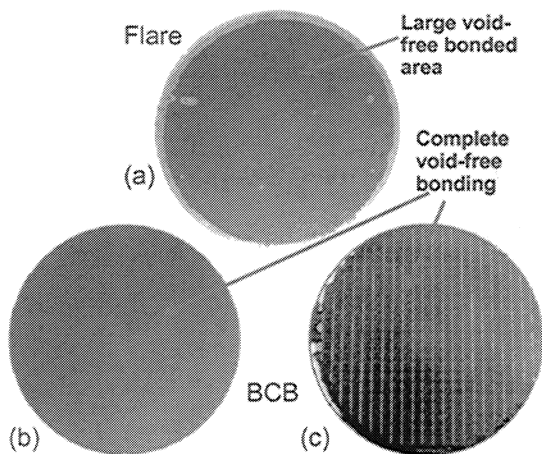

Fig. 3. Wafer bonding results: (a) Corning glass 7740 bonded to Prime Si with Flare [1], (b) PG&O glass 1737 bonded to Prime Si with BCB, and (c) two via-chain patterned wafers bonded with BCB. No visible changes can be observed after Si wafers are thinned to ~ 30 μm.

Figure 3(a) shows the wafer bonding result using Flare (Poly aryl ether) as the bonding glue on blanket wafers. Figures 3(b) and 3(c) show wafer bonding results using benzocyclobutene (BCB) as the bonding glue on blanket wafers and our via-chain patterned wafers, respectively. In Figs. 3(a) and 3(b), a silicon wafer is bonded to a commercial thermal-coefficient-of-expansion (TCE) matched glass wafer so that bonding uniformity can be visually inspected through the glass wafer. Void-free bonding is routinely obtained with BCB on both blanket and patterned wafers. High bonding strength is achieved for both Flare and BCB, as determined using the razor blade test and four-point bending test [7, 8].

Subsequent to wafer bonding, the top Si wafer is thinned to less than 10 μm and leveled to minimize the inter-chip via length and aspect ratio using a two-step thinning process, which has been established to minimize mechanical damage. In the first step, the backside Si substrate is uniformly thinned to ~ 30 μm by mechanical grinding and polishing (CMP). Figure 4 shows a plot of 49-point thickness measurement of a thinned top Si wafer, which is bonded onto a glass wafer with BCB as the bonding glue before thinning. Similar results are routinely obtained with this first-step thinning process.

In the second thinning step, several alternatives are being explored to further thin the top wafer to the desired thickness [9], including (1) continue (fine) grinding and polishing, (2) reactive ion etching (RIE), and (3) wet chemical etching. In our via-chain fabrication and wafer thinning with SOI wafers, the baseline second-step thinning process uses tetramethyl-ammonium hydroxide (TMAH) as the Si etchant due to its compatibility with CMOS process and excellent selectivity to SiO_2 (selectivity as high as 6000 has been obtained using this approach).

Results to date show a stable bonding interface after the Si wafers are ground and polished to ~ 30 μm for all the bonded wafers, i.e., either blanket wafers or patterned

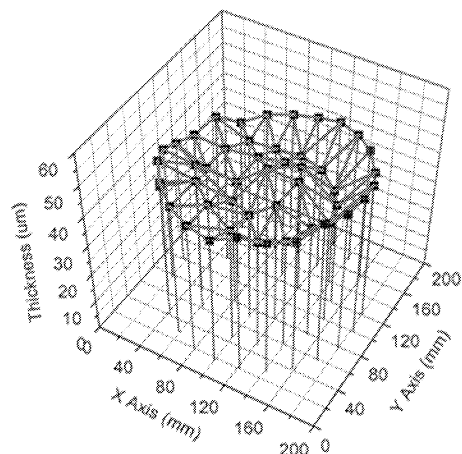

Fig. 4. A 49-point thickness map of top Si wafer after backgrinding and CMP (with Aptek Industries), with a mean of 42 μm and a standard deviation of 4 μm.

wafers using either Flare or BCB as the bonding glue. In Fig. 3(c), the backside of the top, patterned Si wafer is ground, polished, and wet-etched using TMAH. A void-free bonding interface and damage-free patterns are maintained. In some cases it was observed that some areas of the backside silicon are thinned through to oxide or the glue layer due to over-thinning; however, the remaining silicon layer (very thin) is still bonded well to the bottom wafer, with no visible changes at the bonding interface.

2.2 Inter-Wafer Interconnects

With the baseline processes of wafer bonding and thinning established, the remaining key challenge for 3D integration is the processing of inter-wafer interconnects. This section focuses on inter-wafer interconnects, including processes for wafer-to-wafer alignment, HAR via etching and cleaning, liner and copper filling, and CMP. In order to evaluate the processing feasibility and to establish design rules for inter-wafer interconnect technology using dielectric wafer bonding, a four-layer mask set of via-chain test structures has been developed with features for testing both bridge and plug types of vias [1, 9].

Figure 5 illustrates the process flow of the inter-wafer interconnect fabrication, showing plug- and bridge-type vias. The Si substrate on the top wafer is completely removed by backgrinding, polishing, and wet-etching in order to simplify and focus on the inter-wafer interconnect process. Except for wafer-to-wafer alignment and bonding, conventional Cu damascene BEOL processes are used for this test structure.

Images in Fig. 6 show plug- and bridge-type via-chain patterns for a two-micron via with different landing pads, plug sizes (for plug type) and chain lengths, prior to deep via processing. These photographs are taken on a pair of Cu-damascene wafers after alignment, bonding and top wafer thinning using our baseline process with the top Si substrate completely etched, and bridge lines, plug pads and test pads patterned. As can be seen, one-micron wafer-to-

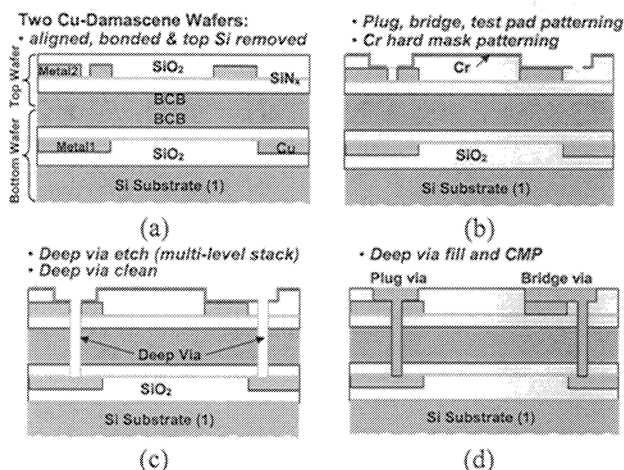

Fig. 5. Inter-wafer interconnect process flow for via-chain structure fabrication.

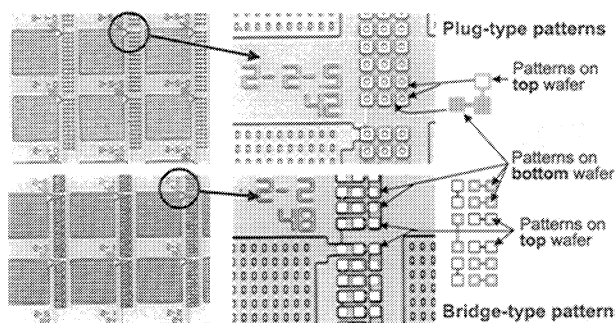

Fig. 6. 200 mm wafer alignment accuracy with via-chain test structures, indicating one-micron wafer-to-wafer alignment has been achieved (<0.5 μm shown). Pictures taken on a pair of Cu-damascene wafers, prior to deep via processing (see text).

wafer alignment accuracy has been achieved using an EVG wafer aligner with SmartView™ technology, though the alignment accuracy varies over the 200 mm wafer pair. While the wafer alignment accuracy will be improved in time, the one-micron accuracy is sufficient for most applications envisioned since global interconnects have relatively large feature sizes.

The HAR via etching is quite complex because the via is of the order of 10 μm deep and the etch has to go through a multi-level/ material stack. Control of the sidewall profile with a variety of materials (such as SiO_2 and the BCB bonding glue) is challenging, and the etch rate may not be uniform due to via-size differences and etch-chamber loading effects. A few hard-mask materials have been considered for such a deep HAR via etching, namely chromium, silicon, silicon carbide, and aluminum. In this work, a 0.2 μm chromium layer is used as the hard mask.

A design-of-experiment procedure was used to study the deep via etch through various materials on either blanket films or multi-material structures, using a 200 mm wafer capable inductively coupled plasma (ICP) reactor. Figure 7 shows a SEM picture of a vertical and clean etching achieved for BCB blanket film. In general, the via must penetrate through more than three different materials,

Fig. 7. Vertical and clean etching of BCB film with a Cr hard mask

including Si, SiO_2 or other low-k dielectric with etch-stop, and bonding adhesive layer (BCB or Flare in our work) [9].

Prior to via filling after etching, a two-step via cleaning is used, i.e., wet-chemical cleaning followed by plasma dry clean. For via filling, a low temperature (< 300°C) CVD TaN liner process is carried out on a custom designed load-locked 200 mm wafer CVD tool. The Cu CVD fill is performed on a modified Tokyo Electron (TEL) Phoenix 200 mm wafer cluster tool. A PVD copper flash layer is applied prior to CVD copper fill in order to enhance the adhesion of the thick stack [9].

Figure 8 shows a FIB cross-sectional view of a filled vertical via in a test structure similar to the via-chain test chip. Though Fig. 8 shows seamless wafer bonding ($Si/SiO_2/BCB$-$BCB/SiO_2/Si$ substrate, where the top Si was removed completely) and a complete via fill, some issues associated with via etch (e.g., BCB lateral etch) and via clean remain to be addressed. CMP of such structures to complete the copper damascene process has been demonstrated.

3 HETEROGENEOUS HDMI

Heterogeneous integration is possible with any technologies having a common starting wafer diameter and die size. An example of heterogeneous integration of an optical distribution wafer (top wafer) and two electronic wafers (e.g., a high speed processor (bottom wafer) and a memory (middle wafer)) is shown in Fig. 9. Across the die, the distance between the optical distribution network and the photodetectors in the Si CMOS circuitry (middle and bottom wafers) is 10-15 mm. With a similar approach, the top wafer could be a sensor, actuator (e.g., MEMS) or bio-

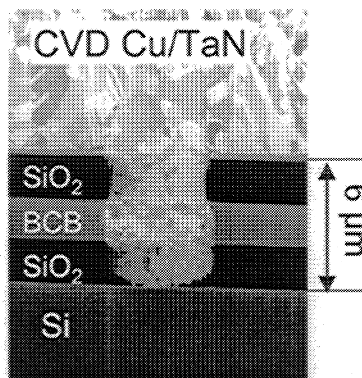

Fig. 8. FIB cross-sectional view of a vertical via (4 μm in diameter).

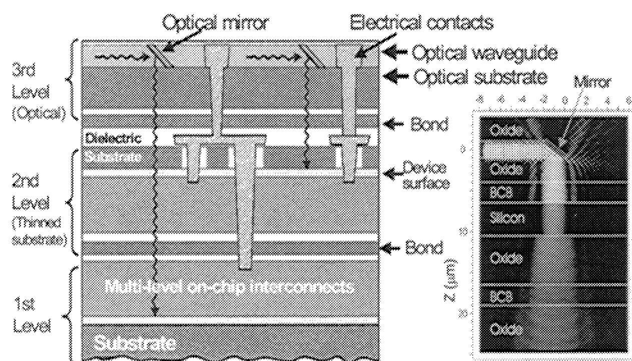

Fig. 9. HDMI with optical inter-wafer interconnects, showing the schematic (left) and the simulation result of the divergence of an optical beam (right).

molecular structure, with either silicon or TCE-matched glass substrates. A chip-scale reactor incorporating a microfluidic pump is shown in Fig. 10.

A package assembly envisioned to such HDMI implementations as depicted in Fig. 11 [10] includes a high density of input/output (I/O) contacts using flip-chip solder bumps or sea-of-leads contacts [11] to a thin film structure. Vias through the stack are used for heat sinking, electrical isolation and power distribution purposes. A flexible backplane connection can be included for additional I/O capability (e.g., optical, RF or power).

4 SUMMARY AND CONCLUSIONS

As the electronic HDMI can significantly improve interconnect performance by reducing delays of global interconnects, more generic HDMI for low-cost micro/nano/electro-opto/bio heterogeneous systems can be enabled by this technology with reduced processing and material constraints. Nanotechnology enhancements such as atomic layer deposition (ALD) liners and bonding layer adhesion promoters can easily be incorporated in our process flow.

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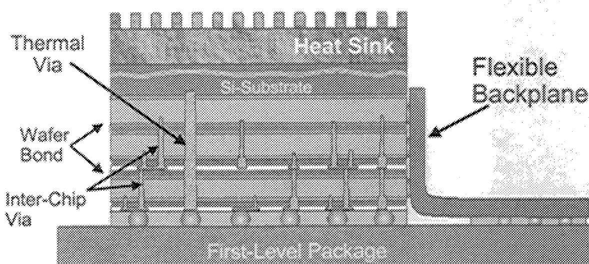

Fig. 11. Package assembly envisioned with HDMI technology. Thermal and ground vias enable cooling and electrical isolation; flexible backplane (edge contacts) offers additional I/O capability.

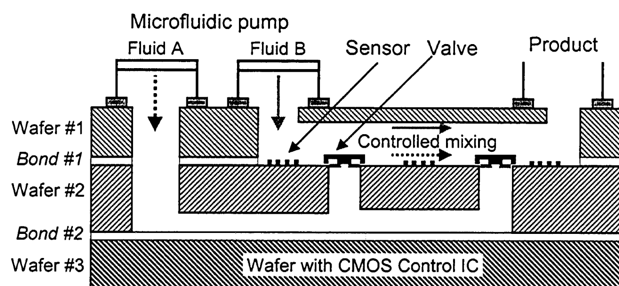

Fig. 10. A schematic of a microfluidic system integrated with a CMOS processor, which controls the electrically actuated valves to allow an optimal mixing of two or more fluids in a micro-channel using the signals from chemical sensors.

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