A Predictive Length-Dependent Saturation Current Model Based on Accurate Threshold Voltage Modeling

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ABSTRACT

This paper presents a compact length-dependent saturation current (I_{dsat}) model for deep-submicron MOSFET's based on accurate modeling of the threshold voltage (V_{th}). The proposed unified model has considered all the important two-dimensional (2-D) short-channel effects, such as V_{th} roll-up and roll-off, drain-induced barrier lowering (DIBL), transverse-field mobility degradation and series resistance. The unique feature of the compact model is its ability to correlate to process variations such as implantation dose and energy. The model is verified with measured I_{dsat} data for various bias conditions and process split-run.

Keywords: Saturation current, threshold voltage, short-channel effect, compact modeling, process correlation.

INTRODUCTION

The turn-on current of a MOSFET is one of the most important device parameters for advanced digital circuits as it determines the delay of logic gates. For a fixed-dimension MOSFET, its turn-on current, also known as saturation current (I_{dsat}), is normally defined as the drain current at gate (V_{gs}) and drain (V_{ds}) biases both being equal to its power supply (V_{dd}). It is well known from semiconductor theory that MOSFET's I_{dsat} is related to its device dimension, gate oxide thickness, high-field mobility, source and drain series resistance, gate- and substrate-bias conditions, and most importantly, its bias-dependent threshold voltage (V_{th}). In this paper, an improved bias-dependent V_{th} model [1] that relates to process conditions is proposed and discussed, thereby, a predictive I_{dsat} model, which also correlates to process conditions, is presented. The proposed saturation current model is compared and verified with experimental data of a 0.25-μm 2.5-volt CMOS technology.

MODEL

The theoretical threshold voltage of a MOSFET consists of three components, namely, the flat-band voltage (V_{FB}), the channel surface potential (ϕ_s), and the potential across the gate insulator (V_{ox}), which can be expressed as:

$$V_{th} = V_{FB} + \phi_s + \frac{Q_B}{C_{ox}}$$

However, this simple model is only valid for long-channel devices because it does not account for 2-D effects, such as charge sharing, lateral doping pile-up and DIBL. A predictive bias-dependent V_{th} model that accounts for the above effects has been developed [1], [2]. An extension of that model is used in this work, which consists of only five important process-dependent parameters and two auxiliary DIBL parameters, namely, N_s, λ, α, β, κ and i, j, respectively. The improved V_{th} model is as follows:

$$V_{th} = V_{FB} + \phi_s + \gamma\sqrt{\phi_{s0} - V_{bs}}\left[1 - \frac{\lambda\zeta}{L_{eff}}\left(\sqrt{\phi_s - V_{bs}} + \frac{jV_{ds}}{\sqrt{\phi_s - V_{bs}}}\right)\right]$$

$$\zeta = \sqrt{\frac{2\varepsilon_{si}}{qN_{eff}}}$$

$$\phi_{s0} = \frac{2kT}{q}\ln\left(\frac{N_{eff}}{n_i}\right)$$

$$\phi_s = \phi_{s0} - \Delta\phi_s$$

$$\Delta\phi_s = \frac{1}{\cosh\left(\frac{L_{eff}}{2l_\alpha}\right)}\left[\left(V_{bi} - \phi_{s0}\right)\cosh\left(\frac{z}{2}\right) + \frac{iV_{ds}}{2}\,\frac{\sinh\left(\frac{L_{eff}}{2l_\alpha} - \frac{z}{2}\right)}{\sinh\left(\frac{L_{eff}}{2l_\alpha}\right)}\right]$$

$$N_{eff} = N_s + \frac{\kappa N_s}{\cosh(L_{eff}/2l_\beta)}$$

$$l_\alpha = \alpha\left(\phi_{s0} - V_{bs}\right)^{0.25}$$

$$l_\beta = \beta\left(\phi_{s0} - V_{bs}\right)^{0.25}$$

$$z = \ln\left(\frac{V_{bi} - \phi_{s0} + V_{ds}}{V_{bi} - \phi_{s0}}\right)$$

Each of the seven empirical fitting parameters has their own physical representation that characterizes the individual short-channel effects. The first parameter N_s

represents the effective vertical nonuniform channel doping profile, which shifts the V_{th}–L_g curve in parallel. All the other parameters affect the threshold voltage in short-channel regime only. The parameters k and b characterize the reverse short channel effect (V_{th} roll-up). k determines the degree of V_{th} roll-up while b sets the onset of V_{th} roll-up. Similarly, the normal short-channel effect (V_{th} roll-off) is modeled by the two parameters l and a. l is introduced to model charge sharing whereas a is for surface-potential lowering based on the quasi 2-D formulation [3]. The new auxiliary parameters i and j are introduced in this work to fine tune the DIBL dependency, which are used to model the asymmetric nature of the source and drain depletion region at high V_{ds} condition.

Once an accurate V_{th} model is available, developing an I_{dsat} model is mainly a matter of mobility and series-resistance modeling. The I_{dsat} model in [4] is employed, combined with our V_{th} model to predict experimental I_{dsat}–L_g data measured from the same wafer split-lots. The I_{dsat} model considers all the important short-channel effects, which include perpendicular-field mobility degradation, velocity saturation, as well as source/drain series resistance. The saturation current model is expressed as follows:

$$I_{dsat} = I_{dsat0}\left(1 - \frac{2I_{dsat0}R_s}{V_{gs}-V_{th}} + \frac{I_{dsat0}R_s}{V_{gs}-V_{th}+E_{sat}L_{eff}}\right)$$

$$I_{dsat0} = v_{sat}C_{ox}\frac{\left(V_{gs}-V_{th}\right)^2}{V_{gs}-V_{th}+E_{sat}L_{eff}}$$

$$E_{sat} = \frac{2v_{sat}}{m_{eff}}$$

$$m_{eff} = \frac{m_0}{1+\left(\frac{V_{gs}+V_{th}}{5.4t_{ox}}\right)^{1.85}}$$

In the above saturation current expression, the parameter m_0 represents the low-field mobility. It is used as a technology-dependent fitting parameter. On the other hand, m_{eff} is the effective mobility including the effect of perpendicular-field degradation. The values of the saturation velocity v_{sat} are fixed at 8×10^6 and 6×10^6 cm/s for electron and hole, respectively [5]. The I_{dsat0} expression represents the saturation current without taking into account of the series-resistance effect. However, for short-channel devices, due to the increased drive current, the potential drop across the source and drain series resistance cannot be neglected. The above I_{dsat} expression is used to model the series-resistance effect.

EXPERIMENTAL VERIFICATION

An empirically-based model will not be useful unless a consistent and simple parameter-extraction procedure can be adopted, nor will it be of any interest if experimental data are needed to extract the parameters every time the model is used. The compact V_{th} model employs a simple, five-step, parameter-extraction procedure, which requires the measured V_{th}–L_g data from the same process with only five sets of measurements: V_{th}(long L_g) for all V_{bs}, V_{th}(low V_{ds}, high V_{bs}), V_{th}(low V_{ds}, low V_{bs}), V_{th}(high V_{ds}, low V_{bs}) and V_{th}(high V_{ds}, high V_{bs}) for all L_g.

A simple nonlinear regression on the theoretical long-channel threshold voltage expression, fitting the long-channel V_{th}–V_{bs} data is used to extract N_s. The improved V_{th} model for short-channel devices can also be used since the values of (l, a, b, k, i, j) will not affect the long-channel V_{th}. The extracted N_s value will be fixed in the subsequent steps. Nonlinear regression on the improved V_{th} equation is then performed by fitting the V_{th}(low V_{ds}, high and low V_{bs}) vs. L_g data to extract l, a, b, and k. To characterize the DIBL effect, additional parameters i and j are needed. With fixed l, a, b and k extracted at low V_{ds}, i and j are extracted by fitting the V_{th}(high V_{ds}, low and high V_{bs}) vs. L_g data at high V_{ds}.

With additional long-channel $V_{th}(V_{bs})$ data for different wafer-splits, the parameter N_s in the V_{th} model can correlate to process variables such as V_{th}-adjustment implant dose (F) and punchthrough implant energy (E).

Once the V_{th} model is completely characterized, (by N_s, l, a, b, k, i, j), the low-field mobility (m_0) and series resistance (R_s) are extracted by fitting to only one set of I_{dsat}–L_g data at $V_{ds} = V_{gs} = V_{dd}$. Then, a complete compact I_{dsat} model with drawn gate length (L_g), bias voltages (V_{gs}, V_{ds}, V_{bs}) and process variables (implant dose F and energy E) as input parameters is available.

The excellent prediction of the I_{dsat} model to the experimental data has been demonstrated in Figs. 1–4. The empirical correlation between the channel doping parameter (N_s) and the implant dose and energy, which is extracted from long-channel V_{th} data (shown in the insets of Figs. 3 and 4), applies equally well to the saturation current.

Figures 1 and 2 show the model (*lines*) as compared to the measured data (*symbols*) for different gate and substrate biases, respectively. The V_{th} model parameters are extracted at V_{ds} = 0.1/2.5V and V_{bs} = 0/–2.7 V. Excellent prediction of I_{dsat} at the intermediate biases $V_{gs} = V_{ds}$ = 1 V and V_{bs} = –0.9/–1.8 V demonstrates the accuracy of the model. Figures 3 and 4 illustrate the predictibility of the model (*lines*) as compared to the experimental data (*symbols*) for different V_{th}-adjustment implant dose (F) and punchthrough implant energy (E), respectively. The parallel shift in the measured I_{dsat} has been well predicted by the shift in V_{th} due to the change in the substrate doping profile (long- and short-channel devices), which is related to the implant dose F and energy E through linear empirical correlation, as shown in the insets of Figs. 3 and 4. Once the correct channel-length dependent V_{th} parameters (N_s, l, a, b, k, i, j) and I_{dsat} parameters (m_0, R_s) are determined, the same set of parameters can be applied to various process and bias conditions.

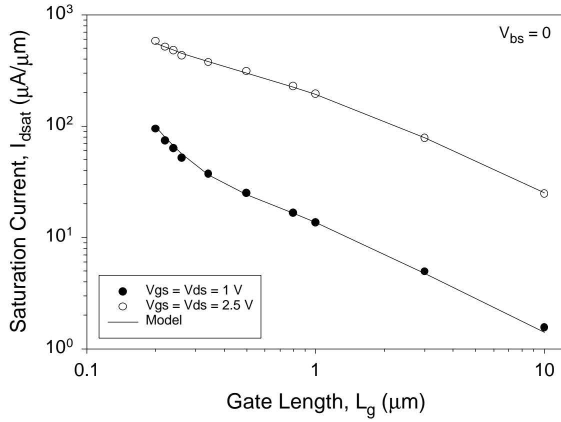

Figure 1: Measured (*symbols*) and modeled (*lines*) saturation current vs. gate length for different supply voltage V_{dd} (with $V_{gs} = V_{ds} = V_{dd}$). Only the V_{dd} = 2.5 V data are used for μ_0 and R_s extraction. All others are predictions by the model.

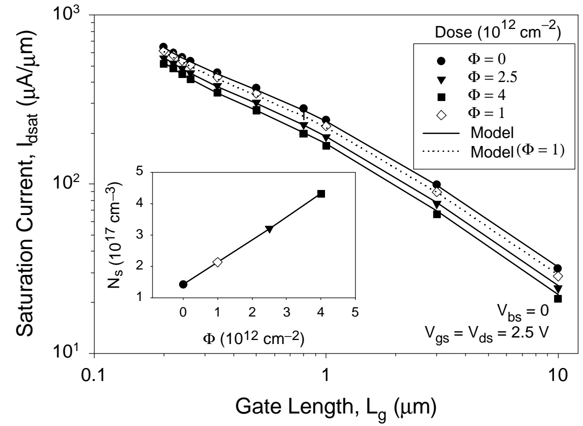

Figure 3: Measured (*symbols*) and modeled (*lines*) saturation current vs. gate length for different V_{th}-adjustment implant dose Φ. The inset shows the extracted linear correlation between N_s and Φ extracted from the V_{th} model.

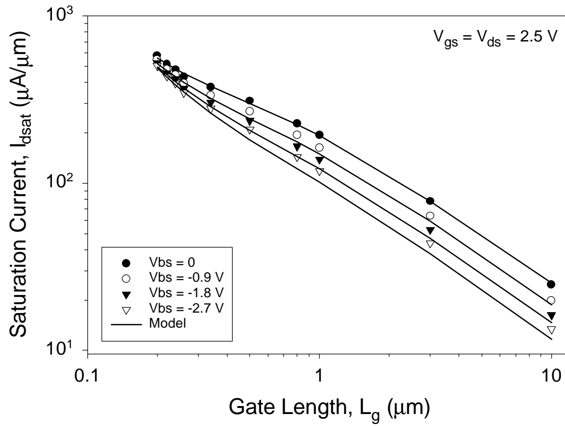

Figure 2: Measured (*symbols*) and modeled (*lines*) saturation current vs. gate length for different substrate bias V_{bs}. The V_{bs} dependency is modeled by the parameters in the V_{th} model.

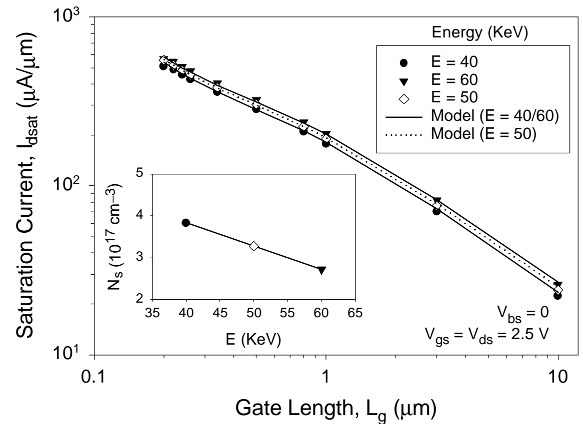

Figure 4: Measured (*symbols*) and modeled (*lines*) saturation current vs. gate length for different punchthrough implant energy E. The inset shows the extracted linear correlation between N_s and E extracted from the V_{th} model.

The essence of the proposed compact-modeling approach is to predict physical behavior by interpolation. This means that one needs to design the experiment to cover a wide range of interest (e.g., full range of L_g, V_{bs}, and V_{ds}) such that process-dependent empirical parameters can be extracted at the "extreme" conditions. Thereby, the model can be employed for prediction by interpolation at intermediate values of the variables without performing nonlinear regression on every set of experimental data.

CONCLUSION

The proposed model discussed in this work is simple and accurate, which is attributed to the accurate and physical modeling of the short-channel threshold voltage. With minimum effort in model parameter extraction and correlation to process conditions, the model can predict the length-dependent saturation current at all bias conditions. This work has demonstrated an efficient and accurate approach to modeling deep-submicron MOSFET's, which is very useful for reducing experimental wafer split-lot and for process control and optimization.

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