# Simulation of Nonideal Behaviour in Integrated Piezoresistive Silicon Pressure Sensors

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## ABSTRACT

The signal formation in piezoresistive silicon pressure sensors has been studied for many years and is very well understood meanwhile. Nevertheless there are higher order effects of nonideal behaviour such as nonlinearities and hysteresis effects which limit the possible accuracy of such sensors considerably. In high volume applications like in automotive area one has to think about minimization of such effects in order to improve performance and also to enhance yield and to reduce costs.

In this paper we demonstrate the reduction of temperature hysteresis effects of pressure sensors. The improvement is achieved using „influence strength“ (EFS, from german Einflußstärke) analysis and special test structures to examine the influence of local hysteresis effects on the behaviour of semiconductor devices.

***Keywords:*** pressure sensor, temperature hysteresis, test structure, design method

## METHOD

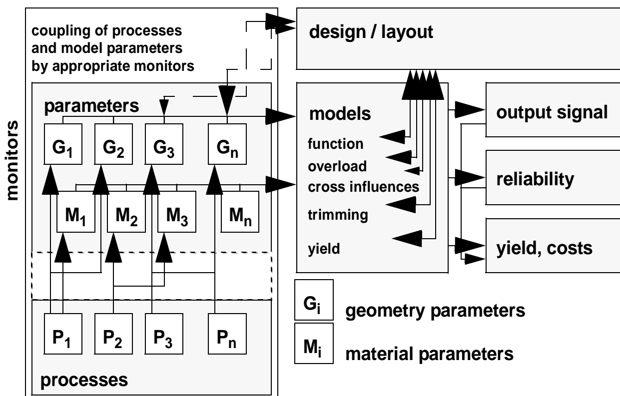


Fig. 1: General chart of the design flow used at Robert Bosch

The general idea of the design method is shown in figure 1. The following points are most important:

- Only two types of design-relevant model parameters (MP) are allowed to be used: geometry parameters (G) and material parameters (M). These parameters can be directly correlated to process influences. Each process (P) can influence different parameters and each parameter can be influenced by different processes.

- The distributions of these model parameters (including their $c_{pk}$-values) have to be known from process monitoring.

- All function parameters (FP) of the device (sensor, test structure) have to be expressed in terms of these process-dependent MP as given in eqn. 1:

$$FP_i = f(MP_j) \qquad (1)$$

The influence strength EFS describes the quality of a design (working point WP) with respect to the accuracy specification of the device as well as with respect to process tolerances. In every design recursion we calculate a matrix given by:

$$EFS_{ij} = \frac{\left.\frac{\partial}{\partial MP_j} FP_i\right|_{MP_{(n \neq j)} = WP} \cdot \Delta MP_j}{ATB_{FP_i}} \qquad (2)$$

Since we use only the first derivative at the actual WP it has to be ensured that the function behaves almost linear close to the WP. $\Delta MP_j$ is the scattering of the MP. We normally use the lower and the upper limit of the monitor value and interpret this span as $\pm 3\sigma$ of the distribution of the MP. ATB is the „allowed tolerance band“ of the function parameter $FP_i$. If the $FP_i$ is a trimmable parameter the ATB is given by the trimming limits. If the $FP_i$ is not trimmable - for example due to physical reasons or due to cost reasons - the ATB means a certain amount of the maximum tolerated accuracy error specified for the device.

Tab. 1: Classificaton of EFS-values

| $EFS_{ij}$-value | Classification |
|---|---|
| $EFS_{ij} > 1$ | hyper-critical |
| $1 > EFS_{ij} > k$ | critical $k = n^{-1/2}$. n is the number of MP |
| $EFS_{ij} < k$ | uncritical |
| $EFS_{ij} = 0$ | not influenced |

For a typical pressure sensor the number of MP is in the range of 50 to 80 and the number of FP is between 10 and 20. Therefore it is necessary to concentrate on the „important parameters“. To find these important parameters the EFS-matrix is a very powerful tool. The EFS values are classified as described in table 1. If $\Sigma_{sq}EFS_i = 1$ this means that $\pm 3\sigma$ of all pieces (99.73%) are *designed* to be within the ATB.

Taking all these relations into account one can deduce some ***standard design-strategies from EFS-analysis***:

- Find an optimized WP for the design to get as low $EFS_{ij}$-values and $\Sigma_{sq}EFS_i$-values as possible.
- If there are limits in optimization (due to boundary conditions like maximum chip area, maximum capture range of trimming ...), one always has to try to design critical functions to such MP which depend only on processes with high $c_{pk}$-values.
- For nonidealities which are not trimmable and which can not be optimized for the above mentioned reasons one has to find compensation mechanisms by applying the physical knowledge about the FP which one got during the development of the models. Additional information about EFS analysis is given in [4].

An example for this strategy will be given in the following sections.

## TEMPERATURE HYSTERESIS

The pressure sensor signal and the properties of the evaluation IC show temperature hysteresis. The hysteresis is caused by the plastic deformation of the two layer aluminum metallization which is used in our bipolar process ((100) silicon). When heating and cooling the chip within a temperature range of $\Delta T \geq 50°C$, the thermomechanical stress in the aluminum reaches the elastic limit: the deformation becomes plastic.

We describe the complex plastic effects with a term called „remanent stress“. This is the stress difference between the end and the start of a temperature cycle (+ 25 $^oC$ ... - 40 $^oC$ ... + 125 $^oC$ ... + 25 $^oC$). As it is well known the electrical behaviour of semiconductor devices is stress dependent (eg [2]).

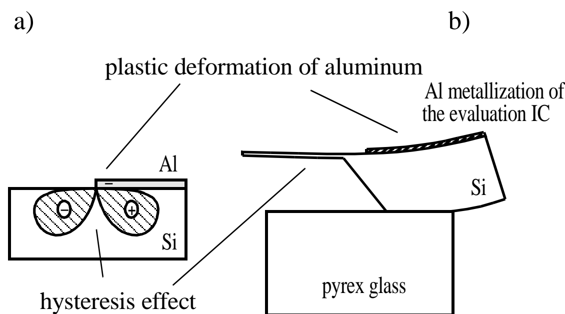


Fig. 2: a) Local hysteresis of an aluminum edge and b) global hysteresis of the chip package

We distinguish between local and global temperature hysteresis effects. The local stress is caused by edges and corners of aluminum films/stripes. Figure 2a) shows a typical substrate stress distribution at a film edge [3]. The global effects are due to the bending of the whole chip after mounting and packaging (figure 2b)).

In order to minimize the hysteresis effects of the bridge voltage we applied the EFS analysis. As MP we used the material properties of Al and all other geometrical parameters like electrical circuit geometries, thickness of aluminum, chip length, membrane dimensions, wafer thickness, and pyrex glass geometry. Table 2 shows the influence of the different MP on the temperature hysteresis.

Tab. 2: EFS of temperature hysteresis of the pressure sensor

| **MP** | **EFS optimized design** | **EFS non optimized design** |
|---|---|---|
| chip geometry | 0.123 | 0.495 |
| glass geometry | 0.087 | 0.125 |
| remanent stress | 0.026 | 0.221 |

It is not possible to design the whole sensor in a way that the temperature hysteresis tends to zero since there are optimization limits due to chip size, sensitivity, linearity, but also due to other parameters. Therefore it turns out to be necessary to compensate this undesired effect. The used compensation structure consists of an additional compensating resistor with a metal stripe nearby which is connected in series to each of the bridge resistors. The influence of these resistors on sensor sensitivity should be as small as possible (small resistance). So we had to choose a compensation structure producing high local remanent stress.

The monitoring of remanent stress together with the necessity to examine the influence of film edge induced local thermomechanical stress on resistors (eg compensation structures) and transistors have lead to the design of several test structures.

### Test Structures

In order to examine the effects of local stress on resistors and transistors we used matching structures such as a resistive voltage divider or a current mirror, which geometrical

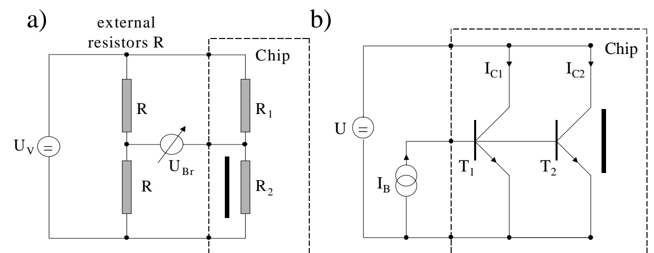


Fig. 3: Measurement principles: the black bars symbolize the additional mechanical structure like a metal stripe.

symmetry is broken: one resistor $R_2$ or transistor $T_2$ has for example an additional metal stripe nearby while the other $R_1$, $T_1$ has not (see „chip“ in figure 3a),b)). We observed that the film stresses can cause a highly temperature dependent mismatch of the voltage divider and current mirror.

Two structures shown in figures 5b), 6b) are both suitable for either compensating or measuring temperature hysteresis. To achieve high resolution in the change of resistivity we took the voltage divider on the chip and connected it to an ideal external voltage divider as shown in fig. 3a). The measured bridge voltage $U_{Br}$ of that device is given by:

$$U_{Br} = \frac{U_V}{2} \cdot \frac{R_2 - R_1}{R_1 + R_2} \tag{3}$$

The relative change of $R_2$ which is caused by the remanent film stress of the aluminum is approximately

$$\frac{\Delta R_2}{R_2} \approx 4 \cdot \frac{\Delta U_{Br}}{U_V} \tag{4}$$

The relative change of resistance caused by mechanical stress is [1]

$$\frac{\Delta R}{R} = \pi_L \cdot \sigma_L + \pi_T \cdot \sigma_T \tag{5}$$

Using equation (4) and (5) the mean value of the remanent substrate stress $\sigma_{rs}$ can be expressed in terms of the change of the bridge voltage:

$$\sigma_{rs} \approx \frac{4}{\pi_T} \cdot \frac{\Delta U_{Br}}{U_V} \tag{6}$$

The geometry of resistor and metal has been chosen in a way that makes it possible to neglect the longitudinal stress. Experimental results of different test structures are shown in figures 5, 6.

In the following we check whether the remanent substrate stress $\sigma_{rs}$ is mainly caused by the remanent film stress $\sigma_{rf}$ or by the scattering of other MP. It is important to ascertain the resolution of remanent film stress which can be achieved with different test structure geometries. For this we used EFS analysis. The chosen FP is $\sigma_{rs}$ which is proportional to $\sigma_{rf}$ and depends on about 20 MP. The partial derivatives of $\sigma_{rf}$ at different WP were calculated by FE simulations. In order to calculate the EFS values the relation

$$ATB = \sigma_{rs}\big|_{WP} \cdot r \tag{7}$$

is used. If $\Sigma_{sq}EFS_i = 1$, 99.73% of the test structures have the resolution r. We define this to be the resolution of the test structure.

The EFS analysis indicates clearly the critical MP of the test structures. Table 3 shows the EFS-values for several designs. In the case of geometry 1 it is obvious that the layer thickness of Al is the only critical parameter using big widths of stripes (WP1, WP2).

Tab. 3: EFS values of different designs (layer system Al1/ZN). WP1, WP2: geometry 1 WP3: geometry 2. EFS values are calculated with r = 10%

| | **EFS WP1** | **EFS WP2** | **EFS WP3** |
|---|---|---|---|
| WP1/2 width of stripe [µm]<br>WP3 distance film edge<-> resistor [µm] | 20 | 40 | 40 |
| width of resistor [µm] | 5 | 5 | 5 |
| **MP** | $\sigma_{rs}$ | $\sigma_{rs}$ | $\sigma_{rs}$ |
| layer thickness Al | 0.6 | 0.69 | 1.1 |
| other layer thicknesses | 0.76 | 0.23 | 0.9 |
| material properties | 0.64 | 0.14 | 1.38 |
| other geometry parameters | 0.06 | 0.04 | 1.83 |
| Σsq(EFS) | 1.16 | 0.74 | 2.7 |
| resolution r [%] | 11.6 | 7.4 | 27 |

## Evaluation Circuit

A sensitivity analysis has shown that the most critical part in the circuit is the V/I-signal amplifier. In order to take into account the hysteresis effects in our SABER simulations, different threshold voltages of matching transistors and different values of matching resistors had to be simulated. We got these values from measurements of the described test structures (fig. 3) [4].

## RESULTS

The main result is shown in figure 4. The temperature hysteresis of the sensor could be reduced by at least a factor of four.

a) b)

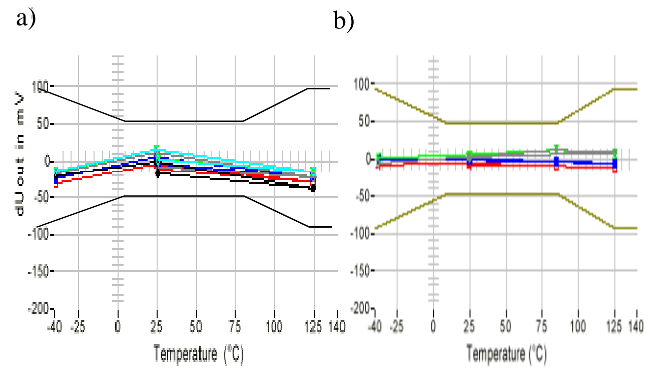


Fig. 4: Typical sensor characteristics for the a) non optimized and b) optimized sensor design

The experiments and simulations show, that the test structures with the resistors under the metal stripes (fig. 5) are more sensitive to remanent stress than the structures with the resistors beside (fig. 6). From calculation of the

EFS values it is deduced that $\sigma_{rs}$, caused by the structures of geometry 1, is much more insensitive to process scattering of the MP than the others (table 3). These facts suggest to use the structures of geometry 1 for measuring and compensating remanent stress/hysteresis effects.

As can be seen in figure 6 for example we obtained a quantitative relation between remanent stress and distance. Distances larger than 50 microns cause less than 0.1% resistivity change. The value of remanent stress obtained from FE simulations is about 100 MPa.

For the npn transistors with different metallization geometries we got results as shown in figure 7. A hysteresis in the current gauge of about 1% is due to the plastic deformation of aluminum.

The measurements of the test structures have lead to simple layout rules which are used in the above mentioned critical regions: 1) as less metal as possible in the immediate vicinity of current mirrors, 2) symmetric layout of the metal wires, 3) the use of p-diffused 45° (010)-oriented Si resistors (figure 6). As an important result temperature hysteresis of the IC could be reduced drastically as shown in figure 4.

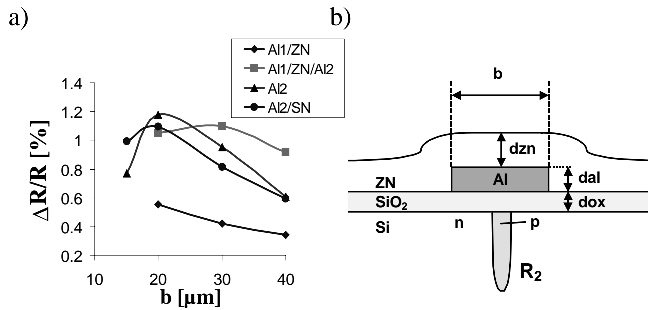


Fig. 5: Test structure with resistors under the metal stripe (**geometry 1**). a) experimental results of different layer systems b) layer system Al/ZN

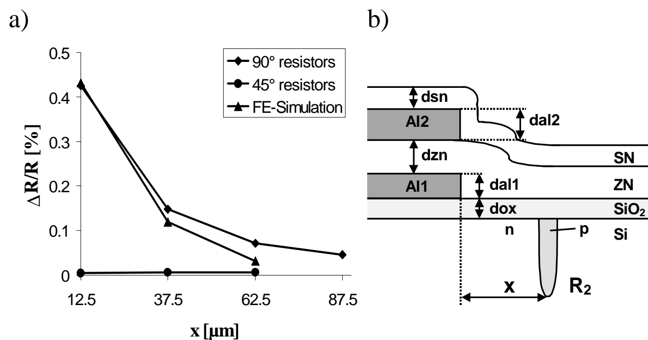


Fig. 6: Test structure with resistors beside the metal stripe (**geometry 2**). a) experimental results, simulated results were calculated choosing $\sigma_{rf}$ = 100 MPa. b) layer system Al1/ZN/Al2/SN

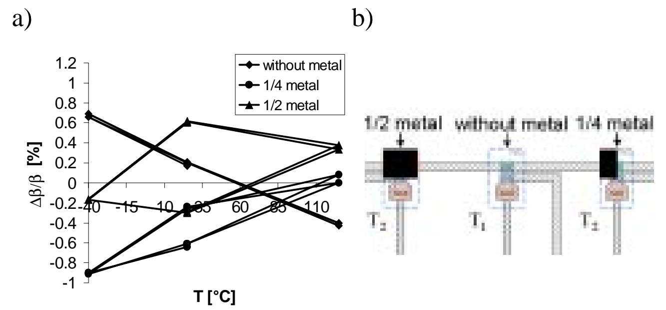


Fig. 7: a) Hysteretic behaviour of npn transistors with different additional metal geometries. b) Layout of the different npn transistors

## SUMMARY

We have shown that the temperature hysteresis of the integrated piezoresistive sensor (sensor and evaluation IC) can could be reduced by at least a factor of four. The improvement was mainly achieved using EFS analysis and special test structures.

The test structures were designed in order to examine the influence of local hysteresis effects on the properties of resistors and transistors. Structures could be found to compensate a certain amount of sensor temperature hysteresis which was left after design optimization of the sensor. Additionally we derived simple circuit layout rules from test structure results.

It could also be shown that it is possible to determine the remanent stress of the aluminum layers from electrical measurements. The method of EFS analysis is a powerful tool to optimize such test structures.

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