Measuring and Characterizing Sub-Micron Short Channel LDD MOSFETs

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ABSTRACT

An efficient model for accurate prediction of the I-V characteristics of submicrometer LDD MOSFET is described in this paper. The model is based on n-th power law model[1] by treating the effective electrical channel length $L_{eff}$ and source-drain external resistance $R_{sd}$ as gate bias dependent in the LDD MOSFET. On the other hand, our experiment shows that the channel length modulation $\lambda_0 (V_{BS}=0v)$ also to be gate-bias dependent.

Through these improvement: gate-bias dependent $L_{eff}$, $R_{sd}$ and remodeled $\lambda_0$, comparison between the measured and modeled I-V characteristics shows excellent agreement for a wide range of channel lengths and biases.

Keywords: Modeling, Lightly Doped Drain (LDD), Effective Channel Length, Source and Drain Series Resistance

EXPERIMENT AND MODEL DEVELOPMENT

Four n-channel LDD devices with mask level gate width of 20µm and mask level gate length of 2.0µm, 1.0µm, 0.5µm and 0.35µm are used for the model parameters extraction. On the other hand, the n-channel LDD devices with mask level gate length of 1.0µm 0.35µm and 0.25µm are used to demonstrate the curve fitting of $I_{ds}$-$V_{ds}$ characteristics. All the devices used in here are fabricated by Character Semiconductor Manufacture by 0.35µm process.

For a LDD MOSFET, the device can be considered as an intrinsic MOS device in series with two resistors $R_s$ and $R_d$[2], as shown in Figure 2, where $R_s$ and $R_d$ are the series resistance at source and drain terminals respectively. $V_{ds}^*$ and $V_{gs}^*$ are the internal drain and gate bias applied to the intrinsic channel region, while: $V_{ds}^* = V_{d}^* - V_{s}^*$, and $V_{gs}^* = V_{g} - V_{s}^*$. The bias differences between the internal bias $V_{ds}^*$, $V_{gs}^*$ and the external biases $V_{ds}$ and $V_{gs}$ are consumed across the extrinsic overlap region given by:

$$V_{ds}^* = V_{ds} - I_{d} (R_d + R_s)$$  \hspace{1cm} (1)

And:

$$V_{gs}^* = V_{gs} - I_{ds} R_s$$  \hspace{1cm} (2)

Thus, by modifying the “ n-th power law ” and taking the effect of source-drain series resistance into account, we propose that the model equations for LDD MOSFETs should be written as;

$$V_{DSAT} = K (V_{gs} - V_{th}) (I_{DSAT} R_s)^m$$  \hspace{1cm} (3)
\[ I_{DSAT} = \frac{(W/L_{eff})^n (V_{gs} - V_{th})}{(V_{ds} - V_{DSAT})} R_s \]

(4)

\[ I_d = I_{DSAT} \frac{(1+ \lambda V_{ds})}{(1+\lambda R_{SD} / L_{eff})} \]

\((V_{ds} \geq V_{DSAT}, \text{Saturation Region})\)

(5)

\[ I_d = I_{DSAT} (1+ \lambda V_{ds}) \frac{(2-V_{ds}/V_{DSAT})}{(V_{ds}/V_{DSAT})} \]

\((V_{ds} < V_{DSAT}, \text{Linear Region})\)

(6)

\[ R_{sd} = \alpha + R_s + R_d \]

\(\lambda = \lambda_0 \cdot V_{gs} \cdot \lambda = \lambda_0 \) (While \(V_{BS} = 0 \)v)

Where \(V_{gs}, V_{ds}\) are gate-source and drain-source voltage respectively, \(W\) is a channel width and \(L_{eff}\) is an effective channel length, \(V_{th}\) is the threshold voltage of the device, \(V_{DSAT}\) is the drain saturation voltage, and \(I_{DSAT}\) is the drain saturation current. \(K\) and \(m\) are the parameters which control the linear region characteristics while \(B\) and \(n\) determine the saturation region characteristics. \(\lambda_0\) and \(\lambda\) are related to the finite drain conductance in the saturated region.

The method mentioned in [2] and the “Shift and Ratio” method [3] are adopted to extract the \(V_{gs}\) dependent \(R_{sd}\) and \(L_{eff}\) respectively, and shown in Fig. 3 (a) and (b).

\(R_{sd}\) and \(V_{gs}\) can be fitted by the solid line as shown in Fig. 3 (a) by an empirical form as:

\[ R_{sd} = R_0 + R_d / (V_{gs} - V_{th})^{1.5} \]

(7)

Where \(R_0 = 57.98, R_d = 9.174, \) and \(V_{th}\) is the threshold voltage when \(V_{BS} = 0\) (\(V_{BS}\) is the bulk-source voltage). Empirical equation (7) will be used to replace the constant \(R_{sd}\) in present model.

In the same way, the curve in Fig. 3(b) shows that the change of effective electrical channel length \(L_{eff}\) with the gate-to-source bias voltage \(V_{gs}\) can be approximated by a line.

\[ L_{mask} - L_{eff} = (-0.0792)^* V_{gs} + 0.537 \]

(8)

Also, the formulation (8) will be used to replace the constant \(L_{eff}\) in the presented model.

**CURVE FITTING \(I_d-V_{ds}\) CHARACTERISTICS**

In order to demonstrate that the \(I_d-V_{ds}\) characteristics of devices with different channel lengths can be fitted approximately by the presented model, four devices with \(L_{mask} = 0.25\mu m, 0.35\mu m, 0.50\mu m\) and \(1.0\mu m\) are used in here for comparison.

In the first batch of tries, we found that the curves are fitted well except in saturation region at higher \(V_{ds}\) and lower \(V_{gs}\) values. Then, many experiments have been conducted, the reason we obtained is that in the saturation region, the channel length modulation is not only a function of drain voltage just as most of the model mentioned, the vertical electric field will also affect the channel length modulation effect. Therefore, the most convenient adjustable parameter to fit the drain current well at different \(V_{gs}\) in saturation region is the parameter \(\lambda_0\). Thus the parameter \(\lambda_0\) is regarded as an empirical fitting parameter and remodeled as:

\[ \lambda_0^* = \lambda_0 + A(V_{gs} - V_{th})^{0.5} \]

(9)

While \(A\) is an empirical fitting parameter.

When the \(V_{gs}\)-dependent \(L_{eff}, R_{sd}\) and remodeled \(\lambda_0^*\) are incorporated into the model equations, very good simulation results are obtained. Figures 4 (a), (b), (c) & (d) show the \(I_d-V_{ds}\) with \(V_{gs} = 1\)v, 1.5v, 2.5v, 3.5v. The solid lines are the measured data and the dotted points are the simulation results.

**CONCLUSION**

In this paper, a simple, accurate and effective semi-empirical \(I_d-V_{ds}\) model for sub-micron LDD device is developed based on n-th power law model with modification to the device characteristics. The current
model shows that both the external source-drain series resistance $R_{sd}$ and effective electrical channel length $L_{eff}$ are no longer a constant in sub-micron LDD device. Instead, they are functions of source-to-drain bias voltage, the dependence of $R_{sd}$ and $L_{eff}$ on $V_{gs}$ can be fitted by two equations accurately. For more accurate simulation in saturation region, a simple and empirical equation is proposed for the channel length modulation effect, which takes into account the dependence on $V_{gs}$.

As a result, a simple and accurate semi-empirical I-V model which considers the special characteristics of sub micron LDD devices is developed. It has been shown that satisfactory agreement between the measured and simulated I-V results have been achieved under a wide range of operating voltages.

REFERENCES


Figure 1(a). I-V Curve fit with nth power law model, W/L=20/1.0

Figure 1(b). I-V Curve fit with nth power law model, W/L=20/0.25
Figure 4 (a). I-V Curve fit with proposed model, W/L = 20/1.0

Figure 4 (b). I-V Curve fit with proposed model, W/L = 20/0.5

Figure 4 (c). I-V Curve fit with proposed model, W/L = 20/0.35

Figure 4 (d). I-V Curve fit with proposed model, W/L = 20/0.25