Measuring and Characterizing Sub-Micron Short Channel LDD MOSFETs

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ABSTRACT

An efficient model for accurate predication of the I-V characteristics of submicrometer LDD MOSFET is described in this paper. The model is based on n-th power law model[1] by treating the effective electrical channel length L_{eff} and source-drain external resistance R_{sd} as gate bias dependent in the LDD MOSFET. On the other hand, our experiment shows that the channel length modulation λ_0 (V_{BS}=0v) also to be gate-bias dependent .

Through these improvement: gate-bias dependent L_{eff} , R_{sd} and remodeled λ_0, comparison between the measured and modeled I-V characteristics shows excellent agreement for a wide range of channel lengths and biases .

Keywords: Modeling, Lightly Doped Drain (LDD), Effective Channel Length, Source and Drain Series Resistance

INTRODUCTION

With the development of silicon MOS-VLSI technology towards sub-micron and even deep sub-micron range, precise characterization of small dimension MOSFETs and their associated circuit models becomes increasingly important for predicting the performance of VLSI circuits.

The n-th power model [1] is a simple and general model for conventional MOSFET, but using the n-th power law model for a sub-micrometer LDD MOSFET, the modeling of measured I_d - V_{ds} characteristics for small V_{ds} is a difficult task , especially at low V_{gs} value, as can be seen in Figures 1(a) & (b). Further investigation found the cause of these problems appears to be the effect of gate-voltage dependent effective electrical channel length L_{eff} and source-drain series resistance R_{sd} of LDD MOSFETs. In this paper, the current and voltage model for LDD MOSFETs will be studied again by including V_{gs}-dependent effective electrical channel length L_{eff} and source-drain series resistance R_{sd} . Secondly , the channel length modulation λ_0 (V_{BS}=0v) is further regarded as an empirical fitting parameter and modeled as V_{gs}-dependent according to the requirement of curving fitting. After this improvement, the proposed model becomes more suitable to fit the I_{ds}-V_{ds} characteristics of sub-micron LDD MOSFETs with broad range of channel lengths and wide range of biases.

EXPERIMENT AND MODEL DEVELOPMENT

Four n-channel LDD devices with mask level gate width of 20µm and mask level gate length of 2.0µm, 1.0µm, 0.5µm and 0.35µm are used for the model parameters extraction. On the other hand, the n-channel LDD devices with mask level gate length of 1.0µm 0.35µm and 0.25µm are used to demonstrate the curve fitting of I_{ds} -V_{ds} characteristics. All the devices used in here are fabricated by Character Semiconductor Manufacture by 0.35µm process.

For a LDD MOSFET , the device can be considered as an intrinsic MOS device in series with two resistors R_s and R_d [2], as shown in Figure 2, where R_s and R_d are the series resistance at source and drain terminals respectively. V_{ds}^* and V_{gs}^* are the internal drain and gate bias applied to the intrinsic channel region, while: $V_{ds}^* = V_d^* - V_s^*$, and $V_{gs}^* = V_g - V_s^*$.

The bias differences between the internal bias V_{ds}^* , V_{gs}^* and the external biases V_{ds} and V_{gs} are consumed across the extrinsic overlap region given by :

$$V_{ds}^* = V_{ds} - I_{ds} (R_d + R_s) \quad (1)$$

And :

$$V_{gs}^* = V_{gs} - I_{ds} R_s \quad (2)$$

Thus , by modifying the " n-th power law " and taking the effect of source-drain series resistance into account, we propose that the model equations for LDD MOSFETs should be written as;

$$V_{DSAT} = K (V_{gs} - V_{th} - I_{DSAT} R_s)^m \quad (3)$$

$$I_{DSAT} = (W/L_{eff})*B*(V_{gs}-V_{th}-I_{DSAT}R_s)^n \quad (4)$$

$$I_{ds} = I_{DSAT}\,(1+\lambda V_{ds})/(1+\lambda I_{DSAT}R_{sd}) \quad (5)$$
$(V_{ds} \geq V_{DSAT}$, Saturaion Region)

$$I_{ds} = I_{DSAT}(1+\lambda V_{ds})\,(2-V_{ds}/V_{DSAT})\,(V_{ds}/V_{DSAT}) \quad (6)$$
$(V_{ds} < V_{DSAT}$, Linear Region)

And, $R_{sd} = R_s + R_d$

$\lambda = \lambda_0 - \lambda_1 V_{BS}$, $\lambda = \lambda_0$ (While $V_{BS} = 0v$)

Where V_{gs} , V_{ds} are gate-source and drain-source voltage respectively. W is a channel width and L_{eff} is an effective channel length. V_{th} is the threshold voltage of the device, V_{DSAT} is the drain saturation voltage, and I_{DSAT} is the drain saturation current. K and m are the parameters which control the linear region characteristics while B and n determine the saturation region characteristics. λ_0 and λ_1 are related to the finite drain conductance in the saturated region.

The method mentioned in [2] and the "Shift and Ratio" method [3] are adopted to extract the Vgs dependent R_{sd} and L_{eff} respectively, and shown in Fig. 3 (a) and (b) .

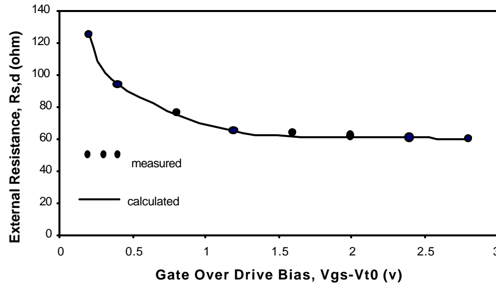

Fig. 3 (a) Variation of the extracted drain-and-source series resistance with the gate voltage.

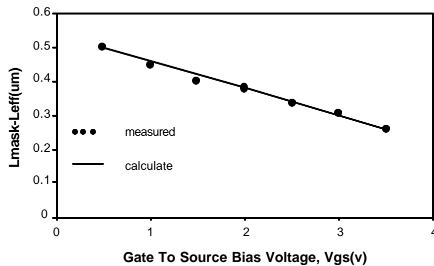

Fig. 3 (b) Dependence of the effective electrical channel length on the gate-source bias V_{gs}.

From the Fig. 3 (a), we can see that the series resistance R_{sd} is a function of the gate-source voltage V_{gs}, while V_{t0} is the threshold voltage when $V_{BS}=0$ (V_{BS} is the bulk-source voltage) . Further study found that the relationship between R_{sd} and V_{gs} can be fitted by the solid line as shown in Fig.3 (a) by an empirical form as :

$$R_{sd} = R_0 + R_1 / (V_{gs} - V_{t0})^{1.5} \quad (7)$$

Where $R_0 = 57.98$, $R_1 = 9.174$, and V_{t0} is the threshold voltage when $V_{BS} = 0$ (V_{BS} is the bulk-source voltage). Empirical equation (7) will be used to replace the constant R_{sd} in present model.

In the same way, the curve in Fig. 3(b) shows that the change of effective electrical channel length L_{eff} with the gate-to-source bias voltage V_{gs} can be approximated by a line.

$$L_{mask} - L_{eff} = (-0.0792)*V_{gs} + 0.537 \quad (8)$$

Also, the formulation (8) will be used to replace the constant L_{eff} in the presented model.

CURVE FITTING I_{ds}-V_{ds} CHARACTERISTICS

In order to demonstrate that the I_{ds}-V_{ds} characteristics of devices with different channel lengths can be fitted approximately by the presented model, four devices with $L_{mask}=0.25\mu m$, $0.35\mu m$, $0.50\mu m$ and $1.0\mu m$ are used in here for comparison.

In the first batch of tries, we found that the curves are fitted well except in saturation region at higher V_{ds} and lower V_{gs} values. Then, many experiments have been conducted, the reason we obtained is that in the saturation region , the channel length modulation is not only a function of drain voltage just as most of the model mentioned , the vertical electric field will also affect the channel length modulation effect. Therefore, the most convenient adjustable parameter to fit the drain current well at different V_{gs} in saturation region is the parameter λ_0. Thus the parameter λ_0 is regarded as an empirical fitting parameter and remodeled as :

$$\lambda_0^* = \lambda_0 + A*(V_{gs}-V_{t0})^{-0.5} \quad (9)$$

While A is an empirical fitting parameter.

When the V_{gs}-dependent L_{eff}, R_{sd} and remodeled λ_0^* are incorporated into the model equations, very good simulation results are obtained. Figures 4 (a),(b),(c) & (d). show the I_{ds}-V_{ds} with V_{gs} =1v, 1.5v, 2.5v, 3.5v. The solid lines are the measured data and the dotted points are the simulation results.

CONCLUSION

In this paper, a simple, accurate and effective semi-empirical I_{ds}-V_{ds} model for sub-micron LDD device is developed based on n-th power law model with modification to the device characteristics. The current

model shows that both the external source-drain series resistance R_{sd} and effective electrical channel length L_{eff} are no longer a constant in sub-micron LDD device. Instead, they are functions of source-to-drain bias voltage , the dependence of R_{sd} and L_{eff} on V_{gs} can be fitted by two equations accurately. For more accurate simulation in saturation region, a simple and empirical equation is proposed for the channel length modulation effect, which takes into account the dependence on V_{gs}.

As a results, a simple and accurate semi-empirical *I-V* model which considers the special characteristics of sub micron LDD devices is developed. It has been shown that satisfactory agreement between the measured and simulated I-V results have been achieved under a wide range of operating voltages .

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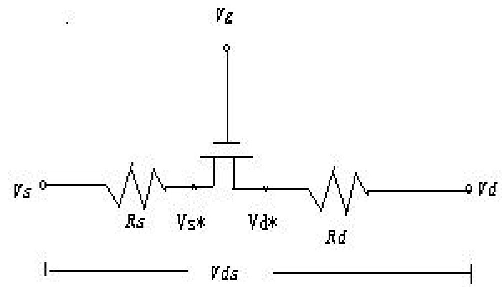

Fig.2 The equivalent circuit of LDD MOSFETs

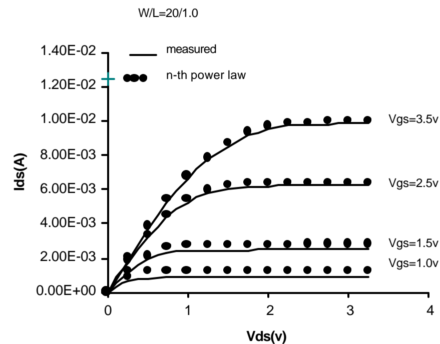

Figure 1 (a). I-V Curve fit with nth power law model,W/L=20/1.0

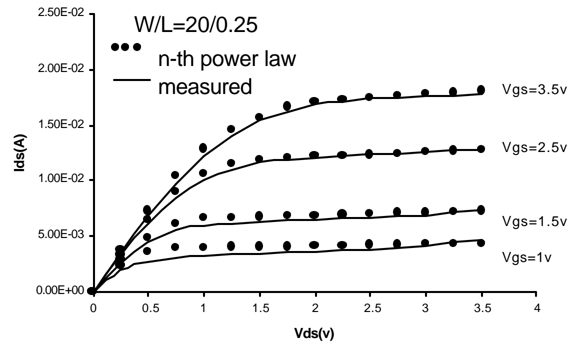

Figure 1(b). I-V Curve fit with nth power law model,W/L=20/0.25

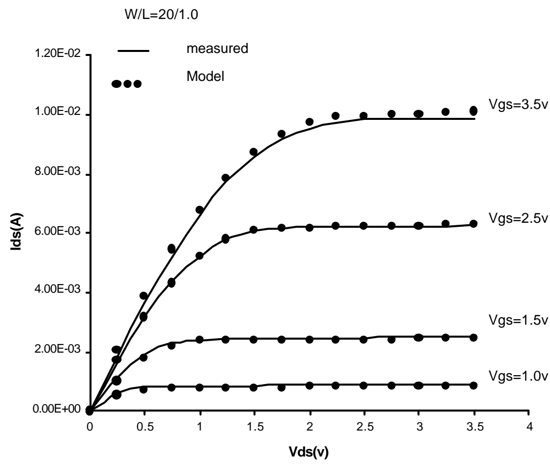

Figure 4 (a). I-V Curve fit with proposed model,W/L=20/1.0

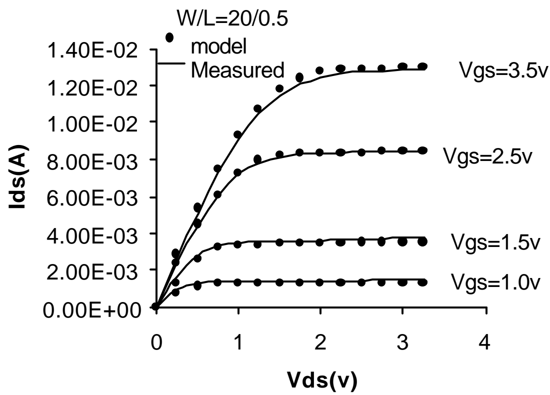

Figure 4 (b). I-V Curve fit with proposed model,W/L=20/0.5

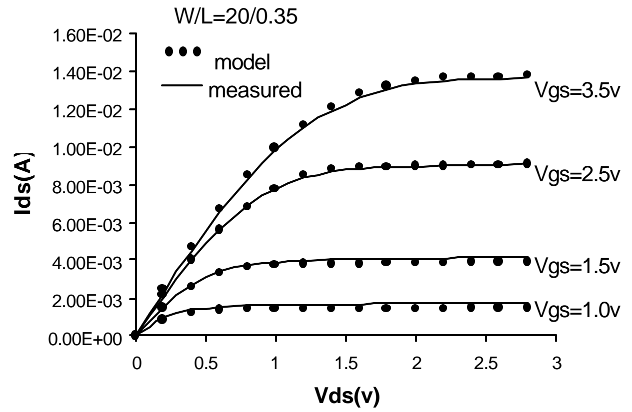

Figure 4 (c). I-V Curve fit with proposed model,W/L=20/0.35

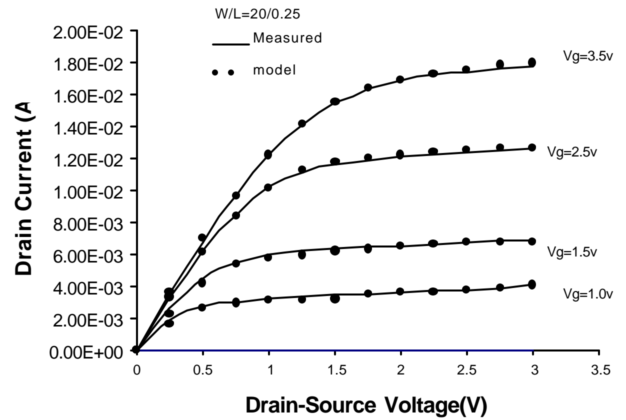

Figure4 (d). I-V Curve fit with proposed model,W/L=20/0.25