Self Aligned Gate JFETs for Smart MEMS

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ABSTRACT

Self Aligned Gate JFET (SJFET) devices and circuits are reported. The problem of electrical isolation between devices on the same chip is realized through Self Aligned Gate approach, enabling the application of standard bipolar discrete device technology (no epitaxy etc.). SJFET structures and circuits are analyzed by 2D numerical device simulation. SJFET differential amplifier circuit modeling is reviewed as an example. On the basis of modeling, test SJFET structures were designed and fabricated. Measurements on test SJFET structures reveale reasonable agreement with modeling.

Keywords: JFET, self aligned gate, device isolation, smart sensors, MEMS.

INTRODUCTION

Different FET structures are gaining on popularity in MEMS world due to their pecularities such as low noise, radiation hardness etc.[1]. Basic properties of Self Aligned Gate (SAG) JFETs, shortly SJFETs, will be given in the paper. Basic SJFET device structure is presented in Fig.1. The most interesting feature of this approach, the solution for electrical isolation between devices enabling integration, is based on a simple approach compatible with standard discrete bipolar technology. Device isolation principle is shown in Fig.2. Modeling of SJFET devices and circuits with a 2D numerical simulator will also be reported. Test SJFETs were fabricated and characterisation results will be reported and discussed.

SELF ALIGNED GATE JFET

Basic SJFET device structure is presented in Fig.1. It is a standard JFET structure, in this case with P-channel (SPJFET) as an example.

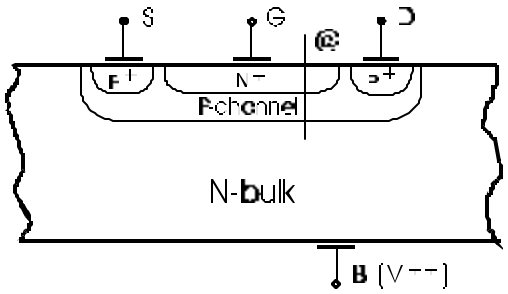

Figure 1: Basic JFET device structure

To provide electrical isolation of this device from other devices on the same chip, we suggest the solution with Self Aligned Gate. In this case N^+-Gate is diffused through the same opening as the preceding P^+-channel diffusion. The lateral cross-section through the channel (marked by @ in Fig.1) is shown in Fig.2.

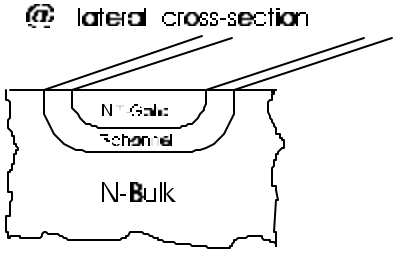

Figure 2: Lateral cross-section through the channel

If bulk electrode (B) is on the highest possible positive potential as shown in Fig.1, there will be an electrical isolation between different devices on the same chip. The situation is similar to device isolation in epitaxial bipolar integrated circuits: reverse biased PN junction surrounding the device will provide its depletion layer that is depleted of

mobile charge carriers. Depletion layer is therefore acting like an insulator layer, providing thus electrical isolation.

Typical SJFET layout for the case of W/L ratio 10 is presented in Fig.3. Fabricated test devices were designed following the rules given in the layout in Fig.3.

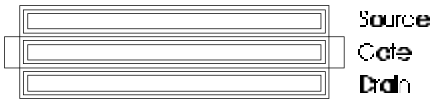

Figure 3: SJFET layout

Typical doping profile through the channel (path marked as @ in Fig.1) for the case of a PJFET is shown in Fig.4. P-channel junction is at 0.60µm and N^+-Gate junction is at 0.30µm, resulting in P-channel thickness d = 0.30µm. Peak channel doping in this case is around $8.10^{17}cm^{-3}$.

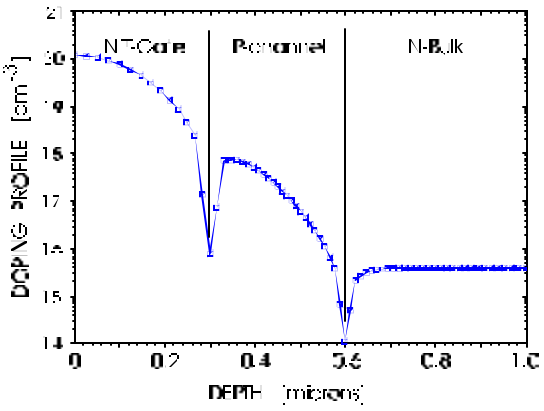

Figure 4: Doping profile through the channel for PJFET

DEVICE MODELING

JFETs described in the previous section were analyzed by device modeling with 2D numerical simulator MEDICI. Modeling was performed for room temperature (300K). Calculated SPJFET characteristics for the device presented in Fig.1, and for doping profile shown in Fig.4, are presented in Fig.5. Due to device isolation explained in previous section, bulk voltage is hold on a maximal fixed positive value (V_{BS} = +5V in this case). Channel length is in this case L = 5µm. Current is calculated per micrometer of structure width. Therefore, for channel width W=100µm the current scale is in [mA]. As can be observed in Fig.5, pinch-off voltage is in this case U_P = 2.5V.

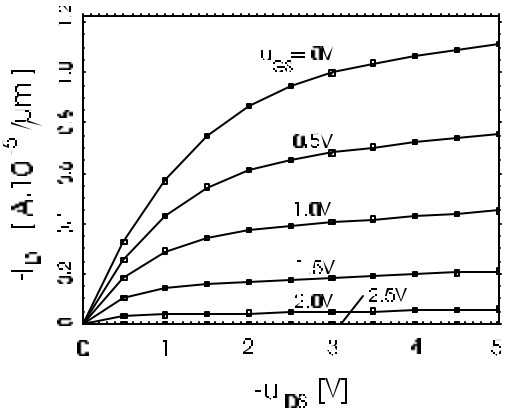

Figure 5: Calculated PJFET characteristics (V_{BS} = +5V in this case).

Accurate insight into the device operation can be gained by analyzing the distribution of different quantities of importance through the structure. As an example, JFET structure together with current flow (arrows in log scale!), depletion layers and equipotentials (smaller separations indicates regions of higher electric fields) is presented in Fig.6. Light coloured regions are P-type and dark regions are N-type. Large channel current and related crowding in nondepleted region of the channel can be clearly seen as well as small leakage currents (log scale) going into the bulk. All dimensions are given in micrometers [µm].

In cases where leakage is too large for adequate device isolation (photogeneration in photodevices, impact generation in radiation detectors etc.), the fabrication of SJFET devices and circuits on thin micromachined membranes[2] instead on bulky wafers seems to provide low leakage, due to its proportionality to silicon thickness. Processing in this case is similar to the fabrication of silicon piezoresistive pressure sensors[3].

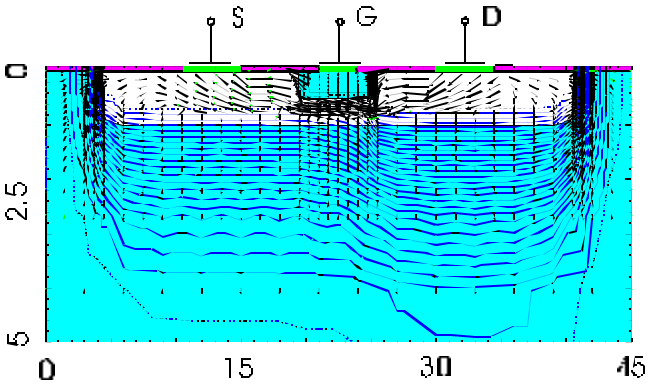

Figure 6: JFET structure, current flow, depletion layers and equipotentials

CIRCUIT MODELING

Device simulation is followed by circuit simulation. In our case, circuit simulation is a direct continuation of the device simulation. Several circuit properties at 300K are studied to get insight into the SJFET circuits operation as well as into the modelling capabilities. In the following, circuit modeling approach and some of the simulation results will be reviewed.

In this circuit simulation section, we apply 2D numerical simulator MEDICI's Circuit Analysis Advanced Application Module /CA AAM/[4] that joins together SPICE like circuit analysis with 2D numerical device modeling. Circuit Analysis AAM in MEDICI, combining simulations of two independent JFETs together with lumped circuits elements (resistors, capacitors etc.) is used for the analysis of a differential amplifier circuit performance.

Differential amplifier circuit under observation, as introduced into the numerical simulator, is presented in Fig.7 and its semiconductor structure in Fig.8. It is a standard two input, one/two output differential amplifier circuit, based on PJFETs from previous section. Therefore, active transistors $JFET_1$, $JFET_2$ are PJFETs described in the preceding chapter, the other circuit components are input gate supply voltages $V_{G1} = V_{G2} = +0.5V$, common drain supply voltage $V_{DD} = -5V$, bulk voltage $V_B = +5V$, drain resistances $R_{D1} = R_{D2} = 150kOhm$ and current generator resistance $R_g = 75kOhm$.

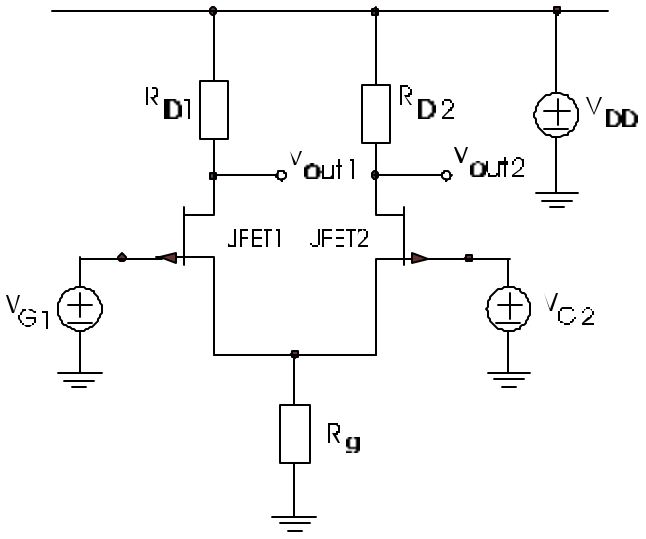

Figure 7: Differential amplifier circuit

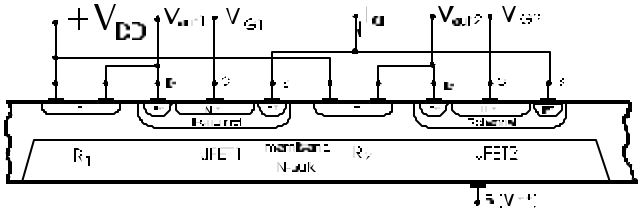

Figure 8: Semiconductor structure of the differential amplifier

Using described features of MEDICI, static operation of differential amplifier circuit is studied by applying voltage ramp for $v_{in} = v_{G1}$ varying from 0.5V to 0.8V. The response, calculated DC transfer characteristics v_{out1} , v_{out2} vs. $v_{in} = v_{G1}$ of the amplifier circuit, are presented in Fig.9.

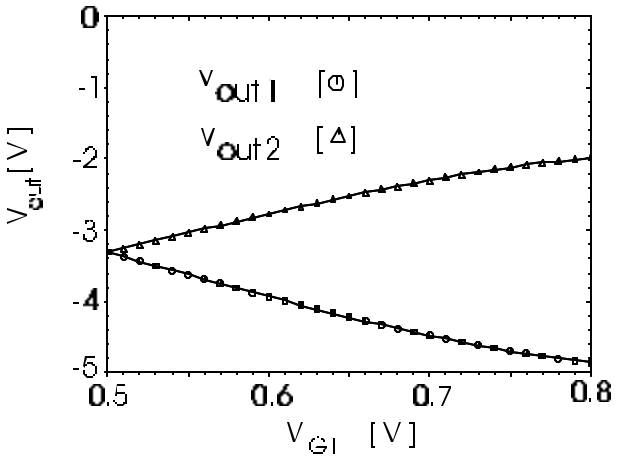

Figure 9: Calculated voltage transfer characteristics of the differential amplifier ($v_{in} = v_{G1}$, $V_{DD} = -5V$, $V_{BS} = +5V$)

All simulations were performed on HP Apollo 9000/720 system. As an indication of the computer time consumption, CPU time needed for complete circuit analysis of the differential amplifier voltage transfer characteristics in Fig.9 is around 20 minutes.

EXPERIMENTAL

Test SJFET structures were fabricated following the layout shown in Fig.3. Starting material were N-type silicon wafers, Phosphorus doped, N_D = 4.10^{15} cm^{-3}, one side polished, orientation (100).

SJFET test structures were fabricated by standard bipolar discrete device technology. Special attention during the fabrication process was paid to low pn-junction leakage currents[5] to assure good device isolation.

First, source and drain regions were fabricated. Then, P-channel was fabricated. This was followed by N^+-gate fabrication. Here, the crucial step in the proposed process for the SJFET fabrication is performed: selective thin/100nm/-thick/500nm/ oxide etch, resulting in SAG fabrication by N+-Gate diffusion into P-Channel, through essentially the same oxide window in the channel (Figs.1,2 cross-section).

Different SJFET test structures were designed and fabricated, for various channel lenghts(L) and channel width(W) vs. length(L) ratios(W/L). In Fig.10, the structure of a fabricated test SJFET (channel length L = 40μm, channel width W = 400μm) is shown.

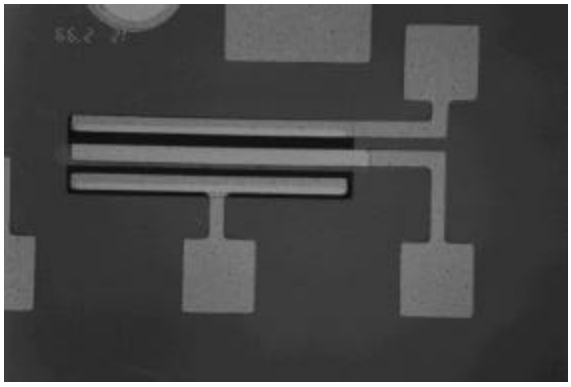

Figure 10: Fabricated test SJFET (channel length L = 40μm, channel width W = 400μm)

MEASUREMENTS

DC characterisation of fabricated test SJFET structures was performed with parametric analyzer HP4145B. Measured characteristics for test SJFET (channel length L = 40μm, channel width W = 400μm) are presented in Fig.11. The measured characteristics are in reasonable agreement with modeling results.

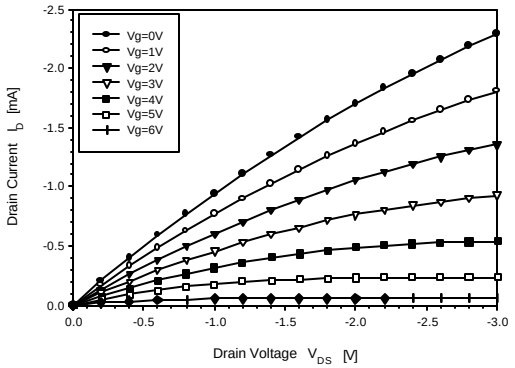

Figure 11: Test SJFET measured characteristics

CONCLUSION

Self Aligned Gate JFET (SJFET) devices and circuits are reviewed. Electrical isolation between devices on the same chip is realized through the Self Aligned Gate approach. By this approach, electrical isolation of the devices on one chip, enabling integration is realized with simple, bipolar discrete device technology (without epitaxy or similar).

To get a deeper insight into the electrical operation, SJFET structures are analyzed by 2D numerical simulation. This is followed by circuit modeling with 2D device modeling simulator MEDICI. Therefore, circuit modeling in this case is a direct continuation of the device modeling, enabling thus the exact analysis of circuit properties, in dependence of basic semiconductor device structural parameters (geometry, doping profiles etc.). As an example, SJFET differential amplifier circuitmodeling is reviewed.

On the basis of modeling, test SJFET structures were designed and fabricated. Measurements on test SJFET structures revealed reasonable agreement with modeling.

ACKNOWLEDGMENT

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REFERENCES

[1] D.Krizaj, W.Bonvicini, S.Amon, “FOXFET structure – device modelling and analysis” .Nucl.Instr.Meth.Phys.Res., Sect.A, Accel., pp.482-490, 1997.

[2] D.Resnik, U.Aljancic, D.Vrtacnik, S.Amon, ”A new approach to silicon bulk micromachining”. Proc. MELECON’98, pp.330-334, Tel Aviv, Israel, 1998.

[3]U.Aljancic,D.Resnik,D.Vrtacnik,S.Amon, “Overpressure protection in silicon low-pressure sensor”. Proc. Int.Conf.Microel. MIDEM’96, Ljubljana, Slovenia, 1996.

[4] "TMA MEDICI", TMA, Palo Alto, CA, USA, 1992.

[5] D.Resnik, D.Krizaj, D.Vrtacnik, U.Aljancic, S.Amon,”Impact of process parameters on leakage current of pin detector structures”. Proc.Midem’97, pp.197-202, Gozd Martuljek, Slovenia, 1997.