Modeling of Stress Induced Hysteresis in piezo-resistive Analysis

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ABSTRACT

The impact of mechanical stress on electrical characterizations of microelectronic circuitry is a major design issue in development of sensors and integrated micro-electro-mechanical systems. Because the electrical properties of semiconductors are influenced by external and thermally induced mechanical stress, the magnitude of such effects should be analyzed during the design process. Such non-linear and hysteresis effects can be modeled and analyzed using state-of-the-art technology CAD (TCAD) tools, providing information about device characteristics prior to production.

Keywords: Piezo-resistivity, stress compensation, technology CAD, integrated simulation environment

INTRODUCTION

Mechanical stress distributions induced by operating conditions or by the fabrication process generally alter the electrical properties of diffused and implanted resistors and transistors due to the piezo-resistive effect. Under certain conditions, thermo-mechanical loads may also permanently alter the stress distribution acting on the micro-system structure and thus introduce an offset in device characteristics, depending on the actual load history. Examples of such undesired stress-related device behavior occur for instance during thermal cycling of doped resistive structures where a different stress distribution remains after each load cycle. Repeated cycles generally produce a hysteresis curve in the electrical device characteristics, distorting the intended device operation. In microelectronics applications, careful analysis of undesirable piezo-resistive effects can be crucial to a successful design. On the other hand, stress-compensation effects can be analyzed using the same approach. Prediction of electro-mechanical effects and analysis of appropriate design considerations are thus important steps in achieving the intended device behavior.

In a simulation of stress-induced electrical hysteresis in semiconductor structures, several rather different simulation tasks must be performed. Realistic structure and doping profile generation by process simulation must be interfaced to a thermo-mechanical load simulation, and the results must both be included in a device simulation taking the local thermo-mechanical state into consideration when solving the semiconductor equations. Specialized simulation tools interacting in an integrated technology CAD environment provide the features required for solving the complex problems outlined above as well as methods for determining an optimal set of design parameters.

PHYSICAL MODELING

Description of charge carrier transport

Electrical characterizations of semiconductor devices usually state a measure of the effective charge carrier mobility under given conditions. Physically, the mobility of charge carriers within the crystal lattice is therefore among the fundamental properties that are to be evaluated in a simulated electrical device characterization. Due to the temperature dependency of charge carrier mobilities, a simulation of the temperature distribution in the active region has to be simulated. Intrinsic heat sources can also be modeled at this stage.

The basic relations between charge carrier transport and external potentials can be expressed by Poisson's equation and a set of continuity equations for the charge carrier species ρ_i:

$$\nabla \cdot \epsilon \nabla \psi = -e \sum (\rho_i + \tilde{\rho}_i) \tag{1}$$

$$\nabla \cdot j_i = \pm e \left(R + \frac{\partial \rho_i}{\partial t} \right) \tag{2}$$

Here, $\tilde{\rho}_i$ is the density of ionized donors/acceptors, R is the charge carrier recombination rate and e is the elementary charge. The expression for the charge carrier current densities is

$$j_i = -e \rho_i \mu_i \nabla \phi_i \tag{3}$$

where the mobilities are symbolized by μ_i. Using Boltzmann statistics, the charge carrier densities can be written in terms of the effective intrinsic charge carrier densities $\hat{\rho}_i$ as

$$\rho_i = \hat{\rho}_i e^{\frac{-e(\phi_i - \psi)}{kT}} \tag{4}$$

Assuming that the charge carriers are in thermal equilibrium with the crystal lattice, an additional term must

be added to (3) accounting for charge carrier transport due to a thermal gradient:

$$j_i = -e\rho_i\mu_i\left(\nabla\phi_i + \theta_i\nabla T\right) \tag{5}$$

The thermo-electric coefficient θ_i describes the (linearized) coupling of charge carrier transport to the thermal gradient. In this expression, the temperature distribution inhomogeneities of the active semiconductor region explicitly couples to the charge carrier transport.

Piezo-resistive effect

Under influence of mechanical stress, the shape of the crystal lattice (and thus also the scattering potential) is distorted which leads to changes in transfer properties of the charge carriers. A phenomenological description of the (generally anisotropic) change in electrical conductivity σ can be expressed by augmenting the electrical conductivity by a coupling to the stress tensor Ξ:

$$j_i = -\sigma_i\left(1 + P\cdot\Xi\right) \tag{6}$$

The piezo-resistive coupling coefficients P depend on doping concentration and temperature. The number of independent coefficients reduce to three in crystals of cubic symmetry.

Inelastic deformation

Hooke's law states that the elongation ϵ is proportional to the applied force by the modulus of elasticity E:

$$\epsilon = \sigma E \tag{7}$$

The Young's modulus E can however only be regarded as being approximately constant for a restricted range of elongations. Applying loads outside of this range, either directly or induced by thermo-mechanical effects, will cause irreversible changes in the mechanical structure of the material. Such loads may influence the charge carrier transport also after the initial load has been removed. In place of the linearized assumption (7), more complex relations between strain and stress must be employed to describe the transition from the elastic to the inelastic deformation region.

Thermal expansion

A temperature change of any part of the system is generally related to a volume change of the materials. Phenomenologically, such a thermo-mechanical interaction is characterized by the thermal expansion coefficient α:

$$\epsilon = \alpha\Delta T \tag{8}$$

A mismatch between thermal expansion coefficients will generally lead to a mechanical stress condition under by temperature differences.

As additional mechanical stress during device operation mainly arise due to temperature differences and the related volume expansion, knowledge of the temperature distribution is fundamental to a physical model of loads acting on the charge carriers in a semiconductor device. A thermal simulation basically solves the heat conduction equation under influence of external conditions Q:

$$\rho c\frac{\partial T}{\partial t} - \nabla\cdot\left(\lambda\nabla T\right) = Q(t) \tag{9}$$

The coupling of the temperature distribution via mechanical stresses to charge carrier density and consequently to electrical characterizations under operating conditions can be described by the physical models and mechanisms outlined above. Their couplings and effects on the device can thus be analyzed during the device design process,

TCAD SIMULATION TOOLS

The process of designing semiconductor devices to suit a complex set of physical and electrical specifications requires an advanced environment for design analysis. In an environment based on technology computer aided design, tools for geometry generation by process simulation and process emulation as well as for simulation of the physical models are required. Due to the different scales of simulation and the nature of the partial differential equations involved in the respective physical simulations, advanced meshing tools and data exchange facilities are also required in order to pipe simulation results from one tool to another.

Common tasks to be repeatedly performed in a design environment range from geometry generation and meshing to visualization and parameter extraction. In such an environment, a command center linking the various tools together and acting as a user interface is of central importance.

Geometry generation can take place by process emulation, which uses geometrical operations to create a representation of the structure, or by process simulation, which solves the differential equations associated with the fabrication steps such as etching, diffusion and so on. An interactive editor may be used for minor design changes. A further important aspect of automated geometry generation, for instance by applying simulated fabrication steps to mask layouts, is the possibility of parameterization. In this way, the influence of quantities such as distances, layer thicknesses, doping profiles etc. on device characteristics under certain operating conditions can be investigated. Coupled with response surface fitting, the goal of a partially automated design process can be achieved.

EXAMPLE OF PIEZO-RESISTIVE ANALYSIS

The following example demonstrates the interaction of the physical models outlined above and exercises several tools offered in a TCAD environment [1].

The structure to be analyzed consists of a resistor fabricated by ion implantation or diffusion. On top of the substrate, an aluminum interconnect strip is placed right above and parallel to the embedded resistor. The metal is separated from the semiconductor region by an insulating layer. This geometry is depicted in figure 1. At ambient temperature, the aluminum is prestressed due to the manufacturing technique.

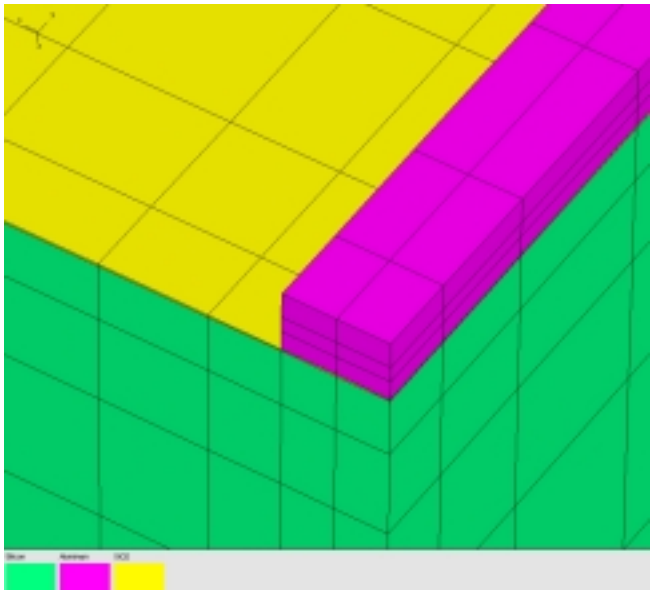

Figure 1: Aluminum line separated from doped silicon by an insulating layer. The fabrication process induces mechanical stresses in the structure, which are augmented by stresses induced by device operation. Due to symmetry, only one quarter of the structure is modeled.

The aim of the numerical simulations is to analyze the changes in resistivity of the embedded resistor due to inelastic deformations of the metal line when exposed to thermo-mechanical loads. A local contraction or expansion of the aluminum line will induce a stress distribution also in the vicinity of the metal, with the possibility of thereby changing electrical properties of the underlying resistor. If this is the case, the inelastic deformation of the metal will be related to the temperature encountered during operation, i. e. the change in electrical properties will be a function of the thermal load history of the device. A simulation of the electrical properties before and after reaching the maximum operating temperature will thus indicate the magnitude of thermo-mechanically induced electrical offset. Knowledge of such a change in resistivity could be important in assessing device specifications.

The first step in a piezo-resistive analysis using the physical model outlined above consists of evaluating the temperature- and mechanical stress distributions in the structure at given external conditions. This information is gained from solving the coupled thermo-mechanical equations (7) - (9). The stress distribution can be derived from the mechanical displacement field. Figure 2 shows a component of the mechanical stress distribution superimposed on the mechanical deformation of the structure. As can be seen from the figure, the stress distribution extends well into the embedded resistor. The simulations were carried out using the finite element based thermo-electro-mechanical simulator SOLIDIS_$_{ISE}$ [2].

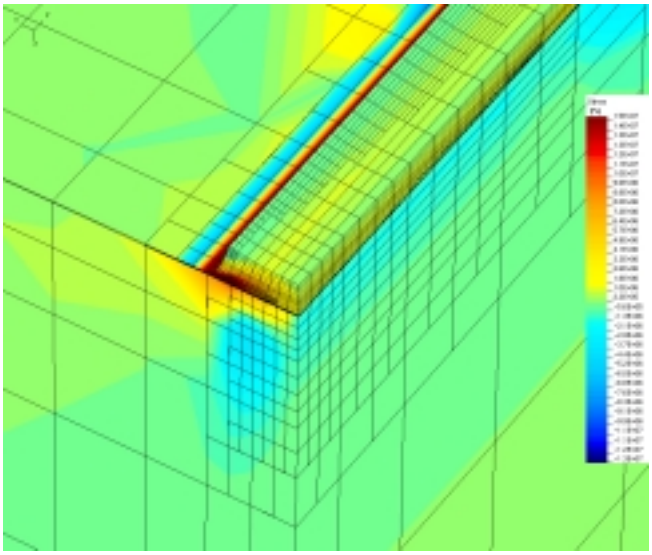

Figure 2: Mechanical deformation (scaled by a factor of 20) and stress distribution induced by thermo-mechanical loads on the structure. Adaptive mesh refinement based on the mechanical deformation energy was used in the simulation.

Next, an evaluation of the effective resistance of the resistor zone using the simulated temperature- and stress conditions can be carried out. The semiconductor device simulator DESSIS_$_{ISE}$ [3] solves the charge carrier transport equations according to the model (1) - (6). Figure 3 shows the electron current density in the resistor region evaluated under influence of mechanical stress.

On a side note, the data interpolation between the rather different meshes used in the two simulations must be mentioned. Clearly, the different physical models involved require quite different meshes for an optimal performance in terms of memory and CPU time requirements. The thermo-mechanical simulation utilized adaptive mesh refinement according to the distribution of mechanical deformation energy, while the semicon-

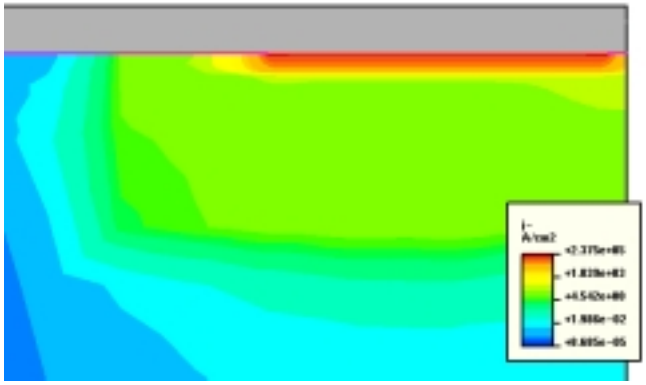

Figure 3: Electron current density in the resistor region evaluated under influence of mechanical stresses. The semiconductor simulation takes the charge carrier mobility augmented by a set of doping-related coefficients coupling charge carrier mobility to the local mechanical stress components into account when solving the equations of charge carrier transport. The color shading indicates that the largest contribution to current conduction takes place in the region affected the most by plastic deformation.

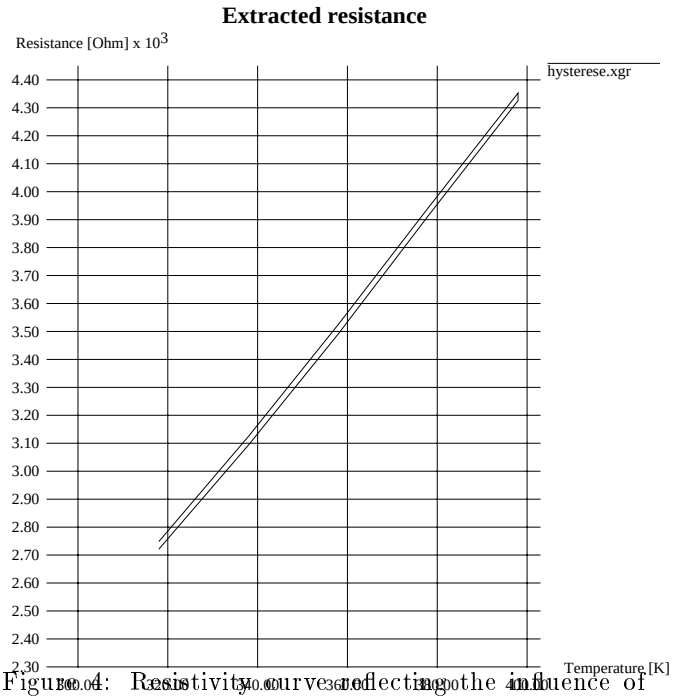

Figure 4: Resistivity curve reflecting the influence of thermo-mechanical loads on the embedded resistor. The mechanical simulation allowed for inelastic deformation.

ductor simulation was performed on a mesh based on the doping profile gradient near the substrate/insulation layer interface. Mapping of temperature- and stress data between the meshes is performed using a dedicated data interpolation tool. In this process, a reduction of problem dimensionality was also performed: The thermo-mechanical simulation was carried out in 3D, while the semiconductor equations were solved in 2D.

The effective resistivity of the semiconductor region under thermo-mechanical load can be extracted from the voltage-current relation defined by the device simulation results. Using discrete temperature steps in the thermo-mechanical simulation, the electrical characterizations of the resistor in its equilibrium stress state can be analyzed. For each temperature, the stress state of the complete structure is computed before and after imposing the maximum operating temperature on the device. The extracted resistivity curve is shown in figure 4.

The magnitude of the resistivity change in function of device geometry, material parameters and external conditions can be analyzed using an environment with job scheduling facilities [4]. All other conditions being equal, the hysteresis behavior of the resistivity must have its origin in the inelastic deformation of the structure during the initial heating phase. This was verified by a simulation with a purely elastic mechanical model, where no hysteresis of the resistivity could be observed.

CONCLUSIONS

The goal of limiting the resistivity offset induced by inelastic deformations during burn-in can be achieved by minimizing the remaining stresses in and near the resistor structure. The necessary precautions in this process can be analyzed in a parameter study by varying quantities such as metal line dimensions, oxide layer thickness as well as the relative placement of resistor and metal line. The integrated technology CAD environment [1] provides all tools required for this kind of device design analysis.

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