

Rapid Reliability Assessment Using CADMP-II

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ABSTRACT

One of the most time consuming activities in new product development is associated with reliability assessment and qualification. This is defined as a process to verify whether the anticipated reliability is indeed achieved under actual life cycle loads for some specified length of time. Reliability assessment and qualification is usually accomplished by testing under accelerated loads to achieve time compression. Typical qualification methods have been borrowed from the military, without knowledge of the rationale or assessment of the true benefits. In fact, prediction of field reliability from these tests has generally been quite poor. Nevertheless, the amount and length of qualification testing has increased over the years. This paper aims to provide a background to the qualification problem that much of industry is faced with today. Then provide an approach to reliability assessment, which provides a method for qualification requiring very little time and money, because the process is simulated.

Keywords: reliability assessment, virtual qualification, electronic packaging, accelerated testing, CADMP-II

INTRODUCTION

Until recently, reliability assessment and qualification consisted of following decades-old military and commercial standards which prescribed a series of "one size fits all" standard tests. The standards were often inaccurate, improperly applied, and unnecessarily restrictive, while the testing was costly and time consuming. In addition, the tests often did not address the actual failure mechanisms occurring in the application environment. These traditional methods are inappropriate for the qualification of the overwhelming number of high volume, commercial electronics components that are currently being inserted into high reliability and harsh environment applications.

What is needed is a radical departure from traditional qualification [1]. Success in today's globally competitive environment requires the ability to repeatedly examine and constantly improve manufacturing processing. This is as true for qualification as for any other area. Reliability assessment and qualification techniques must be questioned, evaluated, torn apart and reinvented for today's

marketplace. For next generation electronic products, it is no longer practical to design the product and then measure and improve the reliability by a series of test and fix steps at the latter stages of development. Fast and cost-effective product development requires that reliability be assessed in the earliest stages of conceptual design, with prototype testing used only to confirm that the designed-in level of reliability has been achieved. Any reliability assessment methodology for next generation electronic products must be fast and cost-effective to permit the development of products with more features and higher quality at lower cost in a time frame commensurate with today's shorter design cycles, and faster times to market and profit. Furthermore, it must be based on the fundamental mechanisms by which electronic systems fail in order to be successful. Finally, the need for concurrent engineering and increased outsourcing of device processing, component manufacturing, assembly, and test requires that the methodology be widely accepted and implemented across the supply chain.

In short, a completely new methodology for reliability assessment and qualification is needed. Such a new methodology - physics-of-failure based rapid reliability assessment - has been developed to meet these demands [2]. Physics of failure based rapid reliability assessment is based on estimating the time to failure for designs using models for the fundamental electrical, chemical, and thermo-mechanical mechanisms by which systems fail. Each model uses the environmental and operational loads, the system architecture and the system materials as the inputs. Each model consists of a stress model that describes the stress response of the system to the applied loads, and a damage model that describes the material response to the stress in the form of a number of cycles or hours to failure. Extensive testing has been used to calibrate and validate the models and confirm the results of reliability assessments.

In order to facilitate the implementation of this methodology in assessing the reliability of electronic components and modules, a set of software programs, known collectively as CADMP-II (Computer aided design of microelectronic packages II), have been created. This reliability assessment software

- assesses candidate and existing package or module designs for reliability in many different environments

using a database of fully validated physics-of-failure models

- calculates times-to-failure for the fundamental mechanisms which cause failure of IC packages and MCM-Ls housing both bipolar and CMOS based systems
- evaluates the effect of different manufacturing processes on reliability by calculating the time-to-failure as a function of typical manufacturing tolerances and defects
- facilitates the selection of cost-effective test parameters for validating the reliability assessment, thereby assisting in the design of value-added qualification processes and tests;
- facilitates the selection of high volume commercial off-the-shelf components by permitting their virtual qualification

This physics-of-failure tool is the critical element in the new reliability assessment methodology permitting virtual qualification of off-the-shelf components and allowing a design team to consider reliability assessment of modules at the initial stages of design, technology and functional definition, and supplier selection. A conservative estimate from Boeing Commercial Airplane Group indicated that the use of this tool would reduce the cost and weight of their electronic systems by up to 40% while improving the reliability.

RELIABILITY ASSESSMENT SOFTWARE

The approach to be followed in utilizing the CADMP-II software in assessing reliability is described below [3].

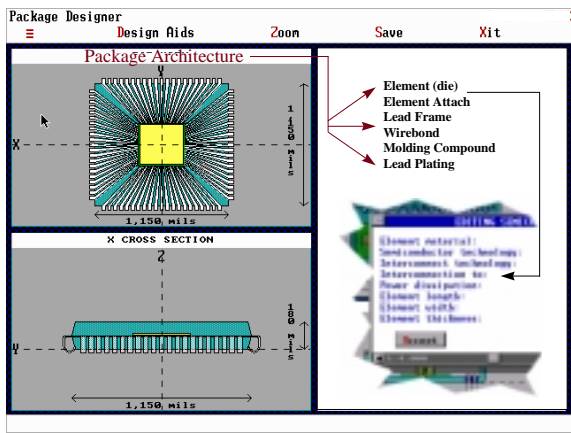


Figure 1 - The graphical package design interface for PEMs

First the structure of an IC package is defined using the package design interface depicted in figure 1. Then a thermal analysis of the package is performed. Because there is often a dependence of component and system failures on operating temperature, temperature cycle magnitude, or temperature gradients, thermal analysis is integral to design-for-reliability. This is particularly true for systems where power dissipation can considerably increase the operating temperature above ambient, such as power modules. The thermal analysis tool is based on control volume theory and uses a finite difference approach to determine the temperature distribution in the system.

After the thermal analysis is complete, the reliability assessment software is used in any one of four modes. Each of these modes is based on the fact that the heart of the reliability assessment software is a solver that calculates the time-to-failure for each potential failure mechanism model for a specific design subjected to a specific environment.

The first mode is virtual qualification of an existing commercial component design. In this mode, dominant failure mechanisms are ranked, starting with those causing failure in the shortest amount of time. This allows the user to determine the dominant failure mechanisms and the time to failure for the package. The second mode is design-for-reliability. In this mode, the effect on reliability of variations in design attributes and environmental/operational stresses is evaluated. An example of how the software is used to conduct a tradeoff between a design parameter and a stress in order to maintain the same design life is shown in figure 2.

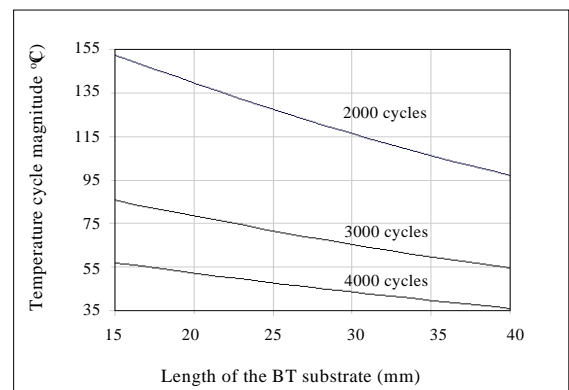


Figure 2 - Constant time-to-failure contour plot for solder joint shear fatigue in PBGAs

The results of such an analysis are used to reduce the risk of package failure by the identified failure mechanisms.

In the third mode, the software is used to develop acceleration factors relating the time to failure at accelerated test conditions to the time to failure at standard use or storage conditions. In this mode, use of the tool aids in the selection of accelerated test parameters tailored for each package design and application. In the fourth mode, the software is used to evaluate the effect of manufacturing defects on failure during use, such as the effect of die attach voids on subsequent die attach fatigue failure. It is also used to evaluate the effect of manufacturing parameters on failure during assembly, such as the effect of maximum reflow temperature on popcorn susceptibility.

Library Structure

In order to perform these functions, the reliability assessment software is equipped with extensive failure mechanism, materials, and environment/test stress libraries, which can be enhanced and updated by the user, if necessary, to address particular applications.

Materials library: The materials information required for reliability assessment is provided in a common material library format. The materials library is taken from the CALCE EPSC materials database, which is the largest and most extensive materials database for the design of electronic packages in the world. It is organized based on categories of materials used in packaging. Currently, it includes over 30 mechanical, thermal, and electrical properties for over 450 materials in 25 packaging categories.

Failure Mechanism Library: The failure mechanism library contains the models and required constants, factors, and sub-models for each failure mechanism. These models express the time-to-failure for each mechanism in terms of geometry attributes, material properties, and environmental/operational stress levels. Sub-models are used to calculate the thermo-mechanical stresses resulting from the environmental/operational stress levels. The sources, assumptions, limitations, and validation histories for each model are also provided in the library.

Environments library: Electronics design requires an accurate description of the application environments for the equipment. The software provides an environment library to contain storage, transportation, and use environments used in performing stress analysis and reliability assessment. Nine standard usage environments are included with the software.

Test/Stress Library: This library provides the opportunity to define accelerated test conditions that can be used to assess the time-to-failure of an electronic component in test. It also provides the opportunity to define typical component

environmental stress screens (ESS) that can be used to assess the fraction of the component life consumed in the screening process.

CONCLUSIONS

The reliability assessment software tool, CADMP-II, described in this paper, forms the key element in a new rapid reliability assessment and virtual qualification methodology. Use of this software allows engineers to create designs which are less expensive and quicker to market arising from the ability to specify, qualify, and optimize the use of new and less costly materials, package geometries, and manufacturing processes. It also permits them to create lower risk product designs based on up-front design for reliability. When combined with efforts in qualifying suppliers and their processes, this technique can greatly reduce the cost and time to market for new, highly reliable electronic products.

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REFERENCES

- [1] E. R. Hnatek, The metamorphosis of the component qualification process, **Proc. 43rd Annual Tech. Mtg. IES, Los Angeles, CA 1997**, pp. 130-136.
- [2] P. McCluskey, M. Pecht, and S. Azarm, "Reducing the time-to-market using virtual qualification," **Proc. 43rd Annual Tech. Mtg. IES, Los Angeles, CA 1997**, pp.148-152.
- [3] **CADMP-II v. 2.2. Reference and Validation Manual**, CALCE EPSC Electronic Components Alliance, College Park, MD, 1998.