A Simple VLSI Spherical Particle-Induced Yield Predictor

K. Nakamae, H. Ohmori and H. Fujioka

Department of Information Systems Engineering, Osaka University
2-1Yamada-Oka, Suita, Osaka 565-0871, Japan
{nakamae, ohmori, fujioka}@ise.eng.osaka-u.ac.jp

ABSTRACT

A simple VLSI particle-induced yield predictor has been developed that allows us to predict the entire yield of VLSI and also to analyze the bottleneck processing steps and faults. Particles with spherical shape are generated in the production equipment for each VLSI processing step and are deposited on the wafer. The yield predictor accepts as inputs (a) layout description of the VLSI under analysis in GDS II format, (b) production flow data, (c) planned layer thickness data, and (d) particle parameters for each production equipment. The predictor was applied to 16Mbit DRAM to show its validity.

Keywords: yield predictor, integrated circuit manufacturing, simulation, particle-induced yield

INTRODUCTION

With an advance in the LSI manufacturing, VLSI products have been highly integrated. Along with an increase in integration, particles have become a major fraction of the cause that determines the yield of VLSI [1]. Thus to reduce the number of particles and the size of particles is a serious problem. Though VLSIs are manufactured in the super clean room, it is reported that the source of particles does not exist in the atmosphere, but generates in the production equipment. Since the VLSI manufacturing process consists of various kinds of equipment with different numbers and sizes of particles, it is difficult to predict particle-induced yields.

Recently, Khare and Maly have reported the contamination-defect-fault relationship where failure mechanism models are developed and presented which can be used to accurately estimate probability of different failures for a given IC [2]. However, given the large amount of memory and simulation time required by their Monte Carlo simulator to simulate the entire fabrication sequence in details, it is possible to simulate only small portions of the IC.

We have evaluated the testing process after the wafer fabrication through simulation analysis [3].Å@In this paper, we propose a simple VLSI particle-induced yield predictor that allows us to predict the entire yield of VLSI and also to analyze the bottleneck processing step and faults.

YIELD PREDICTOR

In the development of yield predictor, we assume that particles with spherical shape are generated in the production equipment for each processing step and are deposited on the wafer. Particles for each equipment are modeled as the Gamma distribution for particle size [4], the Poisson distribution for generated number of particles and the uniform distribution for the position of particle deposited on the wafer. The effects of particles for layer formation, photolithography, layer etch, cleaning, and so on are modeled simply by using the planned layer thickness data. Example is shown in Fig. 1 where etching, resist stripping, and cleaning steps are carried out in sequence. In the cleaning equipment, it is assumed that 90 % of particles on the wafer can be removed but particles pour on the wafer newly in the equipment. The conductivity of particles is also considered.

As particle-induced faults, we consider the active area

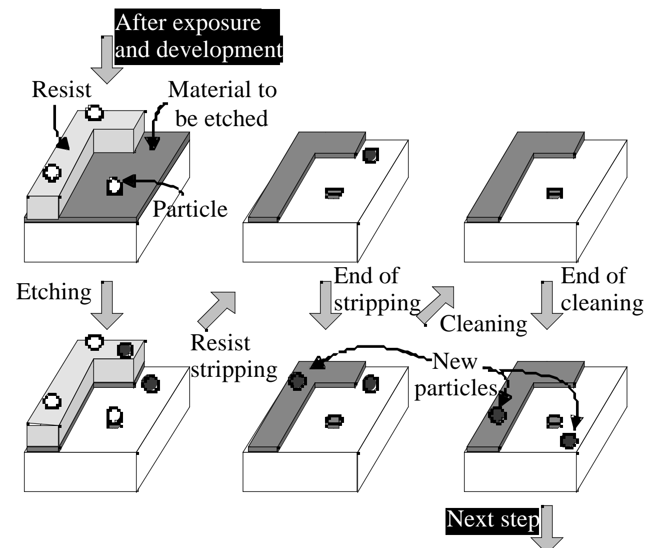
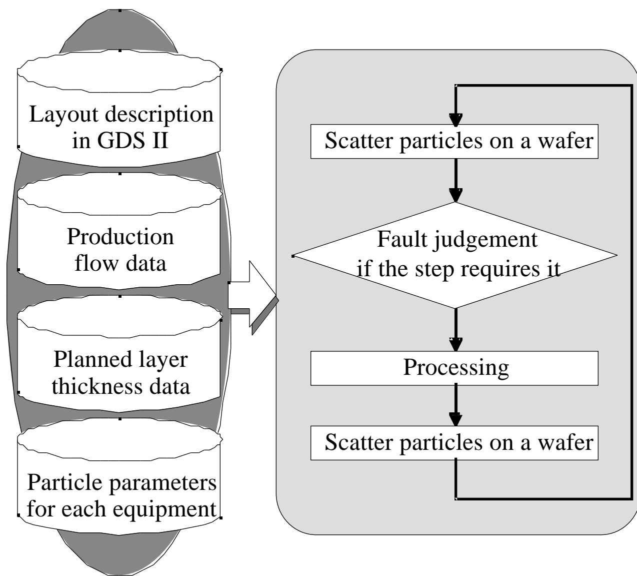


Figure 1: Effects of particles for etching, resist stripping, and cleaning steps in sequence.

fault, the capacity fault, the gate oxide fault, the wire short or open, the short between different layers and the contact fault. We decide that the faults such as shorts and broken circuits occur on a layer when particles deposited on the wafer occupy more than 30 % of the size of the line width, the space between two lines or the film thickness. We recognize the short between layers when two wires are

connected through a conductive particle.

Under these assumptions and the model, we implement a simple VLSI particle-induced yield predictor in C language on UNIX WS (Silicon Graphics Indy R4600(100MHz, SPEC int92:62.8, SPEC fp92:49.9). The yield predictor accepts as inputs (a) layout description of the VLSI under analysis in GDS II format, (b) production flow data, (c) planned layer thickness data, and (d) particle parameters for



Fi

each production equipment. The predictor works in the following manner. For each processing step or each production equipment, at first the number of particles is determined by generating random deviates with the Poisson distribution. Next the particle sizes are obtained from random deviates with the Gamma distribution. The deposited positions are sought on the wafer by generating uniform random numbers in the radial and azimuth directions. In the fault decision, from the deposited positions on the wafer, the positions in the chips are calculated and the spherical particles with specified sizes are put on it on the layout. Then whether or not the particles cause faults is examined if the step requires a fault judgment (this is set by a user). Then the processing is carried out. Actually, one-half of generated particles pour on the wafer at the start of the processing step and the other half at the end of the step as shown in Fig. 2. In this way, processing steps are repeated according to the production flow. Finally from the fault decision data, the yield is calculated.

APPLICATION

We applied the yield predictor to a 16-Mbit CMOS DRAM production process. Figure 3 shows a part of the wafer flow diagram that shows the numbered wafer processing steps and the production equipment used in each processing step. Tables 1 and 2 show the average number of deposited particles on a wafer for each equipment that are extracted from the reported data [5] and the assumed average particle sizes, respectively. There are 100 chips on a wafer.

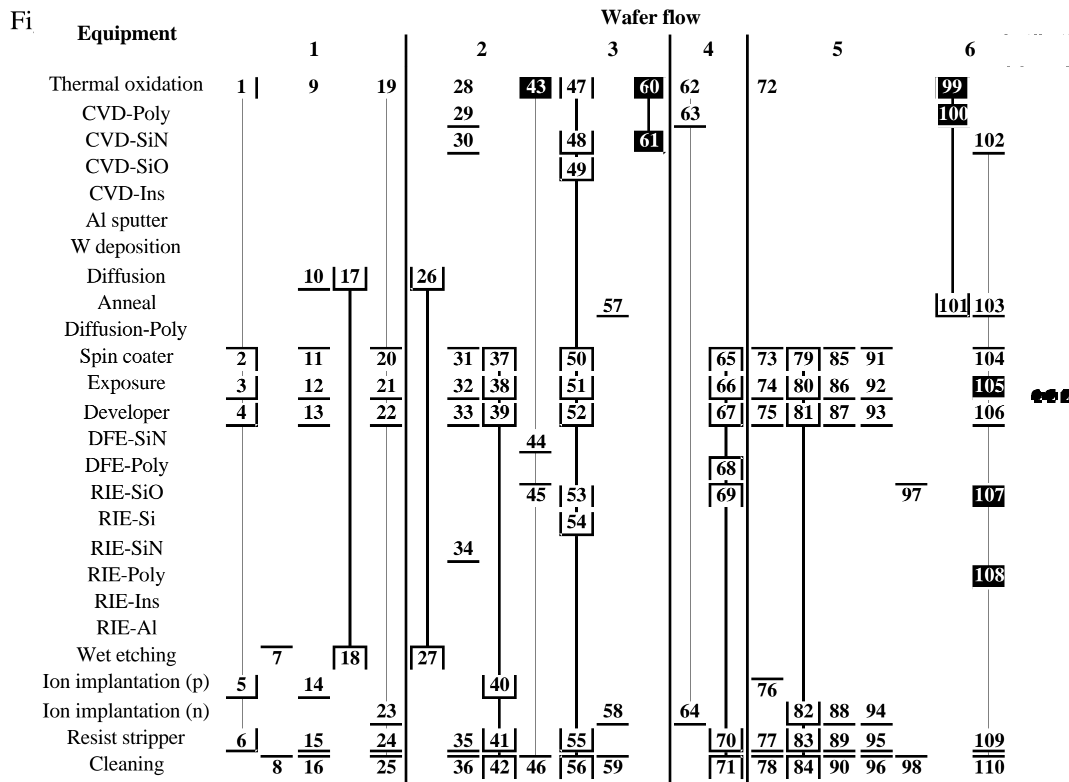


Figure 3: Part of wafer flow diagram. The number indicates the processing step.

The simulation was repeated 100 times to predict the yield. The time required for 100 simulations was about 10 seconds. Figure 4 shows the result in cases of DRAM with

	particles per wafer		particles per wafer
Thermal oxidation	2	DFE-Poly	50
CVD-Poly	10	RIE-SiO	50
CVD-SiN	10	RIE-Si	50
CVD-SiO	10	RIE-SiN	50
CVD-Ins	15	RIE-Poly	50
Al sputter	10	RIE-Ins	50
W deposition	15	RIE-Al	50
Diffusion	2	Wet etching	10
Anneal	2	Ion implantation (p)	20
Spin coater	1	Ion implantation (n)	20
Exposure	1	Resist stripper	10
Developer	1	Cleaning	10
DFE-SiN	50		

Table 2: Average size of deposited particles on a wafer for each equipment.

Equipment	Average size of deposited particles
Equipment with average number of particles 50	0.6 ƒÊm
Equipment with average number of particles 15 ?`20	0.4 ƒÊm
Equipment with average number of particles less than 10	0.3 ƒÊm

and without redundant circuitry. For comparison, the reported yield values [5] are also plotted on this figure. From these results, it is seen that the simulated yield is close to the reported one in case with no redundancy. A little large yield difference for the case with redundant circuitry is due to a larger number of redundant circuits included in the simulation.

By analyzing the yield, it was seen that the RIE-SiO process of the step number 97 was a bottleneck. Then by reducing the average number of particles generated in the RIE-SiO process equipment by half, we repeated the

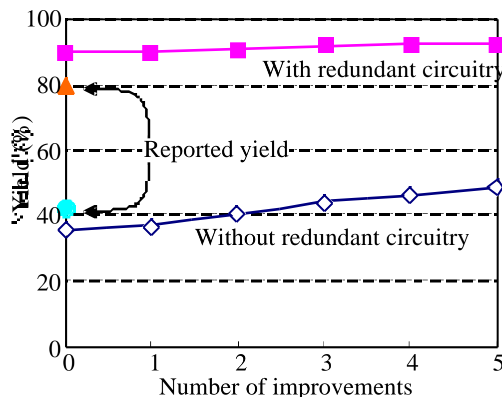


Figure 4: Yield changes due to repeated improvement procedures.

simulation. This reduction improves the processing steps 45, 53, 69, 97,••• . Yield increased by 2 %. These improvement procedures were repeated. Yield changes were plotted in Fig. 4. Also we carried out a failure analysis. Results are shown in Fig. 5. It is seen that the second polysilicon layer short fault is dominant.

Lastly, we performed sensitivity analysis as to the production equipment. The yield values are obtained by increasing or decreasing the average number of particles generated in some production equipment by a factor of 10. Results are shown in Fig. 6 and 7. It is seen that the RIE-SiO process equipment has a high sensitivity on yield.

REFERENCES

[1] T. Hattori, “Contamination control: problems and prospects,” Solid State Technol., 33, S-1 (1990).

[2] J. B. Khare and W. Maly, “From contamination to faults, faults and yield loss: simulation and application,” Kluwer Academic Publishers, Boston, 1996.

[3] H. Fujioka, K. Nakamae, and A. Higashi, “Effects of multi-product, small-sized production of LSIs packaged in various packages on the final test process efficiency and cost,” Proceedings of International Test

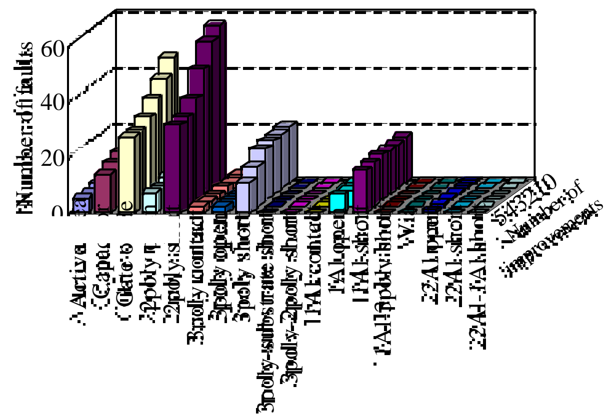


Figure 5: Fa

Conference, 793-799, 1996.

[4] Z. Stamenkovic and N. Stojadinovic, “New fault size distribution function for estimation of chip critical area in integrated circuit yield models,” ELECTRONICS LETTERS, 28, 528-530, 1992.

[5] F. Uesugi, N. Ito, and H. Doi, “In-situ Particle Monitoring in Plasma Processing,” NEC Technical Journal, 50, 62- 67, 1997.

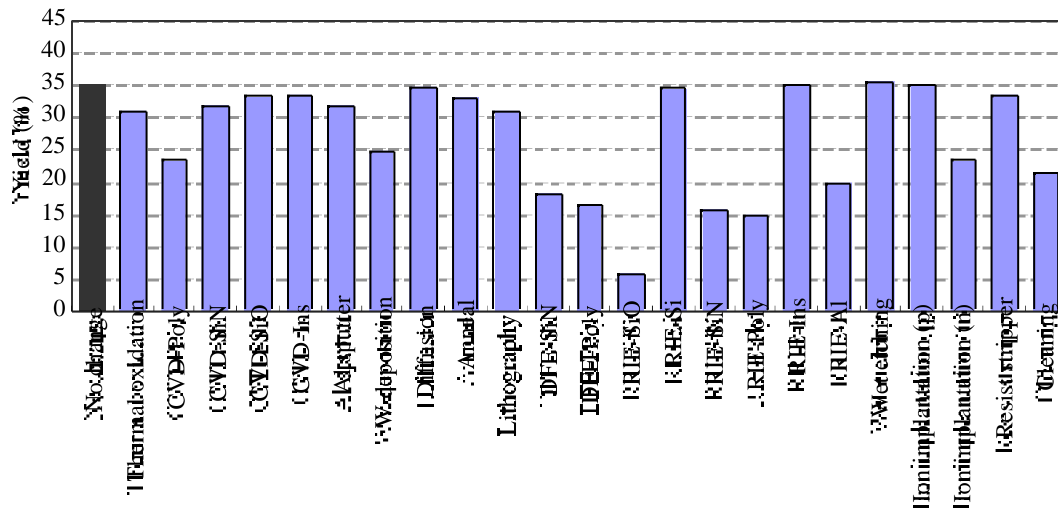


Figure 6: Sensitivity analysis by increasing the average number of particles by a factor of 10.

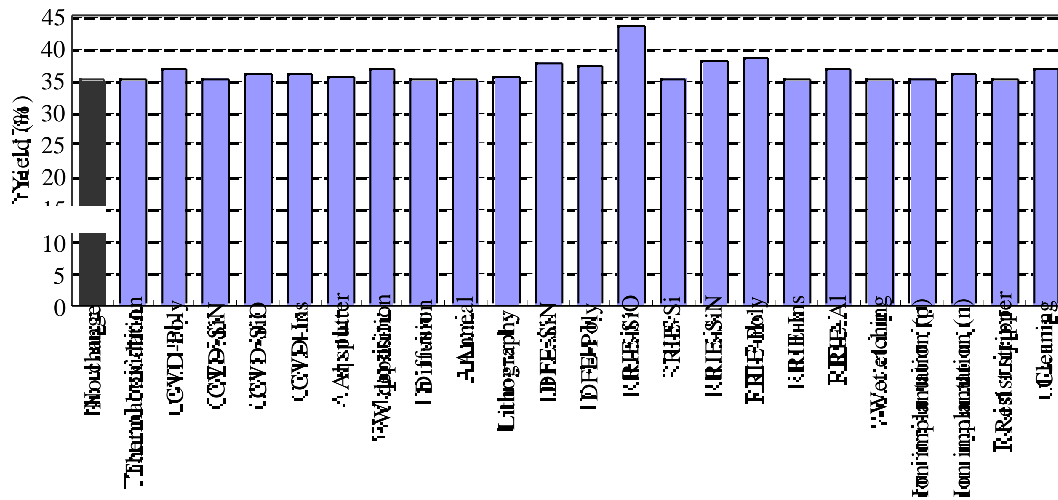


Figure 6: Sensitivity analysis by decreasing the average number of particles by a factor of 10.