Modeling On-Currents for n-MOSFETs: Ultimate Limits vs. the NTRS

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The continued evolution of Si technology hinges to a large extent on the ability to maintain high on-currents while achieving low off-currents. As we move from sub-micron to nanoscale technology, it is not at all clear that these often-contradictory requirements can simultaneously be met. In this talk, we establish ultimate limits for the on-current and compare them against the targets in the National Technology Roadmap for Semiconductors (NTRS). We present a simple theory to predict the on-current of a MOSFET in the limit of no scattering in the critical portion of the device. We show that current devices achieve about one-third of this ballistic limit on-current and that future devices will have to achieve about two-thirds of the ballistic limit in order to meet the NTRS on-current target.

To establish theoretical upper limits for the on-current, we use self-consistent Schrödinger-Poisson simulations to solve for the energy sub-bands, electron inversion layer density, and the Fermi energy. Near-equilibrium conditions prevail in a MOSFET when the drain voltage is small. When the drain voltage is large, the current becomes large, but the carriers injected into the channel retain a near-equilibrium distribution at the source end. The ballistic on-current is evaluated from

$$I_D(on) = qn_S\langle \upsilon(0)\rangle,$$

where n_S, the inversion density near the source end, is taken from a one-dimensional equilibrium solution to the MOS problem. Detailed simulations show that n_S is about 90% of it equilibrium value, even for the strongly off-equilibrium conditions that prevail in the ballistic limit. The velocity, $\langle \upsilon(0)\rangle$, is the average velocity of electrons at the source end of the channel, which in the ballistic limit is given by the thermal velocity appropriate to a two dimensional electron gas. By subtracting the current injected from the drain, a complete ballistic *I-V* curve can be generated. Figure 1 shows such a curve for a MOSFET corresponding to the L = 100 nm node of the NTRS. The corresponding transconductance is shown in Fig. 2. As shown in Fig. 3, a finite channel resistance is observed, even when the channel is ballistic. It is large enough to be important when analyzing experiments and is analogous to the $2e^2/h$ resistance observed in mesoscopic devices.

When the ballistic current is compared to present-day n-MOSFETs, we find that they are operating about one-third of their ballistic limit. Figure 4 shows the projected on-current vs. time using parameters from the NTRS. Even with the assumption that an equivalent oxide thickness of 1 nm can be achieved, future devices will have to operate much closer to the ballistic limits. Since current scaling rules maintain device performance at a constant fraction of the ballistic limit, new approaches will be needed.

In summary, we present a simple approach for estimating the upper limit performance of Si MOSFETs. The results should prove useful in assessing experimental results and for making technology projections.

Topic Area: process, device, and circuit simulation

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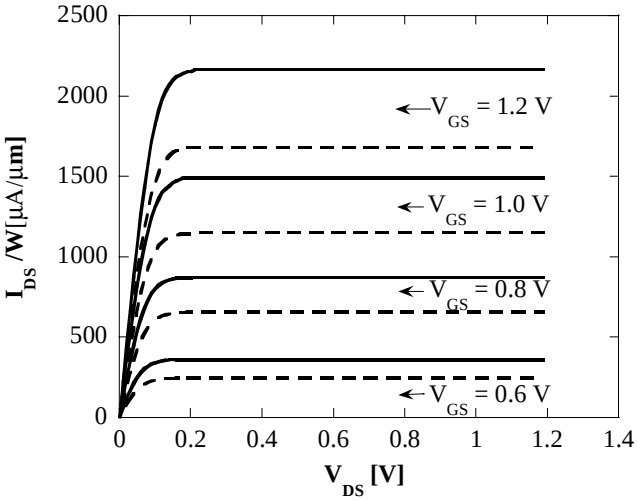

Figure 1. Ballistic common-source characteristics for $t_{ox} = 1.5$ (nm) and $N_A = 2.0\text{x}10^{18}$ (cm^{-3}). The solid lines correspond to a metal gate and dashed lines to a polysilicon gate. DIBL has not benn included

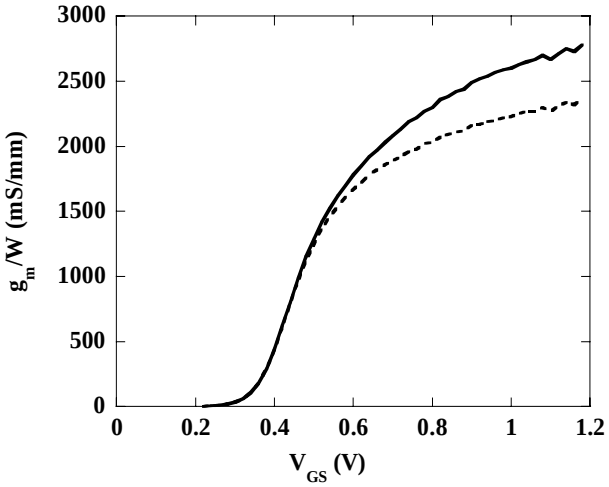

Figure 2. Ballistic transconductance for the metal gate (solid line) and poly-gate (dashed line) device.

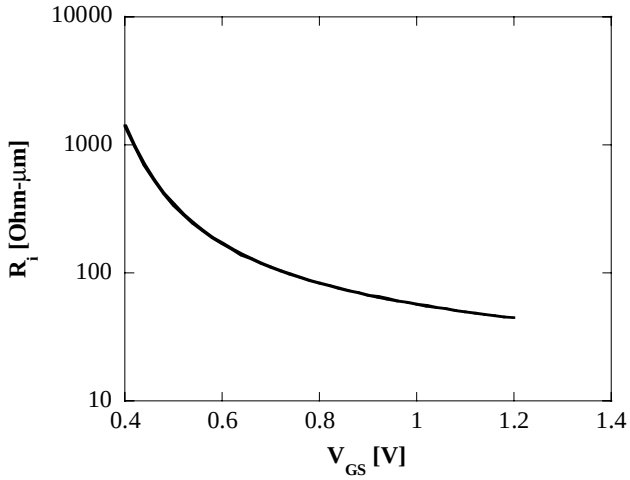

Figure 3. Ballistic channel resistance for the metal gate device, as a function of gate voltage. This resistance is due to the limited number of modes in the channel and therefore will always be present, regardless of the contact resistance.

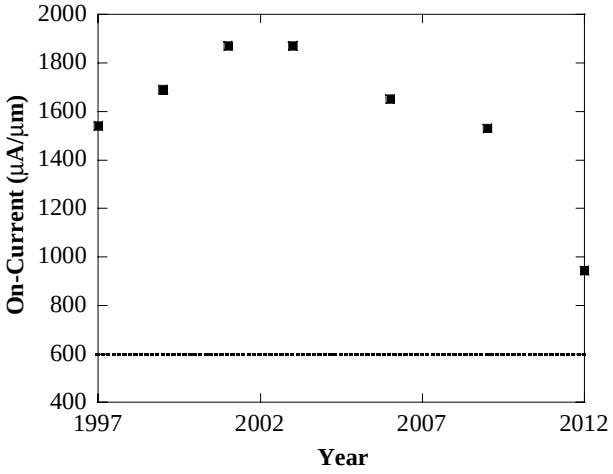

Figure 4. Predicted ballistic on-current vs. time using the NTRS parameters. Also shown (dashed line) is the on-current target of 600 μA/μm