Simulation of the Frequency Limits of SiGe HBTs

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ABSTRACT

The dynamic performance of SiGe HBTs in terms of the cut off frequency and the maximum frequency of oscillation is investigated by numerical device simulation. Simulations based on both the Drift Diffusion Model and the Hydrodynamic Model are carried out for a variety of different transistor structures to clarify the influence of the vertical transistor design on device performance. Based on the simulation results the validity of the Drift Diffusion Model is discussed and design criteria for RF SiGe HBTs are derived

Keywords: SiGe HBT, Hydrodynamic Model, Frequency Limits , Simulation.

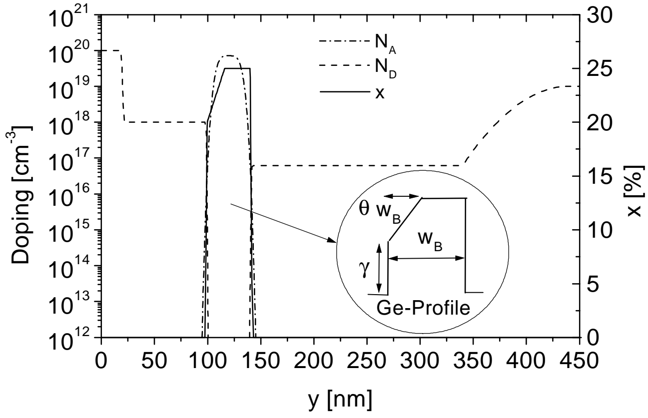
INTRODUCTION

Over the past ten years, SiGe HBTs have evolved from mere laboratory test devices to well accepted RF devices with commercial applications. SiGe HBTs with outstanding RF properties in terms of the cut off frequency (f_T) and the maximum frequency of oscillation (f_{max}) have been reported. Currently, the record values of f_T and f_{max} obtained with these devices are 130 GHz [1] and 160 GHz [2], respectively. Moreover, Hitachi researchers reported a SiGe HBT with both extremely high f_T (92 GHz) and f_{max} (108 GHz) [3].
The main difference in the device structure of SiGe HBTs compared to conventional Si BJTs is that in SiGe HBTs a thin strained SiGe base layer is embedded between the Si emitter and the Si collector, whereas Si BJTs consist only of Si layers. The properties of the SiGe base and of the heterojunction between the Si emitter and the SiGe base give rise to the unique RF properties of the SiGe HBT [4]. The advantage of SiGe devices compared to the commonly used III/V RF devices is that the matured and low cost Si technology can be used. Even though the SiGe HBT is a device well suited for RF applications per se, the design of such transistors with frequency limits in the range of 100 GHz or above requires a lot of work in the field of device simulation and structure optimization. The situation is complicated by the facts that some basic design rules of SiGe HBTs differ from those of Si BJTs and that critical device regions in SiGe HBTs are so small that effects of nonstationary carrier transport as velocity overshoot may affect device behavior considerably. Therefore, for device designers and engineers working on SiGe HBTs, reliable hydrodynamic device simulators with the ability to predict the transistor performance taking into account velocity overshoot are imperative. Despite the fact that such simulators are commercially available for mainstream Si devices, there are no SiGe device simulators with verified models for the various material properties of strained SiGe (e.g. mobilities, carrier energies, relaxation times).
The purpose of this work is to present the device simulator PROSA and to use this tool to investigate (a) the differences obtained in device simulations based on the Drift Diffusion Model (DDM) and on the Hydrodynamic Model (HDM) to verify the limits of the validity of the (DDM), (b) the optimum HBT design for maximum f_T and f_{max}, and (c) the frequency limits of SiGe HBTs in terms of f_T and f_{max}.

DEVICE STRUCTURES AND SIMULATION PROCEDURE

PROSA is a numerical 1d and 2d device simulator that permits calculations based on both the DDM and the HDM [5]. The models for the carrier transport properties have been developed in collaboration with the University of Bremen, where the transport parameters have been calculated by Monte Carlo simulations and verified by measurements [6]. The reliability of the PROSA models by far exceeds that of SiGe models currently incorporated into commercial simulators such as ATLAS. Excellent agreement between PROSA results and the results of Monte Carlo device simulations [7] as well as DC and RF measurements of experimental SiGe HBTs [5] has been obtained.
In the technical literature one can find two basic design philosophies for SiGe HBTs [8]. The first one, introduced by an IBM group [4], is characterized by a doping profile typically used in conventional BJTs (high doped emitter, low doped base) and a relatively low Ge content x in the base. The main features of the second concept, used e.g. by Daimler Benz researchers, are doping inversion, i.e. high base and low emitter doping, and a high Ge content in the base (up to 30%) [2].
The investigations of this work focus on the second concept. The f_T and f_{max} values of about 500 different SiGe HBTs with various vertical designs (details are given in [5] and [9]) and an emitter length of 0.8 µm have been simulated. Width and doping profile of the base and of the low doped collector (in the following designated as collector) as well as the Ge profile in the base (in terms of the Ge content at

the emitter base junction (γ) and the base fraction containg a Ge grading (θ)) have been varied. Figure 1 shows a typical vertical doping and Ge profile of the SiGe HBTs simulated. Figure 1: Doping and Ge Profile of a SiGe HBT with w_b=40nm, w_c=200nm, Θ=40% and γ=20%.



To our knowledge, this work presents the first systematic study of the dependence of f_T and f_{max} on vertical transistor design. Because fully 2d simulations of the great number of transistor structures investigated would require unacceptable amounts of computation time, we used a simulation hierarchy described below that minimizes the computation effort.

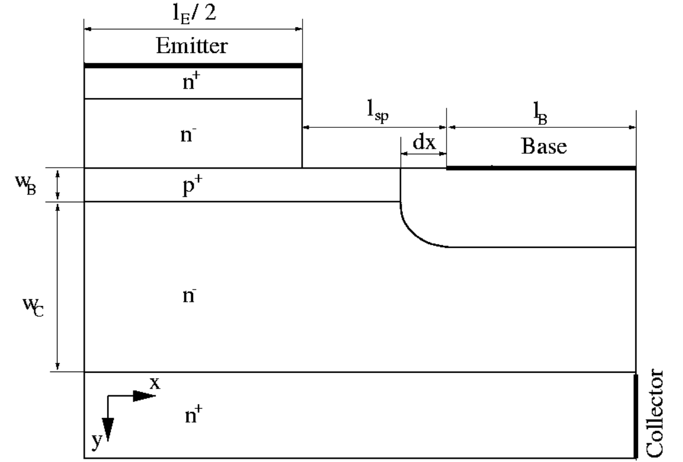
The first step is the calculation of the cut off frequency of all transistor structures as a function of collector current density J_C using the Charge Partitioning Method (CPM) described by van den Biesen [10]. This method allows for the calculation of f_T itself but furthermore of the different components of the emitter collector charging time τ_{ec}. Because f_T is mainly dependent on the vertical transistor structure while the influence of the lateral dimensions is rather marginal in the device structures of our study, only 1d simulations have been carried out at this stage. Next, we calculated the maximum frequency of oscillation of all transistors. In contrast to f_T, the lateral device dimensions strongly influence f_{max}. The maximum frequency of oscillation has been calculated using the approximate expression

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_B C_{CB}}}$$

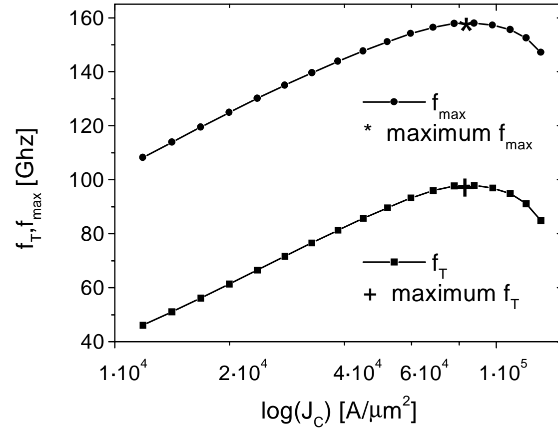
where f_T is the cut off frequency obtained by the 1d simulations mentioned above, R_B is the base resistance and C_{CB} is the collector base capacitance. Both R_B and C_{CB} have intrinsic and extrinsic components, which have been computed taking into account the lateral device dimensions as shown in Fig. 2, the carrier and mobility profiles under the emitter (results of the 1d simulations) and the doping profiles in the extrinsic transistor regions. The main result of the first two steps of our investigation are f_T and f_{max} as functions of J_C. As an example Fig. 3 shows the $f_T(J_C)$ and $f_{max}(J_C)$ curves of a SiGe HBT with w_b = 10 nm and w_c = 200 nm simulated using the HDM. From results like these the maximum values of f_T and f_{max} for each transistor are obtained.

Figure 2: Model structure

Figure 3: f_T and f_{max} vs. J_C (V_{CB}=1.0V) for a transistor with w_b=10nm, w_c=200nm, Θ=0% and γ=25%, calculated by



HDM

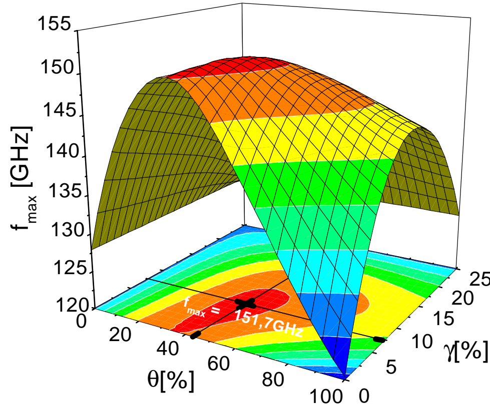


To get the results more clearly arranged, the 500 different transistor structures have been grouped. One group comprises HBTs with a certain base width w_b (e.g. w_b = 40 nm) and a certain collector width w_c (e.g. w_c = 400 nm), but with different Ge profiles in the base, i.e. with different values for γ and θ. For each of the 16 different groups of transistors f_T and f_{max} have been plotted as a function of γ and θ as shown in Fig. 4. From these plots one gets the optimum Ge profile and the maximum attainable f_T and f_{max} for each group. For the eaxmple of Fig. 4, the optimum Ge profile is characterized by values of γ of 7.5% and θ around 50 % and a maximum attainanble f_{max} of 152 GHz. Fig. 5 shows the maximum attainable f_T as a function of w_b with

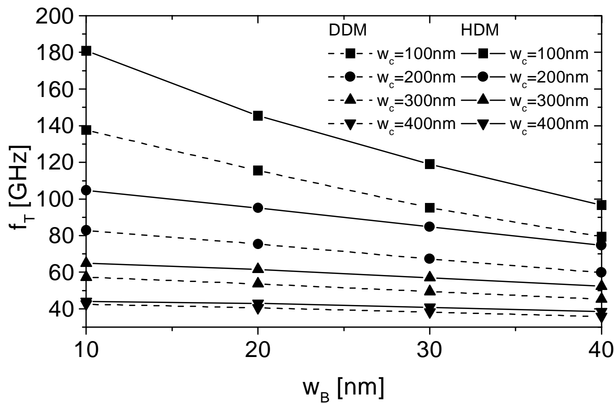
w_c as parameter. As to be expected, transistors with narrow base and collector layers (small w_b and w_c) have the highest cut off frequencies.

Figure 4: f_{max} vs. Ge-Profile (Θ and γ) for the group of transistors with w_b=40nm and w_c=400nm, calculated by HDM.

Figure 5: Maximum attainable f_T vs w_b, calculated by DDM



and HDM



More interesting are two other details of Fig. 5. First, for transistors with wide collectors (w_c = 300 nm, w_c = 400 nm) f_T is only a weak function of w_b. This means that in transistors with wide collectors the cut off frequency is dominated by the effect of the collector or in other words by the base collector charging time t_{bc} (see also insert in Fig. 6, $f_T = (2\pi\tau_{ec})^{-1}$). With decreasing collector width the influence of the base transist time τ_b is getting more important and in transistors with extremely narrow collectors τ_b becomes the dominating part of τ_{ec}. Secondly, Fig. 5 reveals that for transistors with wide base and collector layers the results of DDM and HDM simulations differ only slightly. In these transistors velocity overshoot occurs but does not play an important role for device behavior. The use of the DDM in that case is sufficient. On the other hand, the differences between DDM and HDM results in the simulation of HBTs with narrow base and collectors (e.g. w_b = 10 nm, w_c = 100 nm) are remarkable. Here strong velocity overshoot occurs in a larger part of the device on both sides of the base collector junction (see Fig. 6, note that the velocity axis is exponentionally divided). To describe the behavior of SiGe HBTs with such narrow base and collector layers the HDM should be used. Using the HDM, maximum attainable f_T values of 181 GHz have been calculated for a SiGe HBT with w_b = 10 nm and w_c = 100 nm.

Figure 6: Calculated electron velocity (v_n) vs depth (y) and charging times (τ) for transistors with w_b=40nm, w_c=100nm and w_c=400nm, respectively (DDM and HDM).

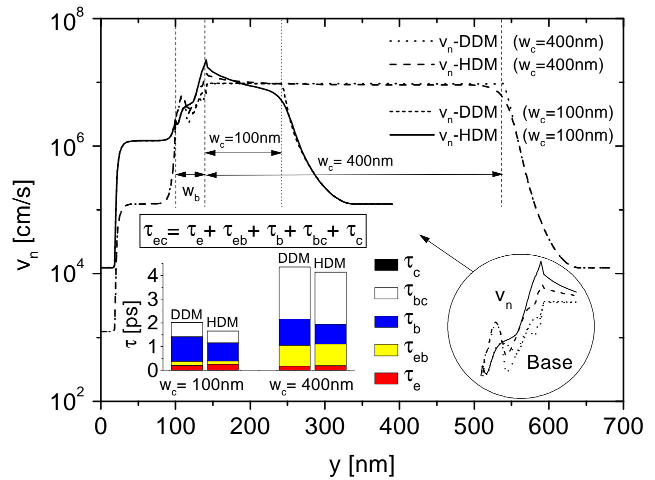
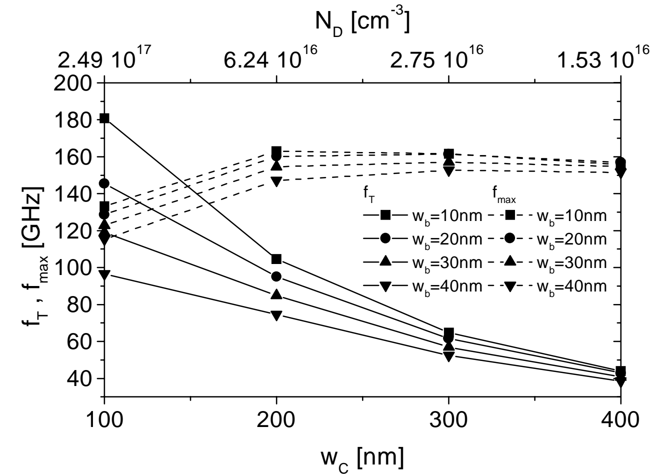


Figure 7: Maximum attainable f_{max} and f_T vs w_c and the corresponding collector doping N_D, calculated by HDM.



In Fig. 7 the calculated maximum attainable f_T and f_{max} as a function of collector with w_c (or in other words collector doping N_D, see upper x axis) is shown. As can be seen from the figure, there is a trade off between f_T and f_{max}. It is not

possible to optimize one and the same SiGe HBT for **both** maximum f_T **and** f_{max} but one has to make a compromise. This trend has been verified experimentally by Schüppen et al. [2]. Depending one the requirements dictated by the device application it is possible to optimize the HBT concerning f_T **or** f_{max}, or to choose a device structure with moderately high and nearly equal values for f_T and f_{max} [3]. The latter choice is often made to make the transistor suitable for a broad range of application.

The obtained optimum γ values range from 12% to 25% and depend on w_b and w_c, whereas the optimum values for θ are about 50 % in most of the transistors. For transistors with narrow base and collector layers the optimum Ge profile approaches a box profile without Ge grading.

In the study presented here, the lateral dimensions of the SiGe HBTs were hold constant. Further work has to be done to optimize these lateral dimensions as well as the design of the base contact implant. For such optimizations rigorous 2d simulations are necessary. In general, even higher f_T and f_{max} values as mentioned above can be expected for transistors with smaller emitter lengths. However, in extremely laterally scaled HBTs a parasitic BJT caused by boron outdiffusion from the base contact implant can occur. Currently work is in progress to investigate this effect by rigorous 2d simulations.

CONCLUSION

A device simulator well suited for the simulation and optimization of SiGe HBTs has been presented. Using the results of the simulation of about 500 different transistor structures, design rules for SiGe HBTs have been worked out. It has been shown that for the simulation of SiGe HBTs with narrow base and collector regions the HDM should be used while in the case of transistors with wider bases and collectors the DDM is sufficient.

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