Impact of Heat Source Localization on Conduction Cooling of Silicon-on-Insulator Devices

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ABSTRACT

The temperature rise in compact silicon devices is strongly underestimated at present by simulations using conventional heat diffusion theory, which is based on the Fourier heat conduction law. This problem is particularly important for devices in which the region of strong electron-phonon coupling is narrower than the phonon mean free path, Λ. The phonon mean free path in silicon near room temperature is already comparable to the minimum feature size of current generation transistors. This work numerically integrates the phonon Boltzmann transport equation (BTE) in order to determine the impact of this heat source localization. The difference in temperature rise predictions based on the BTE and conventional diffusion theory increases by a factor of twenty as the heat source size varies from 10 Λ to 0.1 Λ.

Keywords: SOI devices, Boltzmann Transport Equation, heat transport, localized heating.

INTRODUCTION

The scaling of integrated circuits is yielding transistors with channels of length below 200 nm. This is comparable to an average value of Λ appropriate for the simulation of second breakdown phenomena during electrostatic discharge (ESD) transients, which is estimated to be 180 nm [1]. Large electric fields near the drain side of compact transistors create hotspots with characteristic dimensions of approximately 100 nm [2], which decrease in width with device scaling. Silicon-on-insulator (SOI) devices are particularly susceptible to self heating and thermal failure because thermal conduction cooling is confined within a silicon layer of thickness as low as 50 nm. Because device and hotspot dimensions are comparable with the phonon mean free path, thermal simulations must consider the impact of phonon-interface scattering and heat source localization on the temperature distribution. These non-local thermal conduction phenomena cannot be directly calculated using the heat-conduction equation based on Fourier's law.

Phonon transport in semiconductor devices is modeled at present using diffusion theory based on Fourier's law without considering non-local phenomena [2,3]. However, past work has illustrated the impact of non-local phonon conduction in relatively simple geometries, including thin films, superlattices, and polycrystalline materials [4,5,6]. Sondheimer [7] analytically solved the BTE for electron transport in thin films, yielding a reduced effective thermal conductivity accounting for boundary scattering. This result can also be used to calculate a reduced effective phonon thermal conductivity accounting for interface scattering. However, this approach does not account for heat source localization, resulting in underestimation of the temperature rise in compact transistors. When Λ approaches the hot spot size, a strong nonequilibrium situation exists within the phonon system because of the reduced frequency of carrier collisions [9]. This causes the temperature rise to increase compared to that predicted by conventional diffusion theory. There have been no simulations that resolve non-local phonon transport in practical device geometries.

The present work integrates the BTE to simulate heat transport in compact semiconductor devices. The goal is to determine the impact of the hot spot size on the temperature distribution within a device. A goal for future work is to improve diffusion modeling in device simulators, such that it can account for nonlocal phonon transport for arbitrary heat source distributions.

SOLUTION METHOD

The transient non-dimensional phonon BTE can be written in the relaxation time approximation as

$$\frac{\partial f}{\partial t^*} = -\mu \frac{\partial f}{\partial x^*} - \eta \frac{\partial f}{\partial y^*} + \frac{f_{eq} - f}{\tau^*_{Phonon}} + q$$

(1)

where $f(x^*, y^*, \mu, \eta, t^*)$ is the number of phonons in a given state described by the dimensionless coordinates $x^* = x/L_x$ and $y^* = y/L_x$ and the directional cosines μ and η. The dimensionless time is $t^* = t\,v/L$, where v is the phonon velocity. The third term on the right of Eq. (1) accounts for phonon scattering in the relaxation time approximation using the Planck distribution function, $f_{eq}(x^*, y^*, t^*)$, and the dimensionless mean free path, Λ^*. Energy absorption from hot electrons is considered using the source term q.

The distribution function, f, depends on the two dimensional x and y grid location as well as the direction of phonon travel within the sphere of solid angles. For calculations of the heat flux and energy density at a given location, the Discrete Ordinates Method originally developed for neutron and radiative transport is used for integration over all solid angles. The solid sphere is divided into discrete directions of

phonon transport distinguished by sets of μ and η values with weights, w_i, corresponding to solid angle fractions on the unit sphere [9,10,11]. The weights satisfy

$$\sum_i w_i = 4\pi$$

(2)

This work uses the level symmetric hybrid (LSH) scheme [10] for angular discretization. Level symmetric techniques use the same set of directional cosine values in each coordinate direction ($\mu_1=\eta_1$, $\mu_2=\eta_2$, …). In addition, the directions of phonon transport are chosen such that any particular direction has corresponding directions with 90° rotations about any axis ($\mu_n=\eta_n$, $\mu_n=-\eta_n$, $-\mu_n=\eta_n$, $-\mu_n=-\eta_n$). This simplifies the implementation of boundary conditions and removes directional biasing. The LSH method calculates directions and weights based on constraint equations such that moment equations of the phonon intensity are satisfied [10].

The simulation domain for a simplified SOI device is depicted in Figure 1. The hot spot region located in the center of the domain represents the characteristic peak in the heat generation rate associated with electron-phonon energy transfer, which is typically on the drain side of the device. The top and bottom surfaces are modeled using diffuse boundary conditions which simulate phonon scattering at the interface between the Si layer and the SiO₂. The diffuse reflection boundary condition is

$$f_{\eta+} = \frac{1}{\pi} \sum_{\eta-} f_{\eta-} w_{\eta-}$$

(3)

$$f_{\eta-} = \frac{1}{\pi} \sum_{\eta+} f_{\eta+} w_{\eta+}$$

(4)

for the bottom and top surfaces, respectively. The side boundaries are assumed to have constant and nonvarying temperatures and are placed far away from the heat source compared to the mean free path. The side walls serve as sinks for the heat supplied to the middle of the computational domain. The large separation ensures that the only non-local effect resolved by the simulation will be the heat-source localization.

In order to obtain the temperature distribution, Eq. (1) is integrated forward in time in each of the discrete directions. The MacCormack time integration method, which is frequently used for solving hyperbolic equations [12], is used for explicit time advancement in order to capture the sharp features associated with the
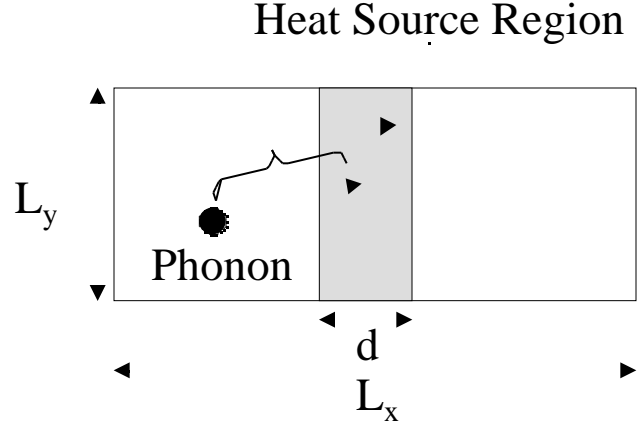

Figure 1: Simulation domain, which approximates the channel region of a silicon-on-insulator transistor.

source term and to resolve the wavelike nature of solutions to the BTE. At each time step, f^{n+1} are calculated from f^n and $f_{eq}{}^n$. Then, $f_{eq}{}^{n+1}$ is calculated before the solution can proceed. The equilibrium distribution function f_{eq} is assumed to be the average value of f over all solid angles that would be obtained if the phonon system was allowed to relax to a uniform value. The equilibrium distribution function is calculated as shown in Eq. (5).

$$f_{eq} = \frac{1}{4\pi} \int_{=4\pi} f\,d\Omega \approx \frac{1}{4\pi} \sum_i f_i w_i$$

(5)

The distribution f_{eq} can then be used to extract the temperature distribution from the temperature dependent distribution function.

RESULTS AND DISCUSSION

The steady state temperature difference between the BTE and standard diffusion theory is shown in Figure 2. This plot isolates the impact of localization from scattering on the top and bottom surfaces of the SOI layer by solving the one-dimensional version of the transport equation. While a one-dimensional solution

to the BTE is of limited relevance for practical device structures, it serves to illustrate the impact of heat source localization on the temperature rise. Ratios of heat source size to the mean free path, d/Λ, range from 0.1 to 5. The temperature at the center of the heated region increases significantly as the heat source size becomes smaller than the mean free path. In the heat source region, phonons are continuously produced by the simulated electron-phonon collisions. For large values of Λ compared to d, the reduced number of scattering events in the heat source region results in a
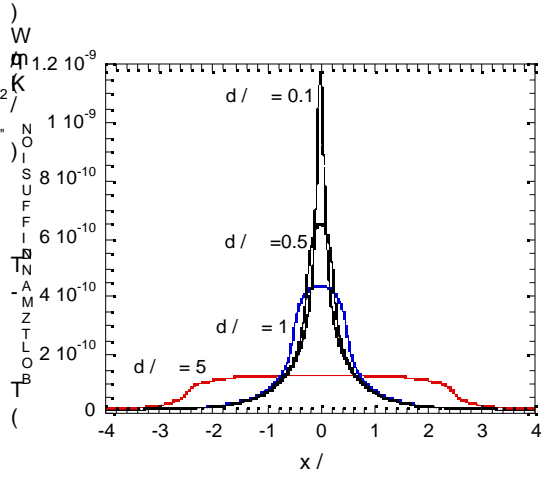
Figure 2: Temperature distribution in the localized heat source region.

Figure 3: Impact of heat source localization on discrepancy between BTE and diffusion theory.

substantial increase in the temperature rise. As d becomes much larger than Λ, the likelihood that phonons will scatter before leaving the heat source region increases dramatically. This establishes near-equilibrium conditions for the phonon system within the heat source region and renders diffusion theory valid. The increased temperature rise caused by heat source localization is confined to a distance approximately two mean free paths from the edge of the heat source. This can be understood with the help of the survival function from kinetic theory,

$$N = N_o \exp\left(-\frac{x}{\Lambda}\right)$$

(6)

which states that only a small fraction, N/N_o, of phonons generated in the heated region can traverse a distance much larger than the mean free path without having a collision.

Figure 3 plots the peak normalized temperature difference from Figure 2 as a function of d/Λ. The peak temperature rise difference increases by a factor of almost twenty as the heat source varies between 0.1

and 10 . The dimension of the heat source in existing compact transistors is already comparable with the mean free path [1,2], and this temperature augmentation phenomenon will become increasingly important for evaluation of temperature dependent electrical properties and for the thermal runaway characteristics of ESD failures [13].

Solutions of the two-dimensional transient BTE can resolve temperature fields in practical device structures. Eq. (1) can be solved for the thermal response to brief transient current pulses as well as steady state heating. The two-dimensional BTE can
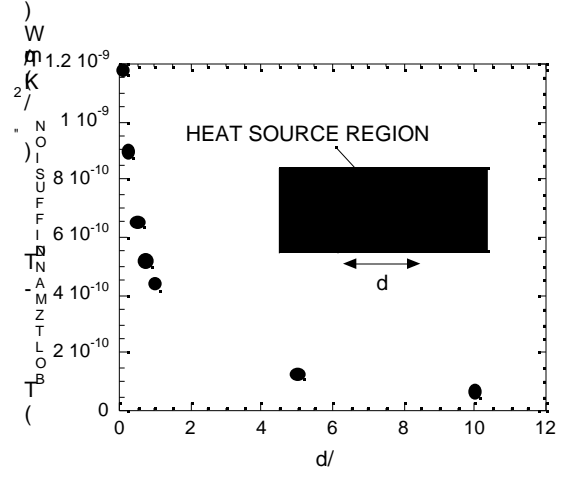
resolve the impact of boundary scattering and heat source localization, and results can be compared to Sondheimer's solution of the BTE which accounts for boundary scattering. Figure 4 plots the temperature distribution in a SOI layer in which both the heat source width, d, and the SOI layer thickness, L_y, are equal to . The characteristic increase in the temperature rise compared to diffusion theory can be seen in the heat source region. The two-dimensional simulations resolve the simultaneous impact of localization and the scattering of phonon heat carriers on the top and bottom surfaces of the SOI device layer. This additional scattering augments the impedance for conduction along the SOI film.

CONCLUSIONS

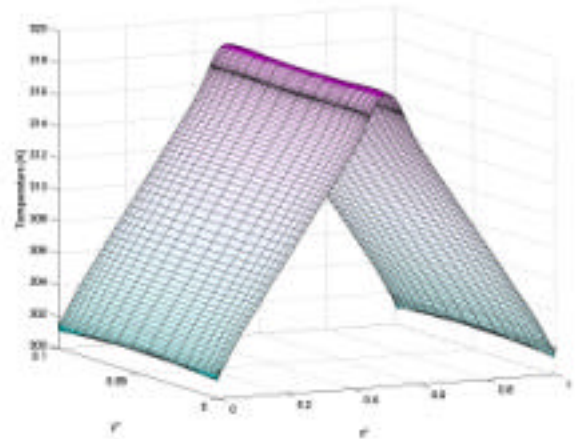The solution of the phonon Boltzmann transport

Figure 4: Temperature distribution in a silicon-on-insulator device layer with $d=L_y=\Lambda$.

equation illustrates the impact of localized heat sources on the peak temperature rise in semiconductor devices. This work contributes to a better fundamental understanding of heat transport in micro- and nanoscale regimes where heat source localization is important. The solution method developed here for the two-dimensional BTE will be used for studies for the coupled impact of localization and phonon boundary scattering in compact transistors.

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