Reduced Electro-Thermal Models for Integrated Circuits

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ABSTRACT

Power dissipation density in today's integrated circuits makes thermal problems very important. Unfortunately, the electro-thermal co-simulations, which are often indispensable in solving thermal issues, are constrained by the lack of the IC's electro-thermal models. This paper presents a complete development process of the Motorola MC33186 thermal model used for such simulations. The requirements for electro-thermal models, with the emphasis placed on the high computation speed, are discussed. Reduction of a 3D model based on the device's physical structure is presented in details. Stress is laid on including in the final model elements typical for the devices' application and crucial for the heat flow – in this case, the PCB. Another important aspect included in the paper is parameterization of the PCB properties

Keywords: Electro-thermal modeling, Model reduction

INTRODUCTION

Pure electrical simulations are not always sufficient, because electrical parameters depend on temperature and in turn, the temperature depends on power dissipated in the electrical devices. Besides, temperature issues can be crucial to the device's reliability, especially in power devices. Too high temperature may destroy the device or cause its malfunction. So-called "hot spots" resulting from the heat accumulated in one place are especially dangerous. Therefore, it is often necessary to extend the electrical model with a thermal part, which computes the dependence between power dissipations and temperatures. Separate electrical and thermal simulations are insufficient due to that correlation and an electro-thermal co-simulation must be performed instead. That is why the thermal model must be coupled with the electrical one.

Multi-domain Models

Nowadays there are a lot of libraries containing models that allow electrical simulations of various electrical devices. With the help of these models it is possible to test a device's electrical behavior before it is installed in an application system. The electro-thermal models we want to create require a multi-domain simulator like SABER or ELDO. When we have a coupled electro-thermal model, we can test the device taking into account temperature growth resulting from both internal and external heat generations. We are also able to check if the temperatures do not exceed its safe operating limits. Unfortunately, there are few such models in the libraries, so creating them seems to be a great challenge. Such models must include not only the model of the IC itself, but also other elements crucial for the heat flow.

Requirements for Thermal Models

Before model creation we specified basic requirements it had to meet. It must at least:

- Allow passing of PCB and environment characteristics as the model parameters to enable using model in various conditions. This includes parameterizing the PCB's dimensions, material properties and cooling type. Without such parameterization the thermal model would not be useful. This is obvious since a particular integrated circuit will not be used with only one kind of PCB.
- The model must provide good accuracy for all combinations of parameters in order to return exact temperature values. That accuracy must be better than in a simple approach based on thermal conductivity. This is especially important when the device operates close to its thermal durability limit and safety margins are very narrow. This is why we must take into account 3D-heat flow and 3D-temperature distribution. All materials from a thermal point of view can conduct heat - there are neither ideal thermal insulators nor ideal thermal conductors. This make heat diffusion radial and an approach based on thermal impedance may cause huge errors.
- The numerical simulation of a 3D model produces small errors, but due to complexity the computation takes long time. The thermal model coupled with the electrical one should be as simple as possible so as not

to increase substantially the total computation time. Models acceptable for pure thermal simulation would be too complex for electro-thermal simulation. Therefore model reduction is essential.

MODELED DEVICE

The aim of the project was to design an electro-thermal behavioral model of the Motorola MC33186 H-Bridge Driver. This is a VLSI smart-power integrated circuit used mainly to control DC motors. One of the most important fields of application for such a device is an ABS car system. The chip is composed of a power part containing four high-power TMOS transistors, sensors measuring voltages, currents and temperatures and a CMOS logic part, which controls the gates of the power transistors and, to prevent damage, shuts down the transistors in case of over-current, over-temperature or under-voltage. The model had to be implemented in SABER as a template and it had to accept PCB parameters to enable use of different boards.

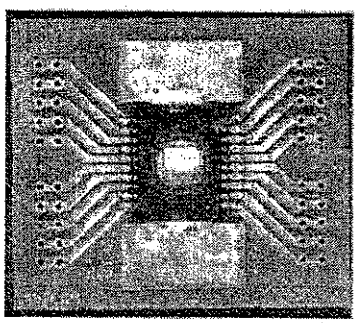

Figure 1. MC33186 on test PCB

In order to test and model the device in conditions close to real-life the MC33186 was placed on a small test board. Both upper and lower surfaces of the board were covered with thin copper foil acting as heat sinks. The part of the PCB just under the IC was equipped with so-called "thermal vias" – a set of small (about 1mm in diameter) holes filled with copper and solder. Thermal vias acted as a connection between the heat sinks and increased the effectiveness of the lower heat sink. The whole device had to be placed in open, still air, with no additional cooling equipment. Some of the PCB characteristics, especially those most crucial for the accuracy, were parameterized within ranges given in the project specification.

MODEL CREATION

The following basic steps were made to create the model:

- Full 3D thermal model creation on the basis of a physical structure.
- Running measurements in order to verify the created model by comparison and adjust heat-exchange coefficients so that the model became equivalent to the real device
- Model reduction performed so that the computation time was acceptable
- Model parameterization performed to enable use of different PCBs
- Implementation in SABER MAST language

Linear Approximation

The problem of heat flow is generally nonlinear. However, computers solve nonlinear problems much slower than the linear ones. We found that for the given operating range of temperatures, the linear model yields results with less than 10% error in the worst case and about 3% for the typical operating temperature. Because we focused on computation speed, this level of inaccuracy is acceptable. That is why we used a linear model for all computations. Employing a linear model made the computations faster, still maintaining acceptable errors. Since superposition is possible in linear systems, the influences of particular transistors on the temperature distribution were additive.

3D MODEL CREATION

The first step was to create a full 3D thermal model of the device. Since there are neither ideal thermal insulators nor ideal conductors, heat flows are three-dimensional and 3D-temperature distribution must be computed. If we compare thermal and electrical conductivity range we find that thermal conductivity for all materials corresponds to conductivity of electrical semiconductors. This is the reason why we cannot simplify the problem by assuming one-directional heat flow and neglecting other directions.

Full 3D models are built on the basis of a detailed physical structure. For such simulation many numerical methods can be used, for example: Finite Element Method, Finite Volume Method, Boundary Element Method or Finite Difference Method. In order to create the 3D model we used TULSOFT - the 3D thermal simulator created at our Department. It uses the Finite Difference Method to transform the full physical structure to an equivalent electrical circuit composed of resistors, capacitors and independent current sources.

The device physical structure was divided into several blocks. Figure 2 presents schematically the created 3D thermal model. It consists of following blocks:

- Silicon that represents the IC's substrate with four heat sources representing TMOS transistors placed on its top surface

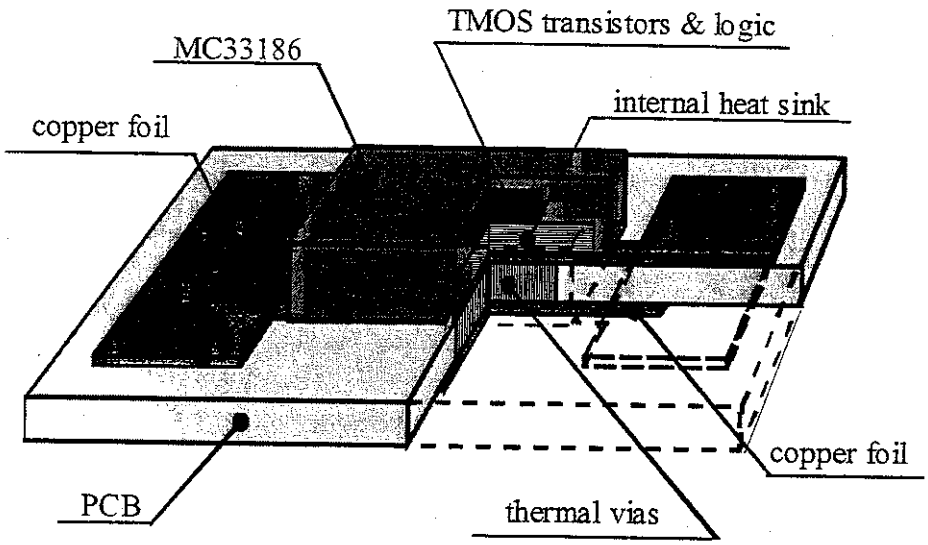

Figure 2. Full 3D model (not to scale)

- IC's internal copper heat sink
- Thin solder layer between the silicon and the heat sink
- Mold compound that represents the IC's package.

The PCB thermal model is composed of the following blocks:

- Central part of the laminate with modified thermal conductivity that represents area with thermal vias
- Laminate representing the remainder of the board
- Top copper foil
- Optional bottom copper foil

For all exposed parts heat drains that represent the heat emission and convection to the ambient were defined.

Model Verification and Tuning

The initial 3D model was based on the dimensions and thermal properties of the modeled structure parts, obtained from the specification. However, in the beginning the model did not yield the same results as obtained from thermal measurements. It was necessary to tune it in order to get accurate results. This mainly included modification of the model structure in order to make it more precise in the section where temperature gradient was high. It was also necessary to adjust the structure-to-air heat exchange coefficient.

MODEL REDUCTION

The 3D model created with TULSOFT was very complicated, it contained more than 15,000 nodes. It is impossible to use such a complicated model as a part of an electro-thermal model for two main reasons:

- first, the computation time would be unacceptable, especially during transient-state analysis
- second, it would be difficult to implement such a big RC network

For these reasons the model had to be reduced before it could be connected with the electrical part.

First Approach to Model Reduction

Here, an initial approach to model reduction will be discussed. This approach, although later given up, is an interesting one, because it lets the designer create the reduced model with minimum effort, almost automatically. The idea was to create a pure mathematical, linear model on the basis of the impulse response of the full 3D model.

The following basic steps were made to create the mathematical model:

- TULSOFT simulations were performed separately for each single active transistor (actually for a half of them, as the model is symmetric). Temperature responses of all transistors for a power step from zero to P_0 in the selected transistor were examined.
- Each examined temperature response was approximated by the following sum of exponential functions:

$$C_1 \cdot (1 - \exp(-a_1 \cdot t)) + C_2 \cdot (1 - \exp(-a_2 \cdot t)) + \ldots + C_n \cdot (1 - \exp(-a_n \cdot t))$$

Maximum three exponential functions were sufficient. Approximation consisted of an initial geometrical exponent decomposition plus their further optimization

using DSC + Powell algorithm combination.

- A system of ordinary, linear, first-order differential equations with constant coefficients was created for each approximated temperature response:

$$\frac{d}{dt}(T_1(t)) + a_1 \cdot T_1(t) = a_1 \cdot C_1/P_0 \cdot p(t)$$

$$\frac{d}{dt}(T_2(t)) + a_2 \cdot T_2(t) = a_2 \cdot C_2/P_0 \cdot p(t)$$

$$\vdots$$

$$\frac{d}{dt}(T_n(t)) + a_n \cdot T_n(t) = a_n \cdot C_n/P_0 \cdot p(t)$$

- Partial temperature responses T_1 .. T_n were added to give the total temperature response for single active transistor:

$$T(t) = T_1(t) + T_2(t) + \ldots + T_n(t)$$

This function is the solution of the above system of equations.

- For each probe site, temperature growths resulting from particular transistors were added to give the total temperature growth in the selected probe site.

This method provided very good accuracy and the entire model could be created automatically with no additional design effort. Unfortunately, that mathematical model could not be parameterized, so this concept was abandoned.

Parameterized Properties

Without parameterization the thermal model would not be useful. It is obvious that a particular integrated circuit will not be used with only one kind of PCB. Therefore it is substantial to build the model so that the PCB parameters changes affect the values of model's elements. In other words, it must be parameterized.

On the other hand, the model of the IC itself needs not to be parameterized. No matter what kind of the PCB we use, the IC remains the same. This seems to be an obvious remark, but it is crucial to the parameterization process. When we look at the reduced model structure, we notice that the part representing the IC is far more complex than the part representing the PCB. The fact that the parameterization does not affect the IC part and we modify only the PCB part simplifies this process.

Influence of several important parameters was taken into account during the parameterization process. These included:

- PCB size
- PCB thermal properties
- upper and lower heat sink dimensions
- copper foil thickness
- number and diameter of the thermal vias

Model Decomposition

In order to make parameterization possible, we decomposed the model into several parts so that each part of the reduced model corresponds to the part of the full model structure. These parts were then reduced separately. (Fig. 3) This allowed evaluating the influence of the mentioned parameters on each part separately. Such an approach is essential, as determining this influence on the whole model at once would be extremely difficult. The influence of parameters on each part was examined using the full 3D model.

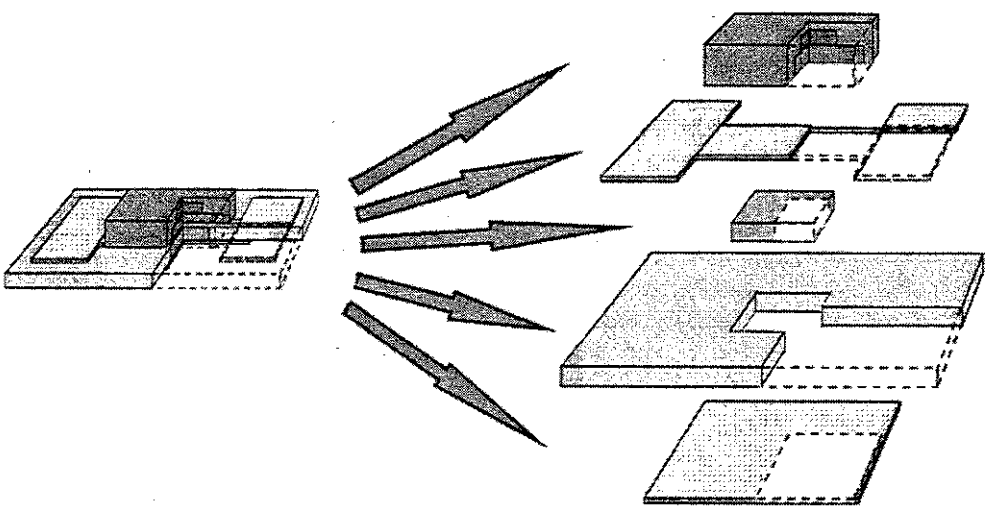

Figure 3. Model decomposition

Model Reduction Process

The following steps led to the creation of the reduced model:

- The model structure was chosen. The structure is based on the shape of the IC and PCB and the connections between its nodes represent the most important paths of the heat flow. The structure takes into account the fact, that the TMOS transistors - the only heat sources and the only points in which temperatures are to be calculated - are located in the IC. This results in a more complex structure of the IC part of the model and simplified PCB part. It should be underlined that this part of the reduction process was a difficult one, as at this moment there are no strict guidelines that help the designer choose the right model structure.
- Initial resistor values were computed separately for each active transistor. The temperature values were obtained from the TULSOFT simulations. At the same time, TULSOFT computed the heat flow through the sections corresponding to each resistor. The results were sufficient to calculate thermal resistances of each resistor. These values created initial points for optimization process.
- The resistor values were optimized using the Powell optimization algorithm. A special program optimized the resistor values so that the temperatures in the consecutive network nodes were equal to the temperatures in the corresponding points of the 3D model and the heat flows through the resistors were equal to the heat flows through the corresponding sections of the 3D model. Those values cannot be identical for all possible sets of power dissipation, so we optimized their values to receive minimal possible error. The stress was laid on minimizing the errors of temperature values rather than heat flows and the emphasis was placed on making the errors of temperature values in probe sites as small as possible.
- Next, the capacitor values had to be determined. Unlike the resistor values calculation, the initial capacitor values were calculated only on the basis of the dimensions and material properties of the PCB and the mold compound. Such an approach resulted in very coarse initial values, so in the preliminary state, the program performed an initial optimization using the Simplex algorithm in order to optimize those initial values for the Powell algorithm. The program optimized the capacitor values so that the differences between impulse responses were minimal.

Reduced Model Structure

The complete reduced thermal model consists of 17 resistors and 6 capacitors. Resistors R1 - R4 and capacitors C1 - C4 correspond to the mold compound (See Figure 4). Resistors R5 - R10 represent heat flows through the silicon substrate, solder layer and internal heat sink. R11 represents heat emission and convection via the top copper foil; R12 via the top surface of the board; R14 via the bottom surface of the board and R15 via the bottom copper foil. R13 is responsible for heat flow across the board, including thermal vias. Capacitors C5 and C6 represent laminate thermal capacity. Most of the thermal capacities were omitted, as the capacities of mold compound and laminate are dominant. During implementation in the SABER MAST language the ambient temperature was taken into account by connecting the resistors not directly to the ground but through a temperature source equivalent to the ambient temperature. However, all capacitors remained connected directly to the ground.

MODEL PARAMETERIZATION

Model parameterization required determining the sensitivity of the model elements on the structure parameters changes. Only the elements with high sensitivity were then parameterized.

In order to obtain the parameterized reduced model the following steps were applied:

- The temperature distributions for many - about 3000 - combinations of all parameters were computed using the full 3D model.
- For each combination the values of influenced resistors and capacitors were found. Most resistors were not affected during this process.
- From optimization we obtained functions describing the values of resistors whose domain was the set of parameters. However, as only a finite number of points from the domain were evaluated, the functions were defined only in these points. To implement the functions in the MAST language, we had to find analytic functions that in the evaluated points approximate the values obtained from optimization.
- Next, in a similar way, the analytic functions describing PCB capacitors values had to be determined.
- Implementing the analytic functions in MAST ends the parameterization process.

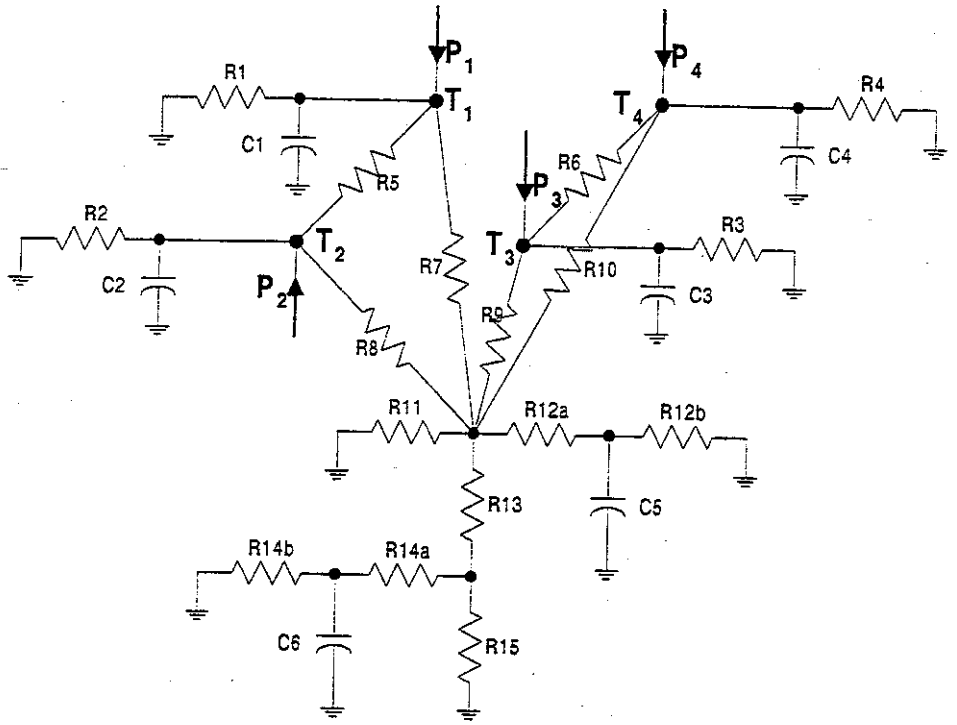

Figure 4. Reduced model structure

COMPUTATION TIME COMPARISON

The complete thermal model has been successfully implemented in SABER MAST language and coupled with the electrical part. From its simulations, two of its advantages became clearly visible:

- The results yielded by the model are sufficiently accurate, especially during the steady-state simulations. For temperature changes varying from 5 to 75 K the relative error was never greater than 10%. What is also important is that model always „assumes" a worse case than the real situation. This is a safe approach, because it prevents the designer from assuming that the device is still within the safe operation temperature limits when actually it is not.
- Computation time for electro-thermal model when compared to the pure electrical model increased by only 13%.

In the future we are going to extend the presented approach, in order to eliminate the steps of the model design process that cannot be automated.

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