Simulation of Electrothermal MOS Circuits using Saber

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ABSTRACT

In this paper we present a simple methodology for simulating small to medium sized circuits where electrical and thermal equations are solved simultaneously using Saber, a commercial, general purpose simulator. Dynamic electrothermal models have been developed representing both metal oxide semiconductor (MOS) and bipolar junction transistor (BJT) devices. The electrothermal models are then employed in the simulation of an infrared detector circuit, and a thermally isolated, suspended plate voltage controlled oscillator. Simulated results are compared to measured results taken from fabricated devices and systems. In all comparisons, the simulated data is in good agreement with experimental data.

Keywords: electrothermal modeling

INTRODUCTION

Over the past two decades there has been much work dedicated to the development of elaborate device models for circuit simulation [1]; however, temperature dependent circuit simulation models are not as readily accessible. The demand for electrothermal simulation tools has increased with the development of microelectromechanical systems (MEMS) which use MOS and BJT circuit technology for sensor systems [2], [3]. These systems exploit the electrothermal behavior of MOS and BJT devices for sensing purposes requiring accurate simulation models of these interactions.

When developing electrothermal circuits, a circuit simulator accounting for both electrical and thermal phenomena is needed. Fukahori [4] developed an electrothermal circuit simulator based on on SPICE2 [5]. This program considered the localized power dissipation effect on temperature gradients across the chip affecting the circuit performance, specifically for high accuracy applications. More recently, Lee [6] implemented an electrothermal simulator based on SPICE3 employing the incomplete Choleski conjugate gradient method to simulate DC electrical and steady-state thermal characteristics simultaneously. The implementation of these electrothermal simulators required large changes to the SPICE code and are not easily portable to current platforms.

In this paper we present a simple methodology for simulating small to medium sized MOS and BJT electrothermal circuits using Saber. Unlike SPICE, Saber provides a stable simulation environment that permits rapid model construction. This is possible due to Saber's analog hardware description language, MAST, which permits the use of state variables across different physical domains.

In the first section, we present the methods used to model the lumped electrothermal effects in both MOS and BJT devices followed by the parameter extraction and experimental verification of the models with fabricated devices. Next we present the simulation of several electrothermal microelectromechanical systems and comparisons with measured data.

ELECTROTHERMAL MODELING

The electrothermal device models developed here contain self-heating effects. The self-heating effects are lumped into a single temperature for each device which in turn affects the electrical characteristics. Therefore the expanded electrothermal model has an additional node representing the device temperature. The lumped electrothermal models of the MOS and BJT devices are shown schematically in Fig. 1 below where Q_S represents the lumped self-heating effect of the devices. In these models it is assumed that the

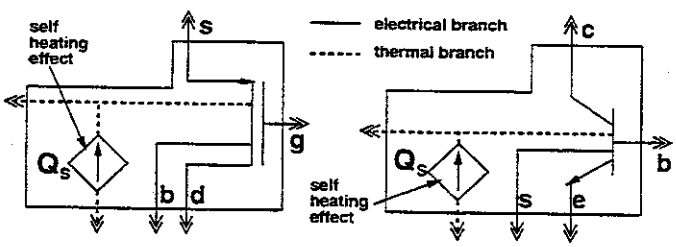

Figure 1: **Equivalent electrothermal circuit model for MOS (left) and BJT (right)**

power generated in the device is completely converted into the lumped heat source Q_S. In this approach, all the device temperature nodes are connected in a thermal network that determines the temperature of each device as functions of internal power dissipation and other external thermal signals. In this manner, the device temperatures are solved dynamically as additional state variables.

MOS Model

In this paper we modified the Berkeley Short-Channel IGFET Model (Level-13 BSIM) [1] to include electrothermal effects. The BSIM model is a good starting point because it has good convergence properties, a subthreshold drain conductance model, and the 71 model parameters are provided from the MOSIS fabrication facilities.

The electrical characteristics of MOS devices are temperature dependent. The main parameters affected by temperature are the effective carrier mobility $\mu(T)$ and threshold voltage $V_{th}(T)$ [7]. The carrier mobility decreases with temperature and is modeled as

$$\mu(T) = \mu_0 \left(\frac{T}{T_0}\right)^{-c} \quad (1)$$

where μ_0 is the mobility at temperature T_0 (27°C), and c is a constant fitting parameter. The threshold voltage is modeled as [1]

$$V_{th} = V_{fb} + \phi_s + K_1\sqrt{\phi_s - V_{bs}} - K_2(\phi_s - V_{bs}) - \eta V_{ds} \quad (2)$$

where V_{fb} is the flat-band voltage, ϕ_s is the surface inversion potential, K_1 and K_2 together model the non-uniform doping effect, and η accounts for the drain-induced barrier lowering effect and channel length modulation effect. The parameters which influence the threshold voltage are V_{fb} and ϕ_s [8]. Since the temperature variation of the threshold voltage is roughly linear [7], then both V_{fb} and ϕ_s are modeled as linear expressions with fixed temperature coefficients

$$V_{fb}(T) = V_{fb} + \alpha_{fb}(T - T_0) \quad (3)$$
$$\phi_s(T) = \phi_s - \alpha_s(T - T_0) \quad (4)$$

These new expressions were added to the BSIM Level-13 model written in Fortran and implemented in a new electrothermal BSIM model.

Both n-channel MOS (NMOS) and p-channel (PMOS) devices were fabricated using the Hewlett Packard (HP) 1.2 μm CMOS process, through the MOSIS service. NMOS gate dimensions were L = 4.2μm and W = 8.4μm and PMOS gate dimensions were L = 8.4μm, W = 4.2μm. The drain current was measured, with an HP 4145 Semiconductor Parameter Analyzer, from each device at different temperatures T = 30°C, 50°C, 75°C, 100°C and 125°C in both the linear and saturation regions as shown in the circuit configurations in Fig. 2. The device temperature was controlled with a thermal hot plate and temperature measured with a thermocouple.

Parameters c, α_{fb}, and α_s were extracted using a combination of MOSIS BSIM Level-13 parameters and experimental data collected from the fabricated devices. The parameters are determined through minimization of the error function

$$\Psi^2 = \sum_{j=1}^{N}\sum_{i=1}^{M}\left[I_{dsm}(V_{gs_j}, T_i) - I_{dsc}(T_i, V_{gs_j}, \alpha_{fb}, \alpha_s, c)\right]^2 \quad (5)$$

where I_{dsm} is the measured drain-source current, I_{dsc} is the drain-source current calculated from the electrothermal model, N is the total number of measurements per temperature setting, and M is the number of temperature experiments. The Levenberg-Marquardt method was used to numerically find the global minimum of Eq. (5). Table 1 contains the values of the parameters which minimize Eq. (5).

The MOS electrothermal model was tested under different circuit configurations. The plots in Fig. 2 depict the comparison between the measured and simulated $\sqrt{I_{ds}} - V_{GS}$ relationship at T = 30°C and 100°C for the NMOS and PMOS devices, respectively. For all cases, the temperature dependency has been captured very well. The zero temperature coefficient (ZTC) point is also verified here.

Table 1: **Electrothermal MOS Parameter Values**

Device	c	α_{fb}	α_s
PMOS	−1.62	4.125×10^{-3}	3.124×10^{-3}
NMOS	−1.46	4.582×10^{-3}	3.438×10^{-3}

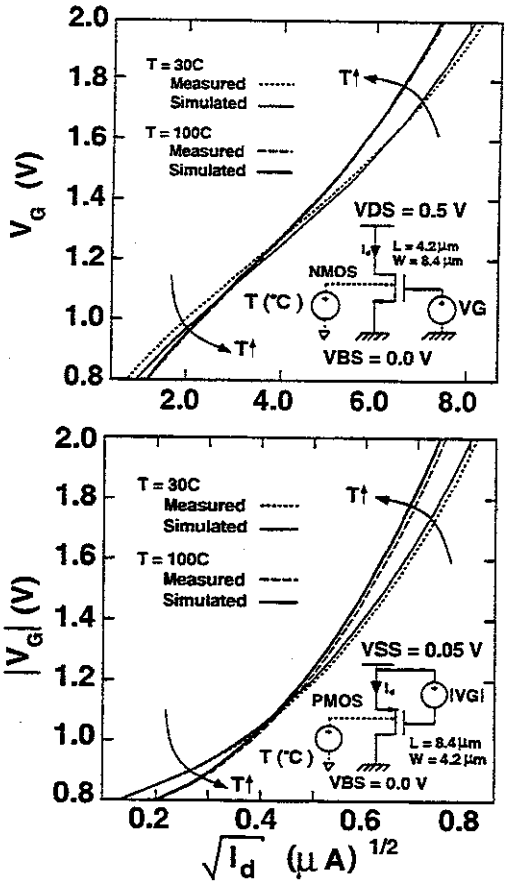

Figure 2: **Comparison of $\sqrt{I_{ds}} - V_{GS}$ characteristics at different temperatures**

BJT Model

The electrical characteristics of BJT devices are strongly temperature dependent. The electrothermal BJT model developed in this paper is a modified form of the Ebers-Moll implemented in SPICE2. In this paper we consider only the temperature effects in the saturation current I_s, and the DC forward and reverse current gain terms β_f, and β_r, respectively.

The temperature dependence of I_s, is caused mainly by the dependence on the square of the intrinsic concentration n_i^2, where the n_i is highly temperature dependent and is modeled as $n_i^2(T) \propto T^3 \exp\left(-\frac{E_g(T)}{kT}\right)$, where $E_g(T)$ is the band gap of the material also dependent on temperature;

modeled empirically as [9] $E_g(T) = 1.16eV - \frac{7.02\times10^{-4}T^2}{1108+T}$ for silicon. As in SPICE2, the temperature dependence of the saturation current is modeled as

$$I_s(T) = I_{s_0}\left(\frac{T}{T_0}\right)^{XT_{is}} \exp\left[\frac{qE_g(T_0)}{kT}\left(1-\frac{T}{T_0}\right)\right] \quad (6)$$

where I_{s_0} is the saturation current at temperature $T_0(27°C)$ and XT_{is} is a parameter to be determined from measured data. The temperature dependencies of the DC forward β_f and reverse β_r current gain parameters are modeled as

$$\beta_f(T) = \beta_{f_0}\left(\frac{T}{T_0}\right)^{XT_{bf}}, \qquad \beta_r(T) = \beta_{r_0}\left(\frac{T}{T_0}\right)^{XT_{bf}} \quad (7)$$

where β_{f_0} and β_{r_0} are defined at temperature T_0. Although β_f is also highly dependent on the collector current [10] it was found from fabricated devices that in the operation limits of our applications, β_f is approximately independent of the collector current, called the mid-current region of β_f. This is shown in Fig. 3 where β_f is plotted from measured data of fabricated devices for several temperatures. In addition, an emission coefficient, n, was added to the exponential terms of the model for low current operation.

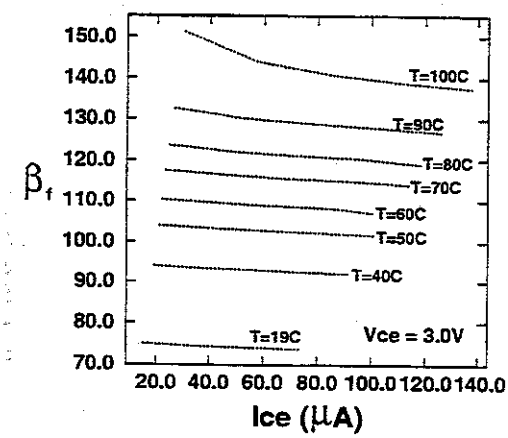

Figure 3: **Plot of DC forward current gain β_f dependence on temperature and collector current I_{ce}**

NPN devices were fabricated using the IBM 1.2 μm CMOS process, through the MOSIS service. The collector current was measured, with an HP 4145 Semiconductor Parameter Analyzer, from each device in the temperature range $20 \leq T \leq 100°C$, with base currents ranging from $I_{bb} = 0.2\mu A$ to $I_{bb} = 0.8\mu A$, and a collector to emitter voltage range of $0.0 \leq V_{ce} \leq 3.0V$.

Parameters XT_{is}, XT_{bf}, and n were extracted using a combination of MOSIS parameters and experimental data from fabricated devices using a method similar to that for the MOS devices. Table 2 shows the extracted parameter values for the fabricated NPN device.

Table 2: **Electrothermal NPN Parameter Values**

Device	XT_{is}	XT_{bf}	n
NPN	1.46	3.24	2.55

Comparisons between simulated results and experimental results are shown for a few temperatures in Fig. 4. Results for higher temperatures are similar. For temperatures below $T = 70°C$ the electrothermal behavior of the BJT is captured well. However, for temperatures of 70°C or greater the devices displayed a pronounced kink at the knee of the I_{ce} - V_{ce} curve, shown in the bottom plot of Fig. 4. As temperature increases further the kink expands vertically. The simple model developed here does not account for this thermal effect; however it does predict the behavior of saturated devices with very good accuracy.

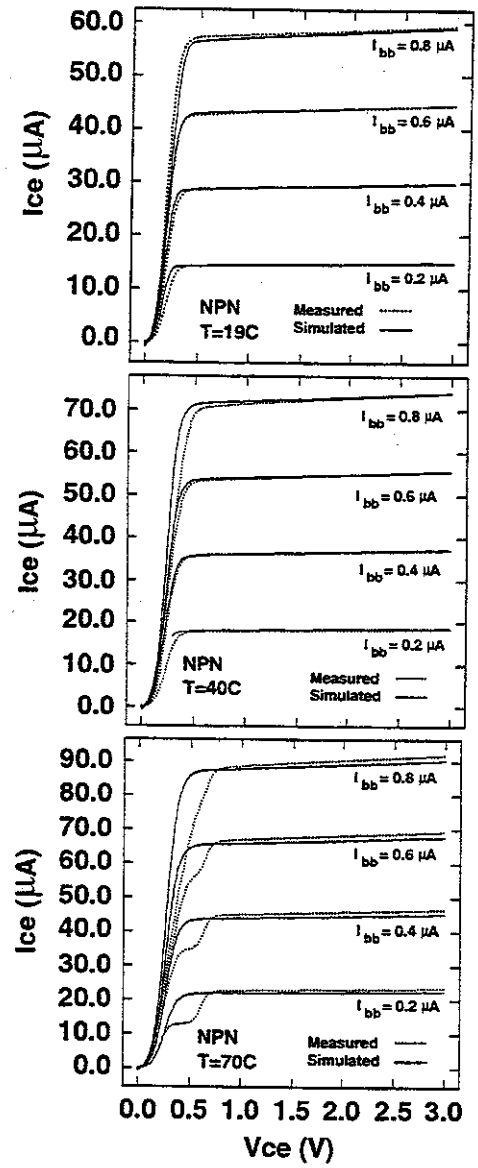

Figure 4: **BJT results for (top) $T = 19°C$ (middle) $T = 40°C$ (bottom) $T = 70°C$**

SABER IMPLEMENTATION

The implementation of the MOS and BJT electrothermal models into the Saber environment required the modifica-

tion of existing model files. In the case of the electrothermal MOS model, the Level-13 BSIM model was modified. The original BSIM model contained only electrical connection nodes for the drain (d), gate (g), source (s), and bulk (b). Thermal nodes were added to this model since Saber can distinguish between electrical and thermal systems. The Saber BSIM model references Fortran routines which were changed to reflect the electrothermal behavior described in the previous section. The model files are actually coded in ratfor (Rational Fortran) and the compiler and library files are available with the Modeling Toolkit available from Analogy, Inc.

The electrothermal BJT equations were programmed in the Saber programming language, MAST. The inclusion of the electrothermal behavior also required the use of both newton step and piecewise linear evaluation control to be discussed later.

Adding new dependencies, such as temperature, into the existing model equations can create systems of very nonlinear equations making it difficult to find a solution. Saber uses the Newton-Raphson algorithm to find the DC operating point and transient (Katzenelson algorithm is also available for transient solution) solutions to the system of nonlinear equations. The Newton-Raphson algorithm used in Saber is an iterative procedure which linearizes the nonlinearities as one of the steps in the iteration loop. Saber provides two control settings that improve the solution finding ability of the Newton Raphson algorithm. The first setting specifies sample points in the model that define the corners of a piecewise linear approximation of nonlinear continuous device characteristics. Therefore, by increasing the sample point density at selected regions the piecewise linear approximation used in Saber can model critical parts of the nonlinear characteristics with adequete accuracy. For example, the knee of the $I_{ce} - V_{ce}$ characteristic, shown in Fig. 4, has a sample point density 20 times any other regions. The second setting specifies the maximum newton step size for each independent variable in the electrothermal device model. A sufficiently small newton step setting prevents the simulator from skipping over important regions of nonlinearities. The sample points and newton step settings are programmed in the control section of the MAST model template.

Figure 5 depicts a simple example electrothermal system consisting of a suspended, thermally isolated PMOS device. The thermal nodes are connected to a thermal network that models heat losses and capacity of the system. The electrical nodes d, g s, and b are connected to voltage sources V_{ss} or V_{gs} and the electrical ground. Thermal node *tamb* is connected to a temperature source T_{amb} representing the ambient temperature of the system. Thermal node *tdevice* represents the device temperature and is connected to the thermal network of thermal impedance R_{th} and thermal capacitance C_{th}.

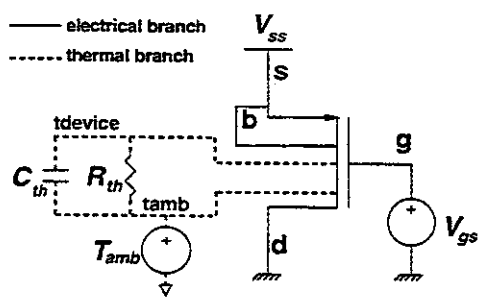

Figure 5: **Electrothermal circuit example**

The saber netlist for this system is shown below. The electrothermal BSIM model is called *mbsimtherm.1* where

```
# read parameters externally file: parameters.text
<parameters.dat

# electrical network
v.vdd d 0 = dc = 5.0
v.vgs g 0 = dc = 1.0

# MOS electrothermal device
mbsimtherm.1 d g s b tdevice tamb = \
                sthd=1, w=4.2u, l=8.4u, \
                dmodel=pmos1, imodel=pmos2, \
                alpha_fb=4.125m, alpha_s=3.214m

# thermal network
tempsrc.tamb tamb 0 = dc = 27
ctherm.cth tdev tamb = 101.2e-9 #(J/K)
rtherm.rth tdev tamb = 4.97e4   #(K/W)
```

sthd=1 activates the subthreshold conduction model, *dmodel = pmos1* and *imodel = pmos2* read the model parameters, and *alpha_fb* and *alpha_s* represent the α_{fb} and α_s, respectively.

To illustrate the calculation of transient electrothermal behavior we use the example shown in Fig. 6 which consists of three devices M1, M2, and M3. Devices M1 and M2 are on a thermally isolated plate; hence are thermally isolated from device M3. The transistor pair M2 and M3 form a current mirror with bias current set by I_{bias}. When device M1 receives a current pulse from I_{IN}, the self-heating effect of M1 causes a temperature change of the plate which in turn induces a current change in M2. Depending on the

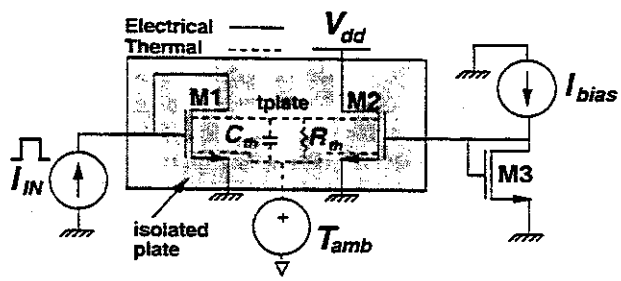

Figure 6: **Circuit configuration for showing electrothermal simulation**

bias current I_{bias}, device M2 can display either a negative or positive temperature coefficient. Figure 7 shows plots of the input current, plate temperature, and the drain current of under two different bias conditions. The scales on the left and right sides correspond to bias currents of 800nA and 1μA, respectively. For $I_{bias} = 1\mu$A and the drain current

in M2 decreases with temperature, but for the lower bias current it increases as predicted by Fig. 2.

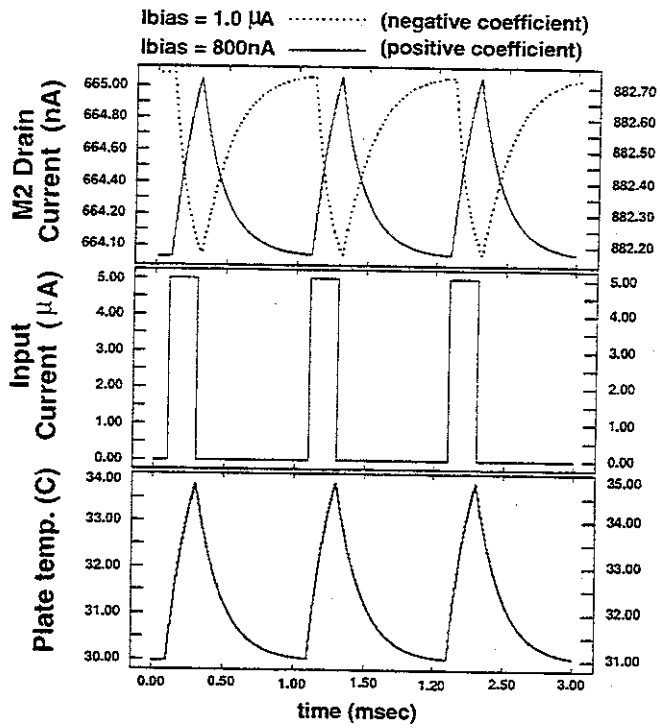

Figure 7: **Simulation results depicting positive and negative temperature coefficients**

EXPERIMENTAL VERIFICATION

In this section, simulated results are compared to experimental results for two microelectromechanical systems: an infrared detector and a voltage controlled oscillator (VCO).

Infrared Detector

The first simulated circuit is the infrared detector [2], shown in Figs. 8 and 9. The detector was fabricated using a

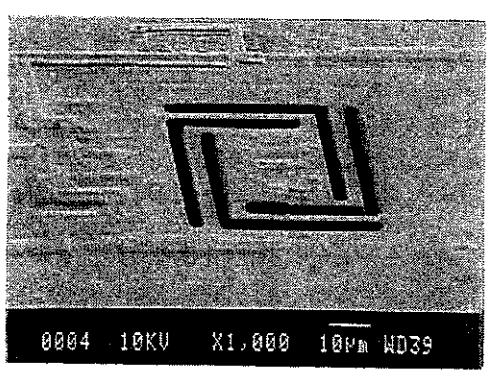

Figure 8: **SEM photograph of infrared detector**

conventional CMOS process with one post-process electrochemical etch that released a n-type well forming a thermally isolated, suspended plate.

Figure 9 shows the circuit diagram. PMOS devices M4 and M5 are located on the suspended plate hence their characteristics are susceptible to heating caused by absorbed incoming radiation. NMOS devices M2 and M3 form a cascode high impedance current source referenced to I_b. Since the PMOS devices are thermally isolated, the bias current raises the suspended well temperature 1-5 °C above the substrate. When heat radiation is absorbed by the suspended

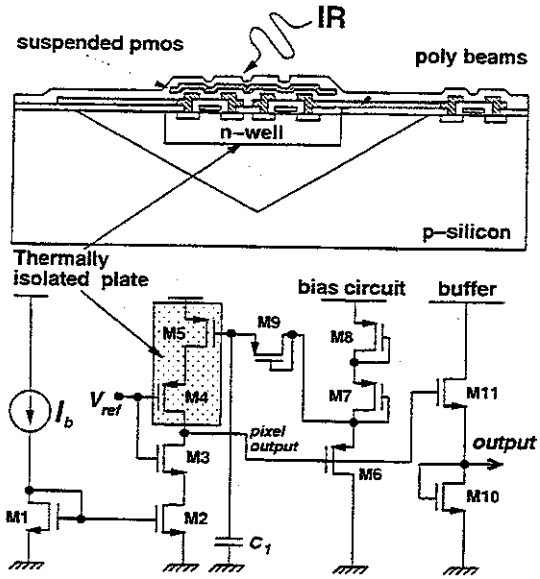

Figure 9: **(top) Cross-section of infrared detector device (bottom) Infrared detector circuit diagram**

plate, the plate temperature increases further inducing a reduction of the threshold voltage V_{th} in M4 and M5. Since the gate voltage of M1 is essentially constant, the transient reduction in V_{th} decreases the voltage drop across plate devices M4 and M5 resulting in a overall reduction in the power dissipation of the plate hence a drop in the plate temperature. This phenomena constitutes an electrothermal feedback loop that tends to maintain a constant plate temperature.

An important measure of the detector performance is the responsivity. The responsivity is a ratio of the change in output voltage to the change of the incoming radiation to the plate. The comparison between the measured and simulated responsivity is shown in Fig. 10. The electrothermal simulation results show a reasonably close match with the measurement result.

Voltage Controlled Oscillator

Figures 11 and 12 show a thermally stabilized VCO fabricated with the same process. This ring type VCO consists of three stages of inverters located on a thermally isolated plate. PMOS drivers MP4, MP5, MP6 and PMOS loads MP1, MP2, MP3 are formed as an inverter chain. The oscillating frequency is controlled by the bias current I_{bias}. The temperature of the plate is controlled using additional temperature stabilization circuits and an independent heater not shown in the diagram for simplicity.

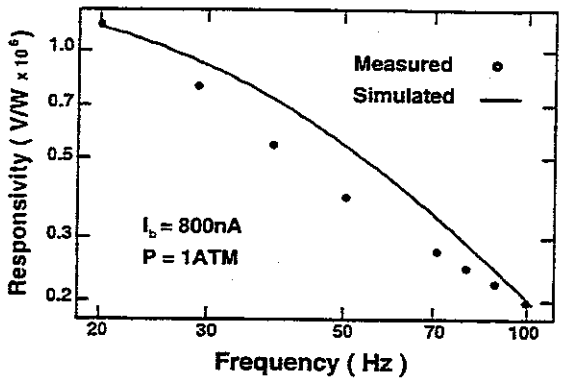

Figure 10: **Comparison between measured and simulated responsivity of the infrared detector**

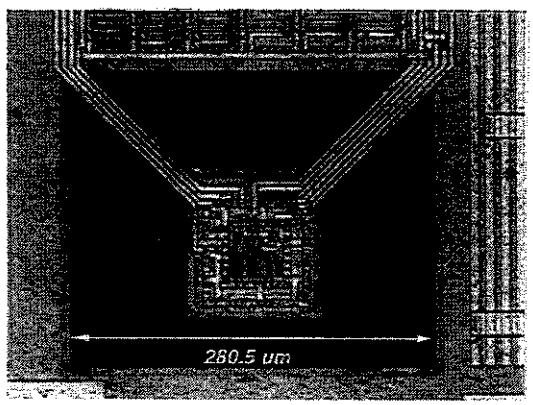

Figure 11: **Voltage controlled oscillator photograph**

This circuit was analyzed with Saber using the electrothermal transistor models. This simulation was performed in two steps. First the DC operating point was found. Then nodes (A), (B), and (C) were forced to 5V, 0V, and 5V, respectively and then the transient simulation was performed. The DC electrothermal simulation predicted a plate temperature increase of $\Delta T \approx 16°C$. The oscillation frequency matches results from experiments as shown in Table 3.

The added capability of coupled thermal and electrical state variable simulation does not come free of cost. The simulation execution time for electrothermal systems is in general larger than for an electrical system. When the oscillator circuit was simulated without thermal effects a DC solution is found in 0.1 sec while the DC solution for the electrothermal system required 1.87 sec. Similarly the ratio of execution times for transient electrothermal simulation to transient electrical simulation was found to be approximately $\frac{24.2 \text{ sec}}{3.2 \text{ sec}}$. The one order in magnitude increase in execution time is consistent with reported values for other electrothermal simulation programs [4].

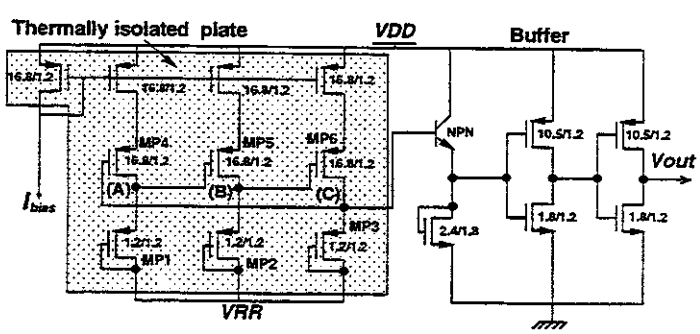

Figure 12: **Schematic diagram of voltage controlled oscillator circuit**

Table 3: **Voltage controlled oscillator results**

Result	Freq.(MHz)
Measured	62.7
Simulated	61.2

CONCLUSION

In this paper we have presented the practical aspects of simulating electrothermal MOS and BJT circuits using Saber. The electrothermal MOS model is an extension of the Level-13 BSIM model, and the BJT model is a modified version of the Ebers-Moll model. Comparisons between simulated and experimental data for an infrared detector and a voltage controlled oscillator are in good agreement.

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