Simulation of mixed signal systems in standard VHDL

H. Grätz * and W.-J. Fischer**

* Fraunhofer Institute of Microelectronic Circuits and Systems, IMS2 Dresden
Grenzstraße 28, D-01109 Dresden, Germany, graetz@imsdd.fhg.de
** Semiconductor and Microsystem Technology Laboratory, Dresden University of Technology
Mommsenstr. , D-01062 Dresden, Germany, fischer@ehmgw1.et.tu-dresden.de

ABSTRACT

Historically, the analogue and digital parts of a hardware design have been modelled and simulated in different environments and could not be combined in a single simulator. On the other hand, if a design contains both analog and digital parts simulating their interactions are most important to reliably verify the design. Therefore, we present a method for simulating analogue circuits and digital components in a VHDL simulator.
For executing analogue simulations in a VHDL environment an analogue simulator has been developed. It permits to model linear and non-linear circuits using only standard VHDL language elements. This fact allows a similar conversion of this method to different VHDL environments. A netlist is used to model the analogue parts with elements from a model library. In order to interface analogue and digital parts A/D and D/A converter elements are be used. This allows signal feedbacks between both parts during the simulation.

Keywords: mixed signal simulation, VHDL, system simulation

INTRODUCTION

A major problem in ASIC design process is the simulation of complete mixed signal systems. In fact, in many simulation environments this is not possible at all. The simplest approach to rely on a pure analogue simulation becomes extremely difficult and time-consuming for complex circuits. Extensive hard- and software resources have to be provided.
A better solution is to use simulators which can handle semantic constructs, for describing both, analogue and digital components. The VHDL standard 1076 does not allow the description and simulation of analogue networks, despite it is most appropriate for simulating digital circuits. The new extension 1076.1 introduced in September 1996 specifies elements for describing continuous-time signals [1]. Ensuring reasonable convergence and an efficient simulation of the used models is a demanding task for a designer. Already the description of small analogue circuits already requires a considerable effort for design entry and modelling. Therefore is has been proposed [2] to provide parameterized models, which can be adapted by the designer. Other VHDL based approaches for simulating mixed signal systems are based on coupling different simulators.
In contrast to these approaches a method will be presented which embeds the simulation of analogue components directly into a standard VHDL simulator. No additional analogue engine or a special simulator interface is necessary. It is easily possible to investigate the hardware description of a digital design which include analogue parts in a single simulation of the complete system. This includes even the bidirectional feedback between digital and analogue parts. A model library provides a variety of basic analogue elements. The analogue circuit is described by a netlist using the models from this library.

IMPLEMENTATION

The hardware description language VHDL provides a variety of elements for describing circuits and systems. Furthermore, elements are defined which allow the abstract description of algorithms. However, these elements cannot be synthesized to hardware. Examples are variables and operations with floating point numbers, physical data types and file operation functions [3].
Based on these elements complex algorithms can be described in VHDL as in other high level languages such as C or PASCAL. Including additional packages allows to use exponential and trigonometric functions.
The simulation of analogue circuits requires network analysis techniques. An analogue circuit is described by a netlist which is built from elements of a model library. After deriving the network equations they can be solved numerically. According to the type of network equations different methods for analysing networks can be distinguished, e.g. analysis of node voltages or loop currents [4]. For a straightforward coupling of an analogue network to digital components via analogue digital and digital analogue converters the method of node voltage analysis has been chosen.
A network is referred as dynamic network if it contains time-depending current and voltage sources and/or components capable of storing energy. Modelling such networks leads to systems of first degree differential equations.

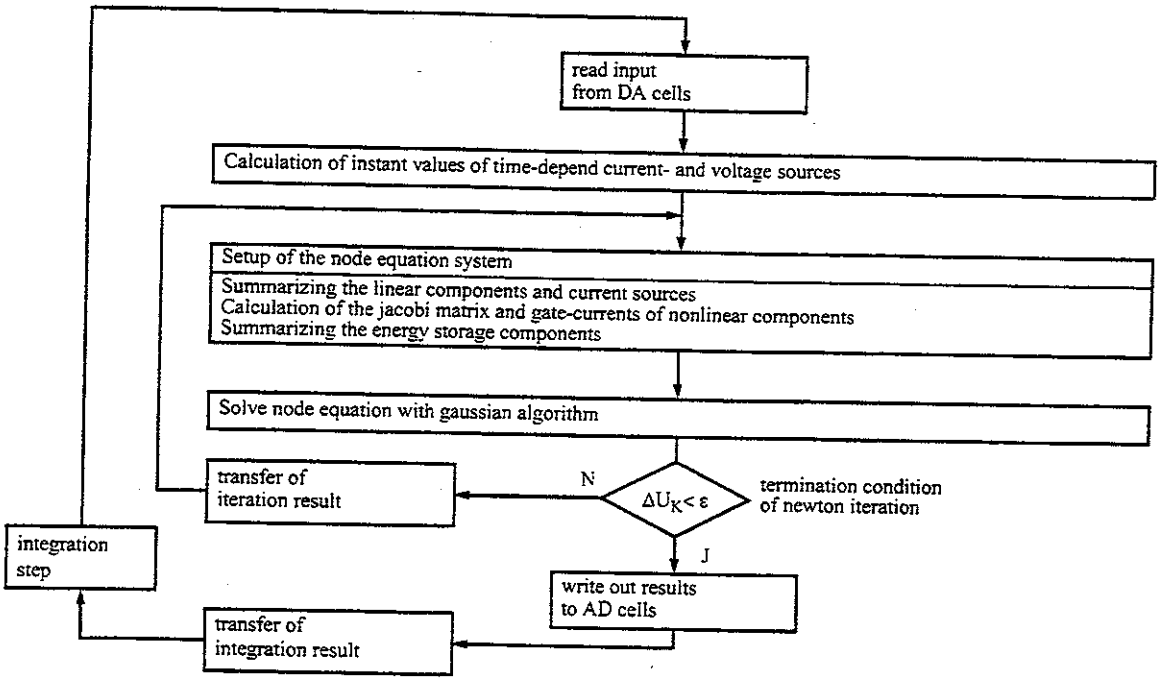


Figure 1. Analogue simulation flow

The solution requires a numerical integration in the time domain which is performed by the Euler-formula. This method is very stable and can be easily programmed. The drawback of a comparatively low accuracy can be avoided by choosing very small integration steps at costs of an increase of the required computation time. For simulating non-linear components the Newton-iteration method is used. A diagram of the simulation flow is shown in Figure 1.
The node voltage analysis can be described with the following equation system

$$Y\vec{U_k} = \vec{I_Q} \quad (1)$$

where Y is the node conductance matrix, $\vec{I_Q}$ the source current vector and $\vec{U_k}$ the node voltage vector. The node conductance and the source current for each model element is defined by its own electrical parameter set. The position in the conductance matrix and in the source current vector were determined from the netlist file, which contains the topological parameters of the analogue circuit. The solution of the equation system delivers the voltage for each node in the circuit.
The concept of building the network simulator is described in [5]. It has been adapted to the VHDL environment and complemented by various features.
A special simulation flow exists for a simulation of digital circuits which takes care for events performed in parallel by the simulated hardware. In VHDL such parallel events are referred as concurrent statements which are described by processes. The control is achieved by a list of so called sensitive signals or by *WAIT* commands within the process. Whenever a signal from the sensitivity list changes or the condition of a *WAIT* command is satisfied, the corresponding process is activated.
During the simulation the actual time is increased. Whenever a time stamp is reached, for which a transaction is scheduled, this transaction will be executed. Due to the fact that the execution of a transaction may cause the activation of a process, "Delta-Cycles" have to be performed at each point of the simulation until a stably state of the circuit has been reached.
In contrast for analogue simulations a constant integration step width is used. For each integration step a new calculation of the analogue network is required. If the simulator is equipped with an automatic step width control simulation time can be saved by a variable adaption of the step width. The principle of the automatic step width control is based on the estimation of the discrete error of the numerical integration by evaluating the difference between a forecasted value and the result of the calculation. If this difference is within a given limit ε the step width can be increased and vice versa.
To simulate digital and analogue parts in parallel in the same simulator a special simulation sequence has been developed. Whenever the analogue part has to be updated, the D/A converter cells estimate an analogue voltage from the digital input for the specified nodes and simulates nodes voltages for the analogue network at the actual integration step. The resulting node voltages are converted in there digital representation by the A/D cells. Then, the analogue simulator holds down for the specified integration step width. The digital parts are updated in case of a signal transition how.

Figure 2 shows the "parallel" procedure of the digital and analogue part simulation in the same simulator.

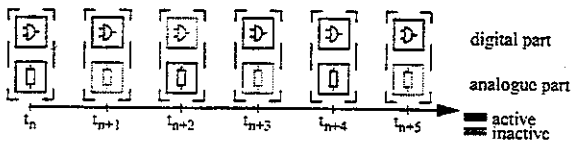


Figure 2. Parallel digital and analogue simulation

The analogue simulator has been implemented as a functional description in a VHDL model. For simulating the analogue part in a digital model the description of the analogue simulator has to be referenced by an instance. The ports of the simulator and the digital model have to be connected. A digital model may instantiate more than one analogue circuit. Thereby the analog circuits have to form the lowest level in the hierarchy, see Figure 3. It is not possible to reference digital modules from an analogue circuit. However, the data exchange between analogue and digital components is possible in both directions during the simulation.

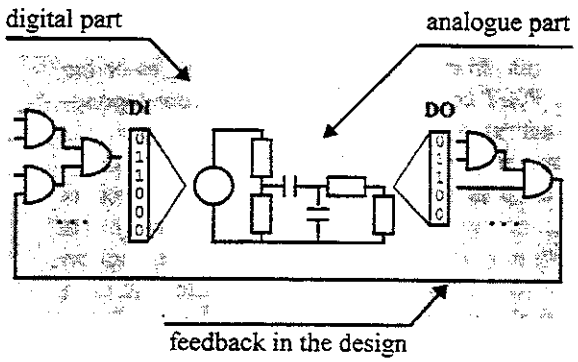


Figure 3. Simple design hierarchy and their connections

The description of the interfaces of the analogue circuit contains an input port *di*, an output port *do* and the parameters *di_num*, *do_num*, *network_file*. The parameters *di_num* and *do_num* determine the bitwidth of the digital ports. The parameter *network_file* denotes the name of the netlist. Figure 4 shows an example instantiation of an analogue circuit.

```
astable_multivibrator : anw
  generic map (
    di_num => , -- bitwidth of input vector
    do_num => , -- bitwidth of output vector
    network_file => "astb_mv.nw"
  )
  port map (
    di => , -- digital input vector
    do =>  -- digital output vector
  );
```

Figure 4. Example instantiation of one analogue part

The model library contains linear and non-linear elements as well as special components for describing analogue circuits. The linear elements are resistor, capacitor, inductance, non-controlled and controlled source. Diode, bipolar transistor, MOS-transistor and OPV represent non-linear components. It is easily possible to extend the libraries by additional elements.

The modelling of the voltage source element is shown in Figure 5. A voltage source is described by a current source and a resistor. In order to generate the network equations for the voltage node analysis the conductance from the two terminals is written to conductance matrix *a* and the model depending source current of the node numbers to the source currents vector *b*.

```
when 'E' => -- voltage source
  -- [k1] + [k2] -
  -- [w1] U in V, [w2] Ri in kOhm
  a(k1,k1) := a(k1,k1) + 1.0 / w2;
  a(k1,k2) := a(k1,k2) - 1.0 / w2;
  a(k2,k1) := a(k2,k1) - 1.0 / w2;
  a(k2,k2) := a(k2,k2) + 1.0 / w2;
  b(k1) := b(k1) + w1 / w2;
  b(k2) := b(k2) - w1 / w2;
```

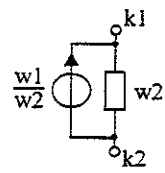
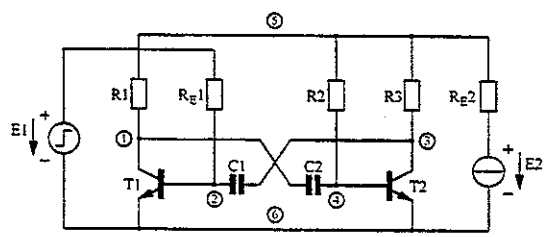


Figure 5. Example of element modelling

Special elements serve for simulation control. For instance, it is possible to select a node of an analogue network and to track its node voltage during the whole simulation in a separate protocol file. D/A- and A/D converter cells connect analogue and digital parts of the circuit. The properties of these cells can be defined in the netlist file. The simulation control base on the netlist. It contains the number of nodes in the circuit, the reference node, the integration step width, and the finish time of the analogue simulation beside the list of elements and their interconnections.

RESULTS

For a demonstration of the properties of the analogue simulator the circuit of an astable multivibrator built from bipolar transistors has been described, instantiated in a digital testbench, and simulated. In Figure 6 the circuit and its netlist representation is depicted. The voltage source E1, realizing an initial step, stimulates the circuit.




```
6 6 1u 200u                C1 2 3 0 0 4700p 0 0 0
E1 2 6 0 0 5 12k 0 1       C2 1 4 0 0 6800p 0 0 0
E2 5 6 0 0 5 1000          T1 2 6 1 0 1 0 0 0
R1 5 1 0 0 220 0 0 0       T2 4 6 3 0 1 0 0 0
R2 5 4 0 0 12k 0 0 0       p0 0 0 0 0 0 0 0 0 0
R3 5 3 0 0 220 0 0 0       P1 3 0 0 0 0 0 0 0 0
```

Figure 6. Schematic and netlist of the multivibrator

Figure 7 shows the voltages of node 1 and node 2 in a real time interval of 200 µs.

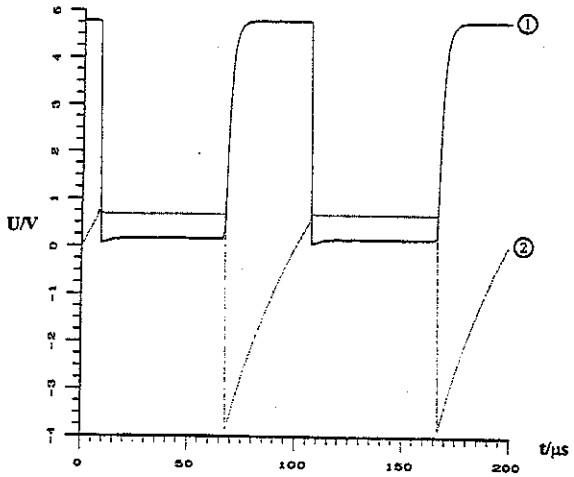


Figure 7. Simulation result of the multivibrator

The described mixed mode simulator has been applied for developing a microsystem [6] consisting of a radiation sensor and a digital signal processing unit. The signal processing is performed by a 8-bit microcontroller described by a VHDL model. To perform a complete simulation the model of the microsystem has been described and simulated after developing the analogue circuit. The controller software has been designed using the simulation model of the microsystem.

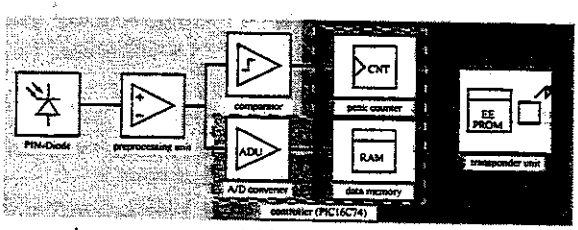


Figure 8. Blockdiagram of the microsystem

Figure 8 shows the components of the microsystem and the mapping of its components to the elements of the simulation environment. Figure 9 shows the output signal of the radiation sensor (1), the output voltage after the pulse shaper (2) and the output voltage of the sample and hold amplifier (3) of the analogue part for radiation detection in the microsystem.

As a second application example, this mixed signal simulation method has been applied to develop an electronic identification system. For the identification sequence the procedure of one way authentication is used. The system includes an integrated circuit using the DES standard as cryptographic unit.

The electronic identification system consists of a fixed and mobile part. The fixed part includes a microcontroller, a cyptographic unit, the clock generator and the power supply for the complete system. Actuators can be controlled additionally by the microcontroller. The mobile part consists of a cryptographic unit and a clock generator. For the data transfer and power supply a two contact connection exist.

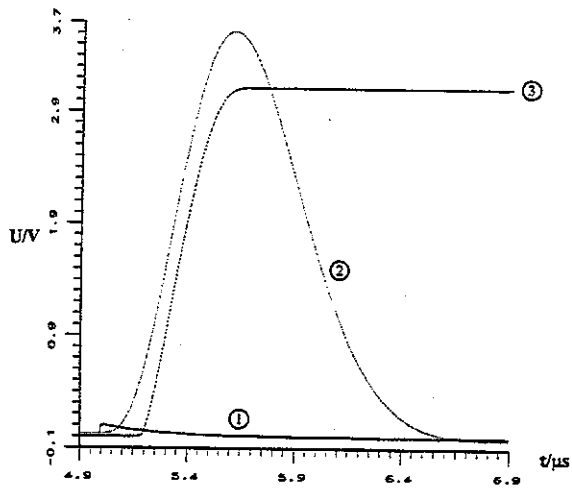


Figure 9. Simulation results of radiation sensing system

In the communication sequence a 64 bit random number, which is generated by the microcontroller is transferred to the mobile part. After decrypting it with a defined cipher key through the DES circuit the 64 bit cipher is retransmitted to the fixed part. The required electrical energy for the transmission and decrypting process transferred via the two contacts.

At present, it is important to test whether the transmitted energy is sufficient to operate the mobile circuit. For the complete system simulation behavioural models of the circuits were used. The electrical characteristics of the circuit, for instance power consumption, are known at this time.

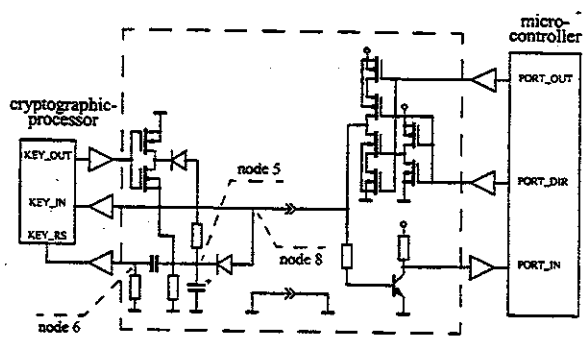


Figure 10. Schematic of the simulated identification system

The communication channel, parts of the digital circuits, and the energy storage capacitor for the mobile part are described as analogue part in the digital system. In order to reproduce the power consumption of the mobile part a resistor is connected in parallel to the storage capacitor. In Figure

10 the schematic of the analogue circuit and the coupling elements to the digital unit are shown.
The simulation results depicted in Figure 11 show the correct function of the specified transmission protocol, the dimension specification of this circuit part, and the realisized controller software.

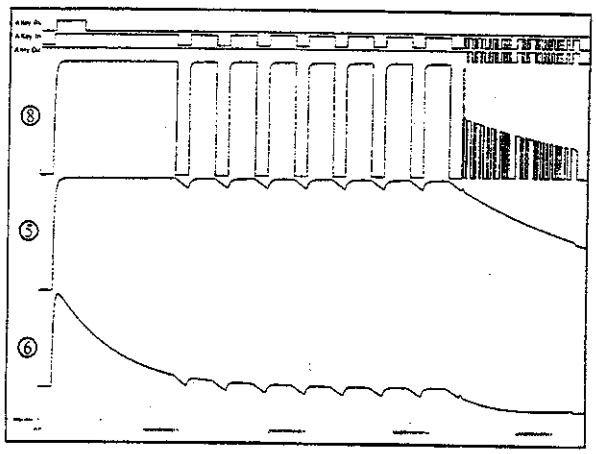


Figure 11. Simulation results of the identification system

Node 8 shows the voltage at one coupling contact. Node 6 in combination with a capacitor and a resistor produce the system reset for the mobile part when a data transfer block is started. The voltage fluctuation over the energy storage capacitor is shown at node 5. The real time for one identification cycle is 440 ms.

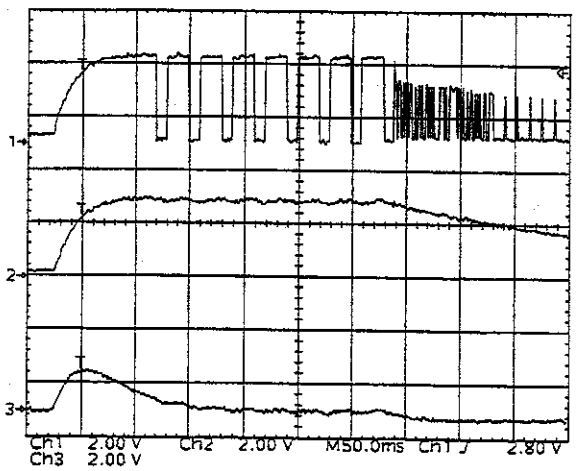


Figure 12. Measured results of the identification system

In order to verify the results obtained with the simulation system, Figure 12 depicts the measurement results of the actual system, showing the same signals as Figure 11. The simulated behaviour is reproduced within usual tolerance limits.

SUMMARY

The presented simulation system allows the investigation of analogue and digital components using a VHDL based digital simulator. Thus, investigations of the behaviour of mixed signal systems with analogue and digital components influencing each other become possible in a single simulator. The analogue simulator implemented in VHDL provides necessary basic functions for simulating analogue circuits. No special interfaces (simulator coupling, data files) or additional software for simulation are required.
The results achieved by the realized analogue simulator lack the precision of commercial analogue simulation tools, but this had not been the demand of this work.
The simulation system is especially suited for a analysis of digital systems including a few analogue elements such as transmission channels, sensors and analogue preprocessing unit. Since the analogue simulator is not restricted to calculate time continuous electrical processes the described approach is also suited to analyse e.g. mechanical-electrical systems.

OUTLOOK

Future work will include the improvement and extension of the simulation models, the integration of an automatic control for the integration step width, and the development of a user-friendly netlist entry.

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