Simulations of a new CMOS compatible method to enhance the breakdown voltage of highly-doped shallow PN junctions.

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ABSTRACT

Avalanche breakdown often limits the working range of planar junction diodes in electronic circuits and in sensors. We present two-dimensional device simulation results (using MEDICI) of a novel CMOS compatible structure. It combines a floating field limiting ring and a metal field plate in order to enhance the breakdown voltage V_{bd} of highly-doped shallow planar junctions. Electrical simulations have shown that a single field limiting ring is effective in increasing V_{bd} only if placed at a distance d smaller than 300nm. For d=100nm, breakdown even occurs over the plane diode. At distance d=400nm, the field ring can enhance the breakdown voltage only if combined with a metal field plate. V_{bd} increases linearly with negative applied gate voltage, with a proportionality factor of about 0.1. For a gate voltage of -10V, V_{bd} increases by about 12 % up to -12.8 V. Measurements on diodes integrated in standard industrial CMOS 0.5 µm process corroborate with simulation results.

Keywords: avalanche breakdown, field limiting ring, metal field plate, shallow junction, CMOS.

INTRODUCTION

Avalanche carrier generation plays an increasing role in MOS devices. By scaling down the geometrical dimensions while keeping the supply voltage constant, the electrical field increases and therefore impact ionization plays a more important role in device degradation due to hot-carrier effects and bipolar parasitic breakdown [1]. The working range of planar junction diodes in electronic circuits and in sensors is often limited by avalanche breakdown. Different techniques have been used to reduce the detrimental effect of junction curvature on the breakdown voltage, like the introduction of a low-doped guard ring or the use of a $p\pi\nu$ profile [2]. The depletion region is forced to have less curvature or greater thickness at the edge of the junction so that the peak electric field is reduced there. Although very efficient, these methods are not CMOS compatible: they require additional well-controlled implantations that can only be realized in non-standard processes. The use of one or more floating field limiting rings [3] has been investigated to increase the junction breakdown voltage. Optimally placed floating field rings reduce junction curvature effects and lower surface electric fields. It is also known [4-6] that V_{bd} of planar diodes can be modulated with a potential applied to a metal field plate over the oxide-protected junction at the surface. These methods have been used with success in low-doped junctions.

In this work, we present two dimensional device simulation results of a new structure combining a field limiting ring and field plate. The edge of the diode is very similar to a MOSFET, with a polysilicon gate used as a metal field plate in between the junction and the field ring. This CMOS compatible method is used for breakdown voltage enhancement in highly-doped shallow planar junctions. The first section describes the structure that has been realized and simulated. In the second part, electric device simulations are presented. The influence of the field ring and of the field plate on V_{bd} is studied separately. Finally, measurement results are presented and compared with the simulations.

STRUCTURE

The structure proposed to increase the breakdown voltage of pn junctions is shown in Figure 1. It combines a floating field limiting ring placed at a distance d from the diode junction and a field plate in-between on top of a gate oxide. A shallow junction is formed between the P^+ layer and the N_{well}. The diode structure is embedded in a N_{well}. A second junction exists between the N_{well} and the substrate, with both sides

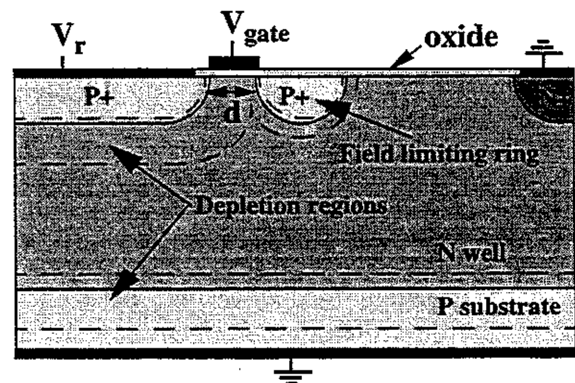

Figure 1: The structure consists of a P^+N_{well} shallow junction, surrounded by a P^+ field limiting ring at distance d. A voltage V_{gate} is applied on a field plate placed between the diode and the guard ring. N_{well} and $P_{substrate}$ are grounded. Depletion regions and electrodes are shown in the figure.

connected to ground. A floating field limiting ring with a width of 1.5 μm is implanted at a distance d from the main p-type layer, with the same junction depth. A field plate is placed between the diode and the guard ring, on top of a 100 Å oxide. It is made using the polysilicon gate of the CMOS process.

The doping profiles of test structures, realized in a standard industrial 0.5 μm CMOS process, have been measured using the secondary ion mass spectroscopy (SIMS) method. The results are shown in Figure 2. The junction depths are 280 nm and 1500 nm. The P^+ peak concentration is 4 10^{19} cm^{-3}, the N well concentration at the Si / SiO_2 interface is 4 10^{17} cm^{-3}.

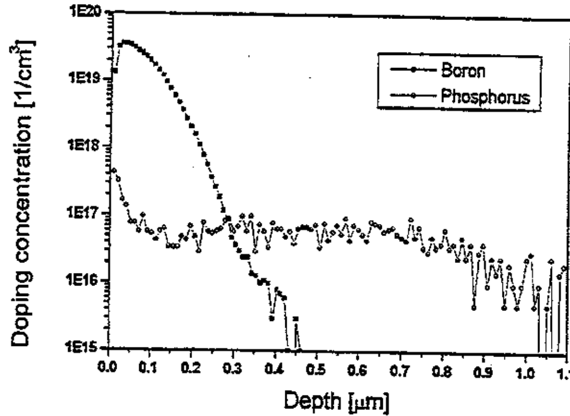

Figure 2: SIMS profiles of boron and phosphorus measured on integrated devices. The shallow junction depth is 280 nm.

ELECTRICAL SIMULATION

The structure of Figure 1 has been simulated using the electric device simulator MEDICI. The two-dimensional nature of the electric field makes the use of 2D simulations necessary. Maes et al have shown that if one applies the simple one-dimensional theory to the problem of designing field ring devices, very poor design would result [1]. For symmetry reasons, only half of the diode was simulated. The impurity profiles introduced into the simulator have been fitted to the measured SIMS profiles of Figure 2.

Simulation models

Different models have been used in the device simulator in addition to the default models. Shockley-Read-Hall is included for the thermal bulk and surface recombination process. A model was chosen that takes trap-assisted and band-to-band tunneling into account in the Shockley-Read-Hall recombination at high electric fields. Auger recombination is also included. A mobility model using the parallel electric field component was used.

In order to simulate the electrical behavior close to breakdown, an impact ionization model was necessary. It includes carrier generation due to impact ionization in the solution self-consistently, with the generation rate G for electron-hole pairs expressed by:

$$G = \alpha_n \frac{|\vec{J_n}|}{q} + \alpha_p \frac{|\vec{J_p}|}{q}$$

with α_n and α_p the electron and hole ionization coefficients, J_n and J_p the electron and hole current densities. The ionization coefficients are expressed in function of the local electric field according to Chynoweth's law [7]:

$$\alpha_n = \alpha_{n\infty} \exp\left(-\frac{b_n}{E_{np}}\right)$$

$$\alpha_p = \alpha_{p\infty} \exp\left(-\frac{b_p}{E_{pp}}\right)$$

with E_{np} and E_{pp} the electric field components in the direction of current flow. $\alpha_{n\infty}$, $\alpha_{p\infty}$, b_n, b_p are experimentally determined parameters.

In the following simulations, the breakdown voltage V_{bd} is defined as the reverse voltage which makes the multiplication factor M_n approach infinity. With W the depletion layer width,

$$M_n = \frac{1}{1 - \int_0^W \alpha dx}$$

Fixed positive surface charges Q_{ss} in the oxide affect device characteristics, especially at low doping levels [2]. However in the CMOS process used for the realization of the diodes, Q_{ss} in the gate oxide is small and the doping concentration is high. For these reasons, the effect of surface charges was neglected in the simulations.

Great care was given to the mesh generation because the discretization of the structure is source of errors, especially in the simulation of the avalanche process. If the discretization mesh is coarse, the results can be erroneous even when the program converges [1]. A fine grid is required to correctly simulate the current increase due to avalanche generation. The pragmatic approach used was to reduce mesh size in critical regions until no significant change was noticeable.

Field limiting ring

First the effect of the field limiting ring on the breakdown voltage was simulated by varying the distance d between the junction and the field limiting ring. A structure similar to the one shown in Figure 1 but without gate has been used in these simulations. Figure 3 shows the I(V) characteristic for d = ∞ and for d between 400 nm and 100 nm. Without field limiting ring (d = ∞), breakdown occurs at a reverse voltage V_{bd} = -11.29 V. A decrease of the distance d up to 300 nm does not influence V_{bd}. The field limiting ring is effective in supporting a portion of the applied voltage

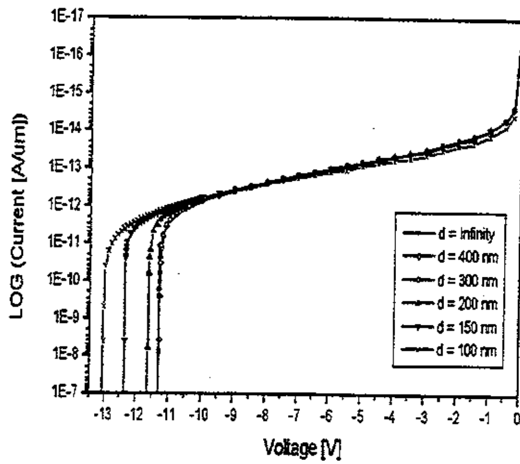

Figure 3: Simulated I(V) characteristic for different distance d between the junction and the field limiting ring. The structure has no metal field plate.

only for d smaller than 300 nm, which is about the depletion layer width at punchthrough. For d=100 nm , $|V_{bd}|$ increases by 16 % up to -13 V. Figure 4 shows the influence of the field limiting ring on the current flow lines distribution. For a reverse voltage V_r = -11.29 V, the upper structure with d=400 nm already suffer from avalanche breakdown, whereas the lower structure with d=200 nm shows homogenous current flow lines. The effect of the field limiting ring on the potential distribution is illustrated in Figure 5. In the upper graph, d is larger than the sum of the lateral depletion layer widths of the junction and of the guard ring. The field ring has no effect on the breakdown voltage. On the other hand, for d=200nm, the depletion layer of the diode reaches the guard ring. The floating field limiting ring supports 22% of the applied reverse voltage. It lowers the lateral edge electric field and increases $|V_{bd}|$.

For d=100 nm the lateral voltage drop is large enough so that avalanche breakdown occurs over the entire parallel plane, as shown in Figure 6. The breakdown voltage (13.05V) is higher by 1.76V than V_{bd} of the corresponding planar diode without guard ring, and corresponds to the breakdown voltage of the plane diode. A premature breakdown at the cylindrical junction is avoided.

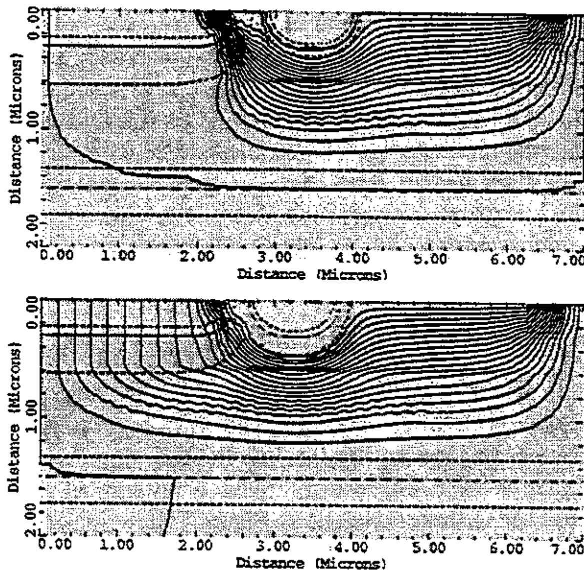

Figure 4: Current flow lines and depletion layers for a diode voltage V_r = -11.29 V. The field limiting ring of the upper (lower) structure is placed at 400nm (200nm), respectively. 5 % of the current flows between two adjacent current lines.

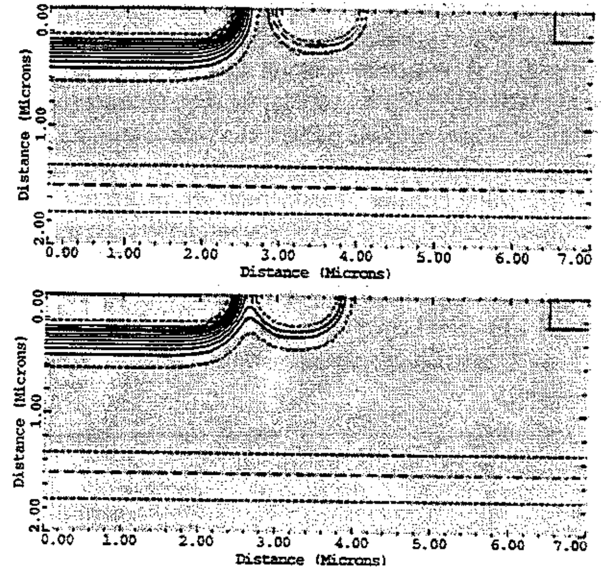

Figure 5: Potential lines and depletion layers for a diode voltage V_r = -11.29 V. The field limiting ring of the upper (lower) structure is placed at 400nm (200nm), respectively. The potential drops by 10 % between two adjacent potential lines.

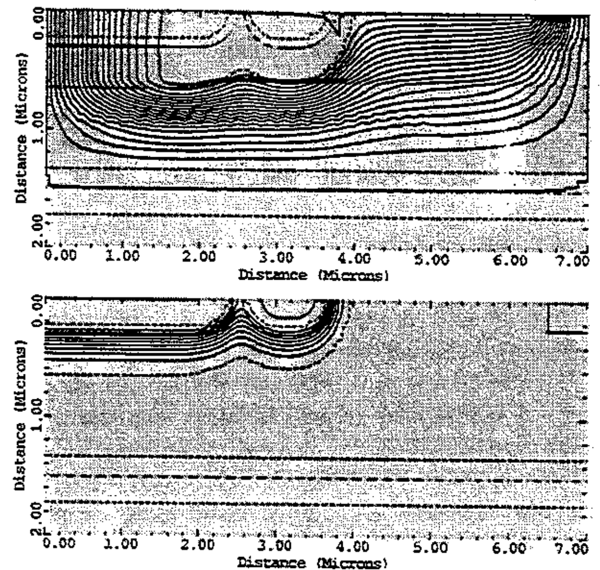

Figure 6: Current flow lines and potential lines for d=100 nm at breakdown voltage (V_r = -13.05 V).

Metal field plate

We have shown in the previous section that in the case of highly-doped shallow planar junctions, a floating field limiting ring is effective in increasing the breakdown voltage only if the distance d between the junction and the guard ring is made smaller than 300 nm. However, two reasons limit the use of this method in practical applications. The first is that in CMOS technologies the minimal spacing between two active regions is large if no polysilicon gate is designed in between. The polysilicon gate is used as a mask layer during the implantation. In the 0.5 μm process we used for the realization of the diodes, the minimal allowed spacing between two active regions is 0.8 μm, while the effective channel length of a MOSFET is 0.4 μm. Another reason that limits the use of a single field limiting ring is that only very few processes are commercially available with effective channel lengths smaller than 300 nm.

We show in this section that an increase of the absolute value of the breakdown voltage is possible even for a distance d=400 nm. This is achieved by the combination of a metal field plate with the field limiting ring. The MOSFET polysilicon gate electrode is used as metal field plate in between junction and field plate, as shown in Figure 1.

When the gate voltage is made smaller than -2 V, the volume under the gate, in between the junction and the field ring, becomes depleted. The depletion layer of the junction, that was not large enough to reach the field limiting ring without metal field plate, is now able to merge with that of the ring. The electric field at the cylindrical junction decreases, causing the point of maximum field to be located deeper in the semiconductor. Figure 7 shows the current flow lines and the potential lines for d = 400 nm, a reverse voltage V_r = -11.29 V and a gate voltage V_{gate} = -8 V. It has

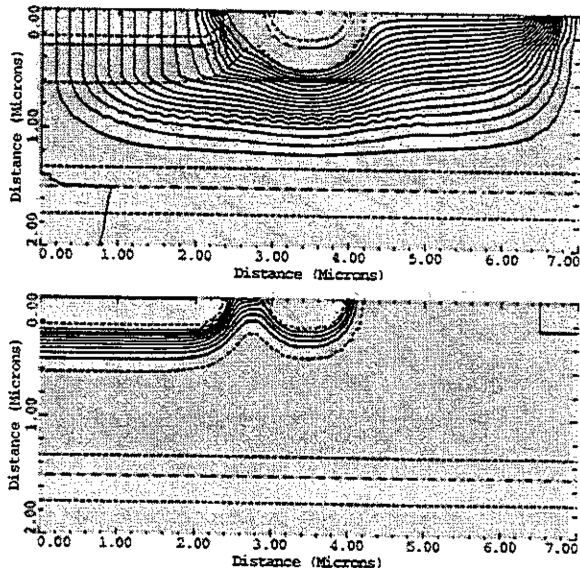

Figure 7: Current flow lines and potential lines for d = 400 nm, V_r = -11.29 V and V_{gate} = -8 V.

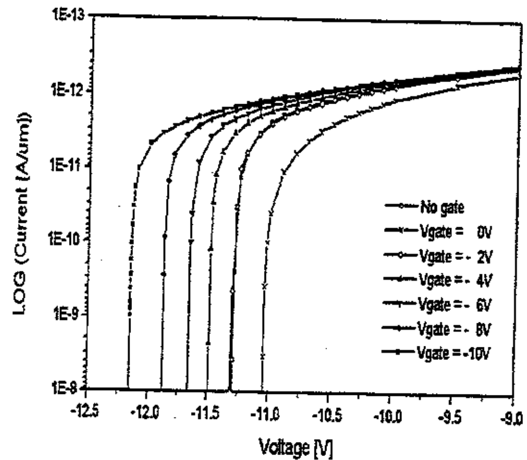

Figure 8: Simulated I(V) curves for different gate voltages V_{gate}, for d=400 nm. The response of a structure (called "No gate") without field limiting ring and without metal field plate is shown as well for comparison.

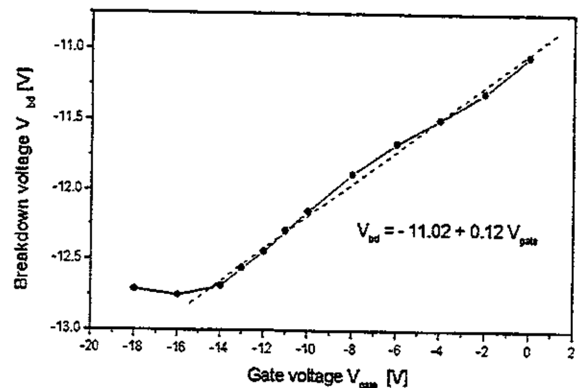

Figure 9: Simulated breakdown voltage V_{bd} versus gate voltage V_{gate}, for d=400 nm. Between 0 and -14 V, V_{bd} depends linearly on V_{gate}. Saturation is observed at higher voltages.

to be compared with the upper simulations of Figures 4 and 5, where the same distance d and reverse voltage were used, but without metal field plate. The flowlines are now homogenously spread over the plane junction, and the potential of the field ring decreases from 0 to -5 V. The I(V) curves for different gate voltages are shown in Figure 8. The breakdown voltage without any metal field plate is -11.29 V. For gate voltages V_{gate} higher than -2 V, the depletion layer width at the surface of the junction decreases and $|V_{bd}|$ becomes smaller. The breakdown voltage for V_{gate} = 0 V is -11.04 V. On the contrary, the application of a gate voltage lower than -2 V increases $|V_{bd}|$. For V_{gate} = -10 V, the breakdown voltage is -12.15 V. Figure 9 illustrates the relation between V_{bd} and V_{gate}. The breakdown voltage depends linearly on V_{gate} for voltages between 0 and -14 V, as already mentioned in [5]. The proportionality factor is 0.12. For V_{gate} < -14 V, the breakdown voltage saturates at about -12.75 V. But in practice the gate shall not be biased with

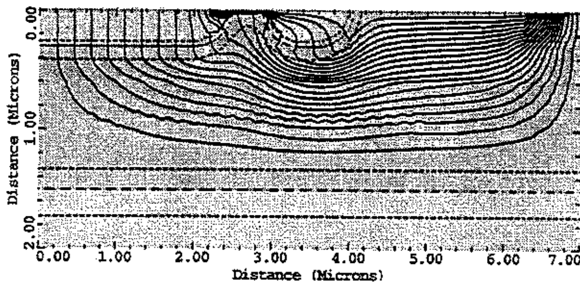

Figure 10: Current flow lines for d = 400 nm, V_r = -1 V and V_{gate} = -8 V.

voltages higher than about -10 V in order to avoid gate-oxide breakdown.

It is interesting to note that the breakdown always occurs at the cathode and not at the edge of the field ring, even when the gate is biased negatively. This can be explained as follows: for sufficiently large negative bias applied to the gate, the MOS is inverted. A surface inversion layer is formed between the field limiting ring (the floating source) and the cathode (the drain). Figure 10 shows the flow lines for V_r = -1 V and V_{gate} = -8 V. Part of the current effectively flows from the diode to the ring. The voltage in the field ring is equal to V_r. But at higher reverse voltages, the current increases, creating a voltage drop in the channel. No current flows to the ring and breakdown occurs at the cylindrical junction of the cathode. This is illustrated in Figure 7 for V_r = -11.29 V and V_{gate} = -8 V.

The voltage difference between the cathode and the ring is equal to 0 at low reverse voltages because a conductive channel exists between them. At breakdown voltage, the potential difference reaches its maximum value (7V), without current flow between the cathode and the ring. This means that the amount of channel hot-electrons injected in the gate oxide is small, resulting in no significant device degradation.

MEASUREMENT RESULTS

In order to test the simulation results, diodes have been integrated in a standard industrial CMOS 0.5 µm process. A cross-section of the diode edge structure is shown in Figure 1. The distance d between the junction and the floating field limiting ring is the effective channel length of the MOSFET, which is 400 nm. The total diode area is 0.56 mm^2. A large diode area was justified by the fact that these diodes were to be used as avalanche photodiodes. The diodes have an octagonal shape, as shown on the photograph of Figure 11. This diode geometry was prefered because it has the lowest corner curvature possible in this technology. Avoiding sharp corners in the design is necessary if one wants to approach cylindrical junction breakdown. For comparison, another structure was realized without floating field limiting ring and without metal field plate.

The I (V) characteristic was measured with a semiconductor parameter analyzer, with the chip shielded in a test fixture. A reverse voltage was applied on the P^+ anode, with the N-well and the P-substrate connected to ground. A long integration time was necessary to avoid undesirable charging of parasitic capacitances. The measured I (V) curves for different gate voltages V_{gate} are shown in Figure 12. They can be compared with the simulated I (V) characteristic of Figure 8. In order to keep the simulation duration reasonably small, only the edge of the two-dimensional structure was simulated. This implies that the absolute value of the simulated current can not be converted to an effective diode current. But the shape and the value of the breakdown voltage can be directly compared with the measurement results.

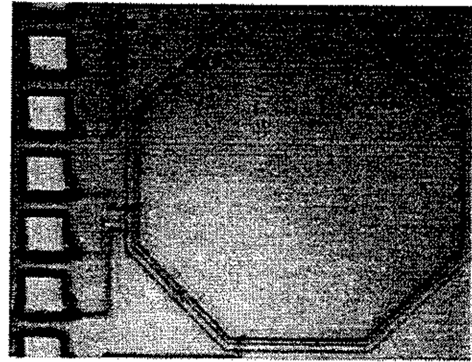

Figure 11: Photograph of the diode realized in standard industrial CMOS 0.5 µm technology. Total diode area is 0.56 mm^2.

The leakage current of the diode, measured at room temperature, is only 500 fA for a reverse voltage of 100 mV and a diode area of 0.56 mm^2.

First consider the structure without field limiting ring and without metal field plate (called "No gate" in the legend

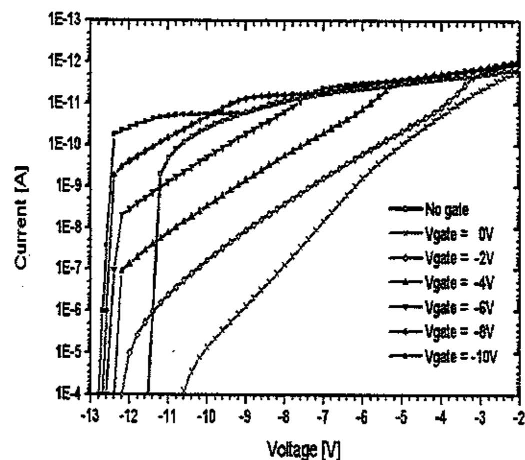

Figure 12: Measured I (V) reverse characteristic for different applied gate voltages V_{gate}, with d=400nm. The response of a structure (called "No gate") without field limiting ring and without metal field plate is shown as well for comparison.

of Figures 8 & 12). In this case, the measured and simulated I (V) characteristic follow almost perfectly the same shape. The measured breakdown voltage V^m_{bd} = -11.5 V is in very good agreement with the simulated value V^s_{bd} = -11.3 V. When a voltage is applied on the gate electrode, the measured I (V) curves deviate from the ideal simulated case, particularly at low gate voltages. But the qualitative behavior of V_{bd} is in good agreement with the simulation results. As the current was limited to 0.1 mA in order to avoid destructive mechanisms, no clear breakdown is observed for V_{gate} = 0 V. For gate voltages lower than 0 V, V_{bd} depends linearly on the gate voltage, as already noticed in the simulations. The proportionality factor is 0.09, slightly lower than the simulated value (0.12).

The combination of a floating field limiting ring at a distance d = 400 nm and of a metal field plate biased with - 10 V gives a breakdown voltage of - 12.8 V. This value is 1.3 V lower than the breakdown voltage obtained from the structure without field limiting ring and without field plate.

CONCLUSION

In this paper, two-dimensional electric device simulations of a novel CMOS compatible structure for breakdown voltage enhancement have been presented. The structure combines a floating field limiting ring placed at a distance d from the diode junction and a metal field plate in between on top of a gate oxide. The structure is very similar to a MOSFET, with a polysilicon gate used as metal field plate. It is to be used in highly-doped shallow PN junctions with low breakdown voltages. Structures have been realized in a standard industrial CMOS 0.5 μm technology in order to verify the simulation results.

Electrical simulations have shown that the field limiting ring alone is effective in supporting a part of the applied voltage and thus increase the breakdown voltage if the distance d is made smaller than 300 nm. For d = 100 nm, the absolute value of the breakdown voltage increases by 16 % up to - 13.05 V, which is about the breakdown voltage of the plane diode. It is shown that the current flow lines are homogenously spread over the entire parallel plane.

Even though the effective channel length of MOSFETs in commercial processes is usually larger than 300 nm, breakdown voltage enhancement can be achieved if the field ring is combined with a metal field plate. The application of a negative voltage on the gate allows the depletion layer of the junction to reach that of the field limiting ring. This means that the electric field at the cylindrical junction decreases, causing the point of maximum field to be located deeper in the semiconductor. When a negative voltage is applied on the gate electrode, the breakdown voltage increases linerarly: $V_{bd} = m\ V_{gate} + cst$. The simulated proportionality factor m (0.12) was close to the measured one (0.09). For a gate voltage of -10 V, the measured absolute value of the breakdown voltage increases by about 12 % to - 12.8 V. The presented method is effective in enhancing the breakdown voltage of highly-doped shallow junctions and allows a good control of avalanche breakdown mechanism.

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