Simple Method of Characterizing CMOS Channel Dopant Profiles Using CV Technique

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ABSTRACT

In CMOS process and device simulations, characterization of complete dopant profiles in the channel region is essential for accurate simulations. We have developed a simple, fast and inexpensive methodology for characterizing CMOS channel dopant profiles using analytical equations, which can be calibrated and validated easily using CV measurements. The calibrated model can predict channel dopant profiles for complex redistribution and diffusion process like dopant loss of phosphorus in PMOS devices.

Keywords: Channel dopant profiles, Dopant redistribution, Process modeling, CV

INTRODUCTION

In CMOS transistor the shape of the dopant profiles in the channel region is critical for device performance. Typically an ion implantation step is used to insert a predetermined amount of dopant into the substrate. The dopant profile is then redistributed subsequently by the growth of the gate oxide and the thermal anneals. The redistribution of the dopant profiles is a moving boundary problem with segregation occurring at the silicon/oxide interface. Since there are no exact closed form solutions available, process simulators like SUPREM™ solve the diffusion equations numerically for the channel dopant profile redistribution from oxidation and thermal steps. These simulations take a long time when used for process optimization.

In this paper we develop approximate analytical expressions for the redistributed dopant profiles and use a simple CV technique to determine the complete channel dopant profiles. The models are based on the previously reported work of Lee *et al.* [1]. Lee models are only applicable for the redistribution of the dopant profiles during oxidation. We have extended their model to include the effect of thermal anneals following the oxidation process. Our model is also able to simulate multiple anneals and oxidation steps, which are usually done in device processing. The analytical model provides a better insight, compared to the numerical solution, into the various physical processes affecting the final redistributed dopant profile. The analytical model also uses considerable less computer time than the numerical solvers. Using the analytical model and CV (pulse CV [2] and standard CV) measurement we developed a technique by which, we were able to obtain channel profiles for NMOS and PMOS devices. We were also able to predict the anomalous phosphorus pileup behavior [3] in PMOS channel region.

ANALYTICAL MODEL

In our model we assume that the as-implanted profiles can be approximated by a gaussian initial distribution.

$$N(y) = N_{Max} \exp\left[-\frac{(y-R_p)^2}{2\sigma^2}\right] \tag{1}$$

Where R_p is the range, σ is the standard deviation and N_{Max} is the maximum concentration for the as implanted dopant profile.

The impurity concentration profile during subsequent oxidation and anneals is governed by the following diffusion equation (The diffusion coefficient D is assumed to be independent of dopant concentration and only dependent on the temperature of the thermal process, y = 0 is the location of the silicon/oxide interface).

$$\frac{\partial N}{\partial t} = D\frac{\partial^2 N}{\partial y^2} \quad y \geq 0 \tag{2}$$

subject to the following boundary conditions:

semi-infinite boundary condition

$$N(\infty, t) = 0 \qquad t \geq 0 \tag{3a}$$

Moving boundary condition

$$D\frac{\partial N}{\partial y}\bigg|_{y=0} = \left(\frac{1}{m} - \alpha\right) N(0,t)\frac{dY_{ox}}{dt} \tag{3b}$$

m = Segregation coefficient
α = Ratio of thickness of consumed silicon to thickness of grown oxide
Y_{ox} = Thickness of the oxide grown

The initial distribution of the dopant species in silicon is given by equation (1).

The equation is solved taking into consideration the moving oxide-silicon interface and the segregation coefficient. The one dimensional solution for the redistribution of the dopants during oxidation is given by [1]:

$$N(y,t) = N_1(y,t) + N_2(y,t) \tag{4}$$

Where N_1 is the redistribution due to the inert ambient and N_2 is the redistribution due to the oxidizing ambient. Details of the expressions are in the appendix.

Figure 1 shows the result of a typical oxidation step. The total dopant profile is given by N(y,t). The two components of the expression $N_1(y,t)$ and $N_2(y,t)$ are also shown. From the figure it can be seen that the contribution of $N_2(y,t)$ (redistribution due to dopant segregation) to the final dopant profile is significant only close to the surface. This is expected because the effect of segregation during oxidation is only confined to a region close to the silicon/oxide interface.

We extended the models previously developed by Lee *et al.* to simulate a sequence of multiple processes like oxidation and thermal anneals using effective values of diffusion and segregation coefficient. Lee's models simulated either a pure oxidation or a thermal diffusion step. In device processing the gate oxidation step is usually followed by thermal anneals. To calculate the dopant profile after inert thermal anneal the profile descriptor's "Dt" and "A" have to be updated. A method to do the updating is described below.

The expression $N_1(y,t)$ is for impurity redistribution due to thermal diffusion in a non-oxidizing ambient. Therefore its contribution after a thermal step (ΔDt) is calculated by:

$$Dt_{New} = Dt_{Old} + \Delta Dt \tag{5}$$

The expression $N_2(y,t)$ is for impurity distribution resulting from impurity out-diffusion from the silicon during oxidation. In an inert ambient the thermal step will not increase the thickness of the oxide grown. It has been shown by Douglas *et al.* [2] that during inert thermal anneals the silicon/oxide interface acts as a perfect reflecting boundary condition, i.e. there is no loss of dopants across the interface during the anneal. Therefore using the conservation of total amount of dopant we get the following expression for $N_2(y,t)$ after a thermal step (ΔDt):

$$\int_0^\infty N_2(y,t)dy = \int_0^\infty A\, erfc\left[\frac{y+\alpha Y_{ox}}{2\sqrt{Dt}}\right]dy = \text{constant} \tag{6}$$

which evaluates to

$$A\sqrt{\frac{Dt}{\pi}}\left[e^{-\gamma^2} - \gamma\sqrt{\pi}\, erfc(\gamma)\right] = \text{constant} \tag{7}$$

where:

$$\gamma = \frac{\alpha Y_{ox}}{2\sqrt{Dt}} \tag{8}$$

The new updated value of parameter "A" can be calculated from the following expression.

$$A_{New} = A_{Old}\frac{\sqrt{Dt_{Old}}}{\sqrt{Dt_{New}}}\left[\frac{e^{-\gamma_{Old}^2} - \gamma_{Old}\sqrt{\pi}\, erfc(\gamma_{Old})}{e^{-\gamma_{New}^2} - \gamma_{New}\sqrt{\pi}\, erfc(\gamma_{New})}\right] \tag{9}$$

Dt_{New} is calculated from equation (13).

For fast, inexpensive calibration and validation of the analytical models, we measure the channel dopant profiles using the technique of pulse CV [2]. Pulse CV technique is able to determine the complete channel carrier dopant concentrations except for a few Debye lengths (L_D) at the Si-SiO_2 interface. Pulse CV is very similar to the standard CV dopant profiling technique. To obtain profile information from deeper into silicon the device is sent into deep depletion by applying a pulsed voltage at the gate instead of a steady ramp-up in voltage for standard CV. To determine the surface concentration and dopant profile near the surface we tune simultaneously the analytical model (effective segregation coefficient (m) and the thermal diffusion parameter (Dt)) to match the flatband voltage from the standard high frequency CV data.

PROCESSING AND MEASUREMENT

The MOS-capacitors (MOSCAPs) were made on 6" silicon wafers. The channel implants were implanted through a screen oxide. A 4nm gate oxide dielectric was grown. A n^+ doped polysilicon was used as the gate electrode. No S/D or drain extender implants were done on the wafers (to allow pulse CV measurements). Aluminum metal contacts were put on the polysilicon gate to give a good contact to the probers. Aluminium was also put on the back side of the wafer for the substrate contact to the probers. Standard CV and pulse CV measurements were also made on the MOSCAPs.

RESULTS AND DISCUSSION

The analytical model for dopant redistribution was compared to the dopant profiles from a numerical solver (SUPREM). The following set of conditions were simulated in SUPREM:

- <100> silicon was implanted with a Boron gaussian profile (Dose=1e13, Range=0.051 μm, σ=0.0296 μm).

- Gate oxidation at 850 °C for 10 minutes to grow an oxide thickness of 65 A^0.
- Inert anneal at 900 °C for 20 minutes.

Using the same values of the diffusion coefficient, segregation coefficient and oxidation growth parameters as that in SUPREM, we obtained the dopant profiles using our analytical model. The comparison is shown in figure 2. From figure 2 it can be seen that there is a perfect match between the analytical and SUPREM profile after the oxidation step. The profiles are also very close to each other after the inert thermal anneal.

For determining the channel profile the first case we studied was PMOS devices. Phosphorus in PMOS channel is known to display anomalous pile up behavior at Si-SiO_2 interface [3]. The pileup is a complex process, which is a combination of transient enhanced diffusion and segregation. These complex processes are difficult to simulate on commercial simulators like SUPREM™, because of the limited understanding of the underlying physical phenomenon and the difficulty in calibrating to experimental data. This pileup process causes a significant phosphorus dopant loss from the channel region. To model the anomalous phosphorus behavior we tuned the effective diffusion and segregation coefficients in our analytical model to match simultaneously the dopant profile from pulse CV and flatband voltage from standard CV. The flow chart for the tuning process is shown in figure 3. It can be seen in figure 4 that roughly for about $3L_D$ (≈300Å) from the Si-SiO_2 interface the dopant concentration information is erroneous due to Debye length limitations. The results of the simultaneous tuning of pulse CV dopant profile and standard high frequency CV curve is shown in figures 4 and 5. The phosphorus dopant profile calculated from the analytical model was then used for simulating the I-V characteristics of the PMOS device. There was an excellent match between the simulated I-V and experimental I-V curves. Similar type of analysis was done for NMOS devices. Boron in NMOS channel does not exhibit the anomalous behavior of phosphorus. The tuned boron dopant profile is shown in figure 6.

CONCLUSIONS

In this report we presented a simple analytical model for predicting the dopant profiles after oxidation and multiple thermal annealing. Our results show a good match between the dopant profiles obtained from our model and SUPREM simulations. We also developed a methodology for calibrating the analytical model using pulse CV and standard CV measurements to obtain the channel dopant profiles for both the NMOS and PMOS devices. Using this technique we were able to obtain channel dopant profiles for anomalous phosphorus behavior in PMOS devices.

APPENDIX

The expressions for N_1 and N_2 are [1]:

$$N_1 = \frac{N_{Max}\sigma}{2\sqrt{2(1+r)Dt}}\left\{\Omega(y+\alpha Y_{ox},t)+\Omega(-y-\alpha Y_{ox},t)\right\} \quad \text{(i)}$$

$$N_2 = A\, erfc\left(\frac{y+\alpha Y_{ox}}{2\sqrt{Dt}}\right) \quad \text{(ii)}$$

Where:

$$r = \frac{\sigma^2}{2Dt} \quad \text{(iii)}$$

$$\Omega(y,t) = \left[1+erf\left(\frac{ry+R_p}{\sigma\sqrt{2+2r}}\right)\right]\exp\left\{-\frac{(y-R_p)^2}{4(1+r)Dt}\right\} \quad \text{(iv)}$$

$$A = \frac{\frac{r}{(1+r)^{3/2}}\frac{R_p}{2\sigma\sqrt{2Dt}}DN_{Max}\left(\Omega(\alpha Y_{ox},t)-\Omega(-\alpha Y_{ox},t)\right)-\left\{\beta+\frac{\alpha Y_{ox}}{2(1+r)t}\right\}N_1(0,t)}{\beta erfc\left(\frac{\alpha Y_{ox}}{2\sqrt{Dt}}\right)+\frac{D}{\sqrt{\pi Dt}}\exp\left(-\frac{\alpha^2 Y_{ox}^2}{4Dt}\right)} \quad \text{(v)}$$

$$\beta = \frac{1-\alpha m}{2m}\left[\frac{k_p}{t+\frac{k_p}{4k_l^2}}\right]^{1/2} \quad \text{(vi)}$$

k_p and k_l are the parabolic and the linear oxidation rates respectively.

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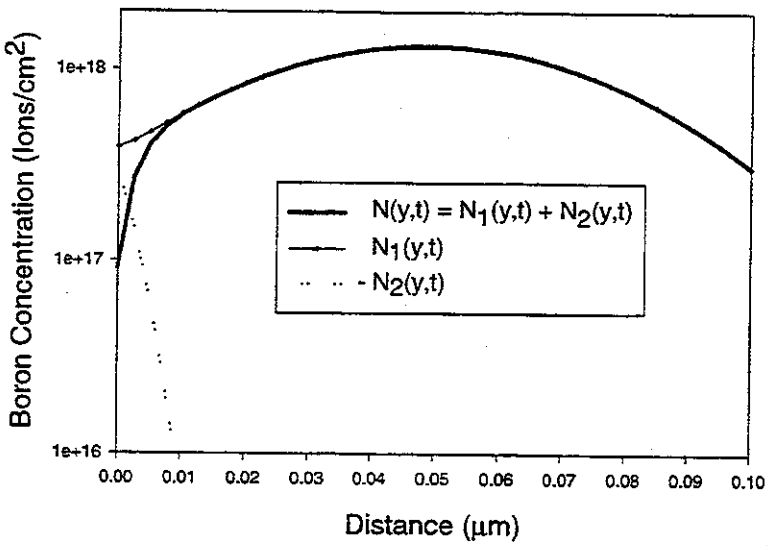

Figure 1: Components of the dopant profile after oxidation.

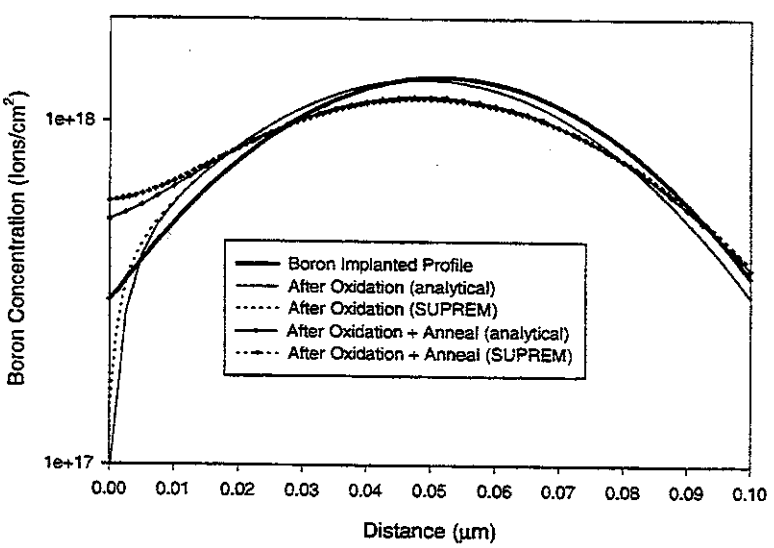

Figure 2: The comparison of our analytical model and SUPREM simulation for Boron redistribution during a multiple sequence of thermal oxidation and anneal steps.

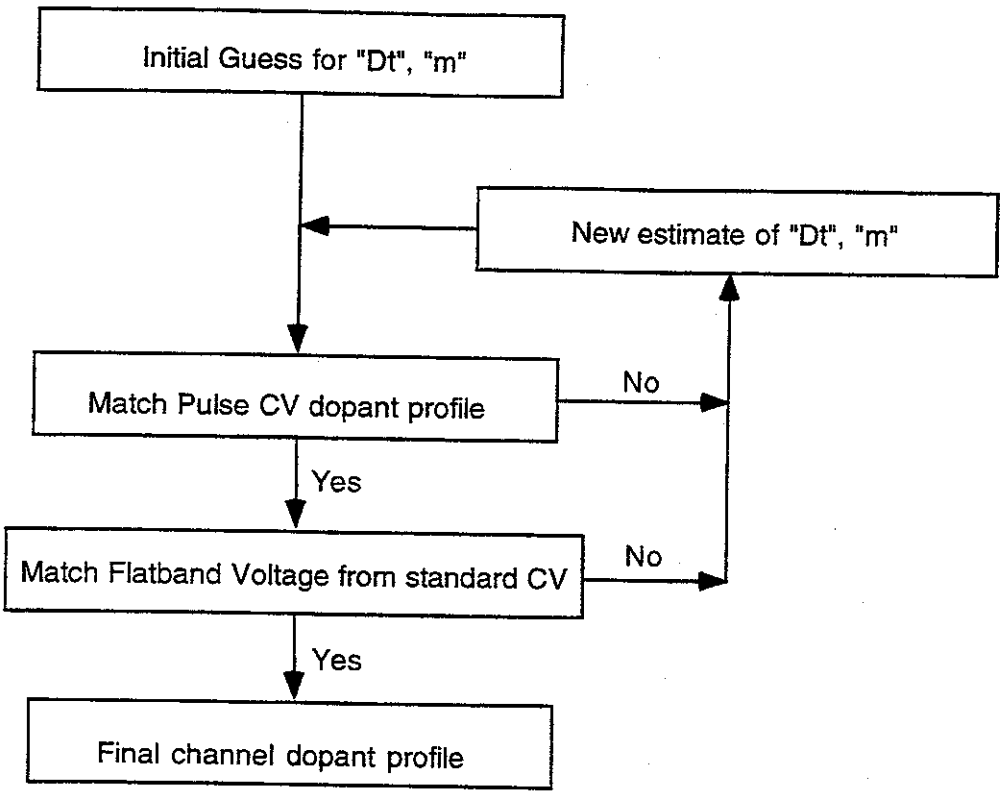

Figure 3: Flow chart for extracting the channel dopant profile from CV measurement techniques.

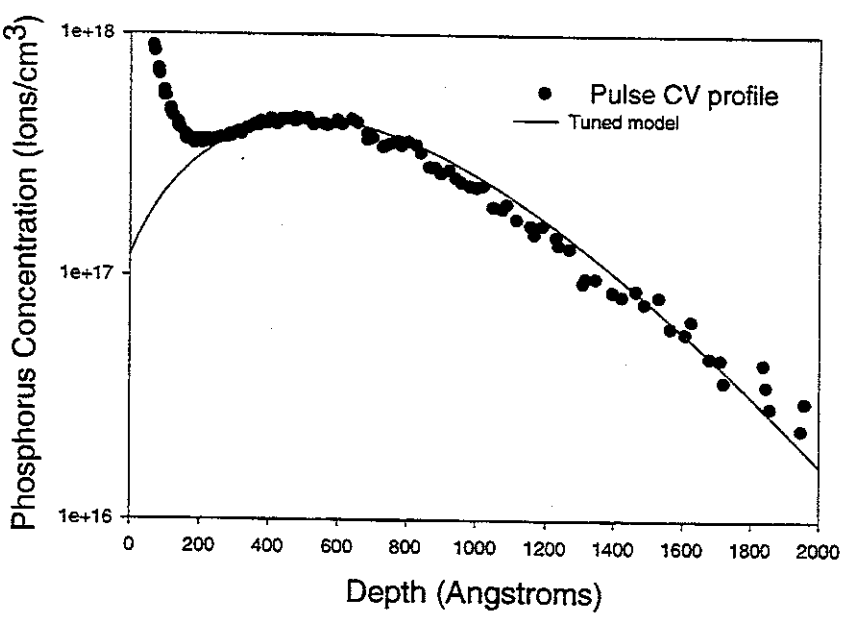

Figure 4: Comparison of tuned analytical model and dopant profile from pulse CV for channel dopant profile in PMOS devices. The pulse CV technique limitation can be seen extending about 300Å from the surface.

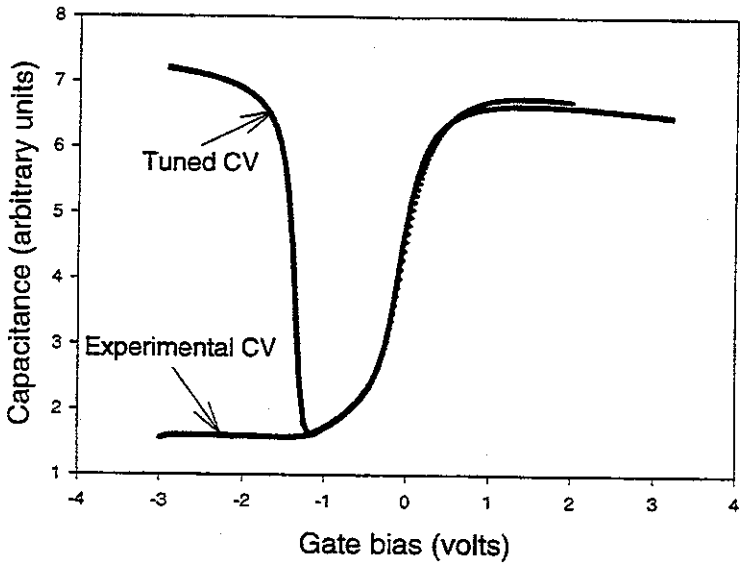

Figure 5: Comparison of tuned and experimental standard high frequency CV for PMOS with the channel dopant profile as shown in figure (3).

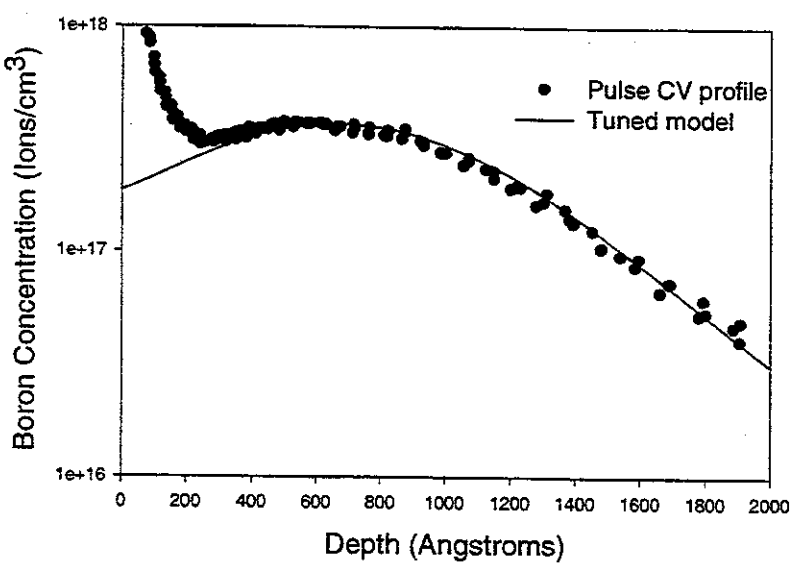

Figure 6: Comparison of tuned analytical model and dopant profile from pulse CV for channel dopant profile in NMOS devices.