Breakdown in the Output Characteristics of Deep Submicron, a-Si:H TFTs

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ABSTRACT

Purpose of this work is to investigate the breakdown in the output characteristics of short-channel (0.2–1.5 μm) amorphous silicon (a-Si:H) thin-film transistors (TFTs). Such effect which, in the case of a-Si:H devices, has been detected for the first time by some of the authors in TFTs fabricated by electron-beam lithography (EBL), is temperature-dependent besides of being field enhanced. Because of the concurrency of several field-enhanced phenomena, it was necessary to supplement the investigation with numerical simulation. Thanks to the latter it was possible to rule out Poole-Frenkel, trap-assisted tunneling, and band-to-band tunneling generation mechanisms, as well as the occurrence of punch-through, which is expected at much higher source-drain voltages than those at which the breakdown is observed. On the other hand, avalanche generation near the drain n^+-intrinsic junction cannot be ruled out, and is in fact amenable to explain the current increase at large drain voltages.

Keywords: Amorphous-silicon TFTs, impact ionization, short-channel, field-enhanced generation

Theory and implementation

In order to understand the current's features it is necessary to consider the influence of a continuous distribution of traps in the material along with a number of mechanisms for field-enhanced generation. The model details were already described elsewhere [1]–[3]. In short, the large number of traps located within the energy gap contributes to the total space charge, and this effect is accounted for by adding their contribution in Poisson's equation. Further, a generalized expression for the recombination rate is used in the continuity equations, to account for their energy-distributed nature. In particular, the energy distribution of traps is modeled by a combination of exponentials as in [4]:

$$\gamma_A(E) = \gamma_{At} \exp\left(\frac{\Delta E_C}{E_{At}}\right) + \gamma_{Ad} \exp\left(\frac{\Delta E_C}{E_{Ad}}\right) \tag{1}$$

$$\gamma_D(E) = \gamma_{Dt} \exp\left(\frac{\Delta E_V}{E_{Dt}}\right) + \gamma_{Dd} \exp\left(\frac{\Delta E_V}{E_{Dd}}\right)$$

where $\Delta E_C = E - E_C$ and $\Delta E_V = E_V - E$. The first suffix in the RHS terms refers to the acceptor/donor states, while the second refers to the *tail/deep* states.

The most important field-enhanced generation mechanisms are accounted for. The mechanisms are thermionic emission over the top of the barrier lowered by the Poole-Frenkel effect (PF), which applies to Coulombic centers [5], modeled as in [6], and thermally-assisted tunneling through the barrier, otherwise called trap assisted tunneling (TAT), which applies to both Coulombic and Dirac centers, modeled as in [7]; such effects are known to be relevant in a-Si:H because of the large concentration of traps. In order to account for PF and TAT, the SRH recombination rate was modified by redefining the emission probabilities, enhanced by a suitable multiplication factor. In addition, band-to-band tunneling (BBT) was considered, also modeled as in [7], and avalanche generation. The latter was modeled via the well-known Chynoweth expression [8]

$$\alpha_n = a_n \exp\left(-\frac{b_n}{F}\right), \qquad \alpha_p = a_p \exp\left(-\frac{b_p}{F}\right) \tag{2}$$

where F is the electric field component parallel to the current flow. The impact-ionization parameters were modified with respect to crystalline silicon, in order to account for the scattering with defects that reduces the mean free path of carriers. The above effects were implemented within the device-analysis tool HFIELDS [9]; the parameters of the trap-energy distribution are determined by fitting the turn-on characteristics of the TFT at low drain voltages; all the remaining model parameters have been taken from the literature and no fitting has been attempted.

Experimental

Inverted-staggered TFTs have been fabricated on Corning Glass 7059. First, 100 nm-thick, sputtered Cr has been photolithographically defined to form gate contacts. Together with the gates, alignment markers for the EBL have also been defined. Then, 50 nm a-SiO_2, 70 nm a-Si:H, and 30 nm n^+ a-Si:H have sequentially been deposited in a radial-flow hot-wall Plasma Enhanced

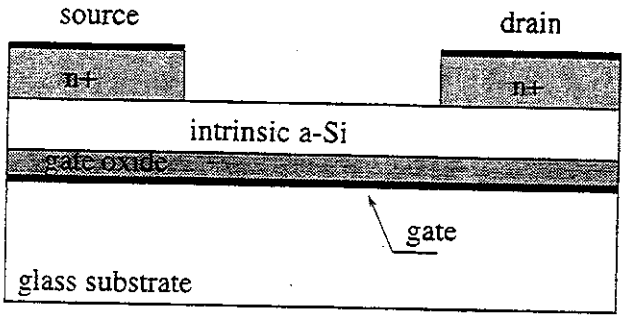

Figure 1: Schematic cross-section of the investigated device.

CVD (PECVD) reactor. The source/drain contacts (30 nm Cr followed by 200 nm Al) are 1 μm wide, and the channel length ranges between 0.2 and 1.5 μm. The electrical properties of the a-SiO_2 turn out to be similar to those of thermal-silicon dioxide, with breakdown fields exceeding 10 MV/cm and no significant charge injection up to fields of 5–6 MV/cm. A schematic cross section of the fabricated devices is shown in Fig. 1.
Electric measurements were performed on devices with different geometries (channel width equal to 25 μm and channel lengths of 0.2, 0.7 and 1.5 μm) at different temperatures, limiting the maximum applied drain-source voltage, V_{DS}, in order to avoid hot-carrier degradation during device measurements [10]. The experimental output characteristics for the 0.2 μm and the 1.5 μm device at different gate voltages are shown in Fig. 2 and 3, respectively. For large drain voltages an anomalous current increase is observed, whose edge increases as the channel length increases. Experiments also show as, in the fabricated devices, for channel lengths larger than 1.5 μm the oxide breakdown occurs before the current increase can take place. As a consequence, only in submicron devices this effect can easily be observable.

Results

The current increase at large drain bias V_{DS} is explained in terms of high-field generation mechanisms. The computed electric field within the intrinsic film at $V_{GS} = 7$ V and $V_{DS} = 13$ V (namely when breakdown occurs) is shown in Fig. 4 for the 0.2 μm device. One can see that the field peaks in the drain and source regions, in the proximity of the passivation oxide (the oxide, which is between the n^+ source and drain regions, has been removed from the plot). Simulations were performed on the 0.2 μm device in order to investigate which of

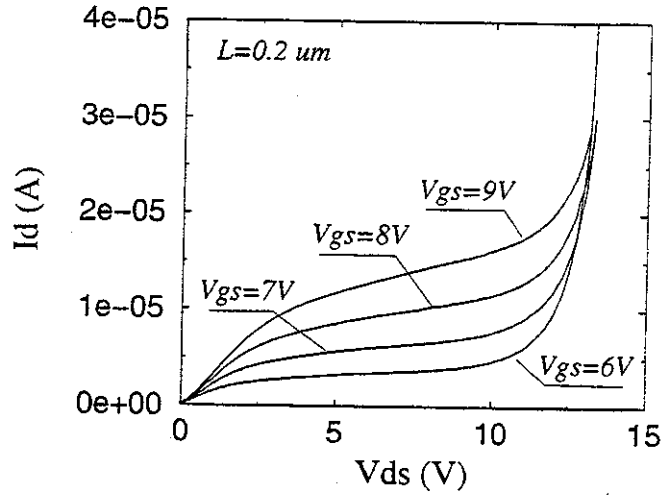

Figure 2: Measured output characteristics of the 0.2 μm channel device, at room temperature.

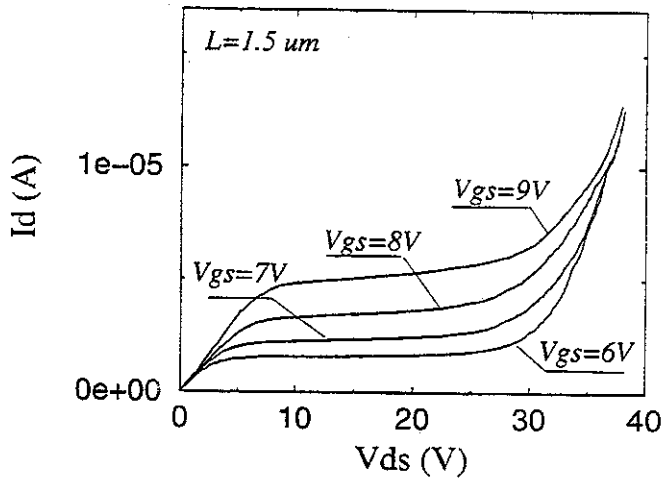

Figure 3: Measured output characteristics of the 1.5 μm channel device at room temperature.

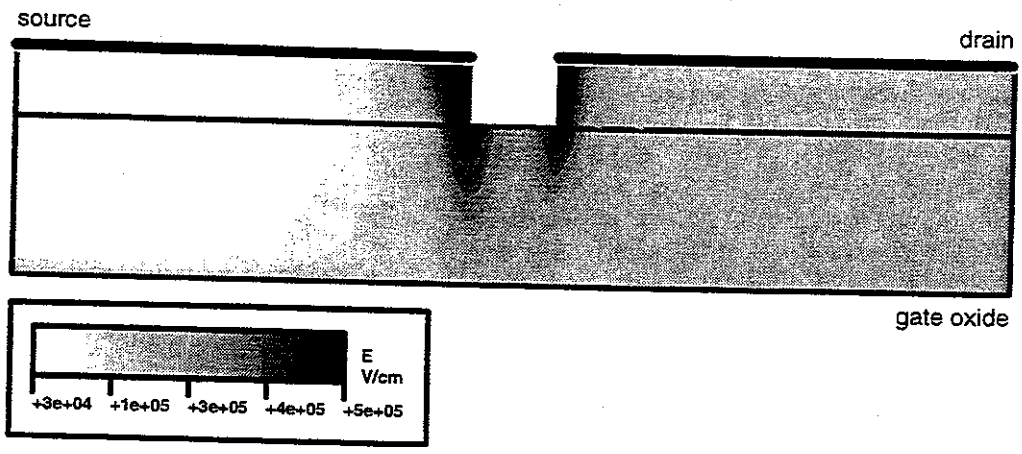

Figure 4: Distribution of the electric field within the intrinsic film, at $V_{gs} = 7$ V and $V_{ds} = 13$ V.

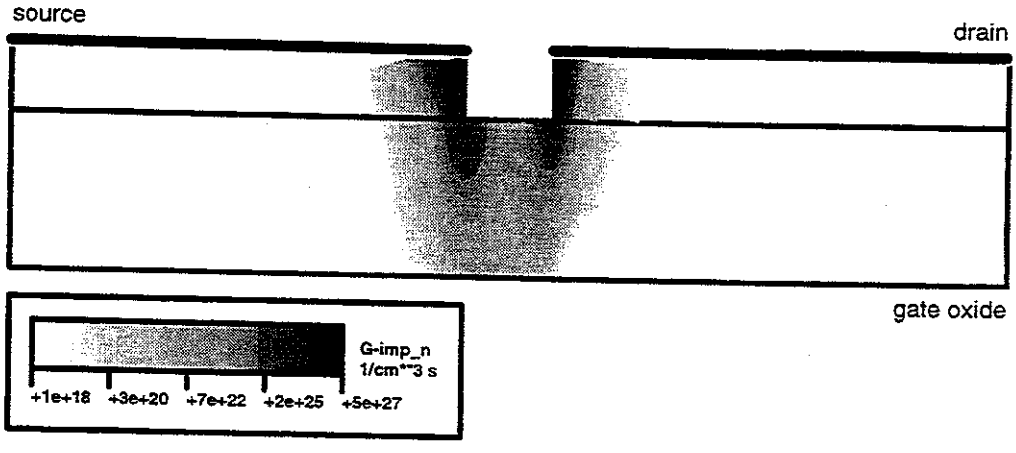

Figure 5: Electron avalanche generation rate within the intrinsic film, at $V_{gs} = 7$ V and $V_{ds} = 13$ V.

the above mentioned field-enhanced generation effects contributes to the current increase. In Fig. 5 the computed avalanche generation rate for electrons within the intrinsic film, at $V_{GS} = 7$ V and $V_{DS} = 13$ V, is shown. The generation rate peaks in the proximity of the source and drain regions, where the electric field and the current density are maximum. Fig. 6 shows the measured output current at $V_{GS} = 7$ V along with the simulated one with impact ionization turned on. As anticipated above, the parameters of the Chynoweth model were modified with respect to crystalline silicon, in order to account for the largest energy gap and for the reduced mean free path of carriers because of collisions with the large amount of defects. The parameters used in the simulations are shown in Table 1. The figure shows a fair agreement with experiments, and the breakdown is correctly reproduced. On the contrary, simulations performed with PF, TAT and BBT separately turned on (Fig. 7) do not exhibit any current increase unless a much higher V_{DS} is applied. Finally, the temperature dependence is shown in Fig. 8 (experiments and simulations); again, no parameter fitting was carried out. In contrast to the case of monocrystalline silicon [11] the dominant effect here, as temperature increases, is the large increase of free electrons due to detrapping. This reflects into a current increase with increasing temperature which, in turn, anticipates the onset of breakdown, as shown in Fig. 8.

Finally, simulations also show that the punch-through effect can be ruled out as the origin of the anomalous current increase. Simulations with all the generation effects (impact ionization, Poole-Frenkel, trap-assisted tunneling and band-to-band tunneling) do not show indeed any current increase in the output characteristics. The punch-through occurs when the drain depletion region reaches the source, thus allowing injection of the source majority carriers into the depleted channel region. In Fig. 9 the electron concentration within the intrinsic film in strong saturation ($V_{GS} = 7$ V, $V_{DS} = 13$V) is shown. One can see that still a good portion of the channel is occupied by the accumulated electrons. Hence this effect is expected to occur at much larger drain voltages than those at which the breakdown occurs.

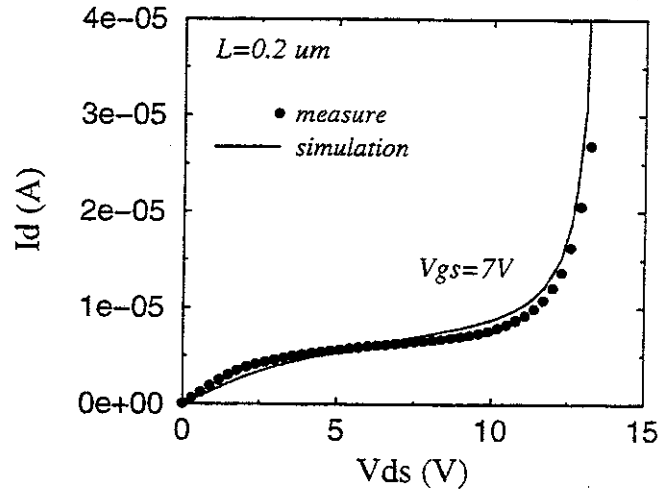

Figure 6: Measured (symbols) and simulated (line) output characteristics at $V_{gs} = 7$ V, with impact ionization turned on.

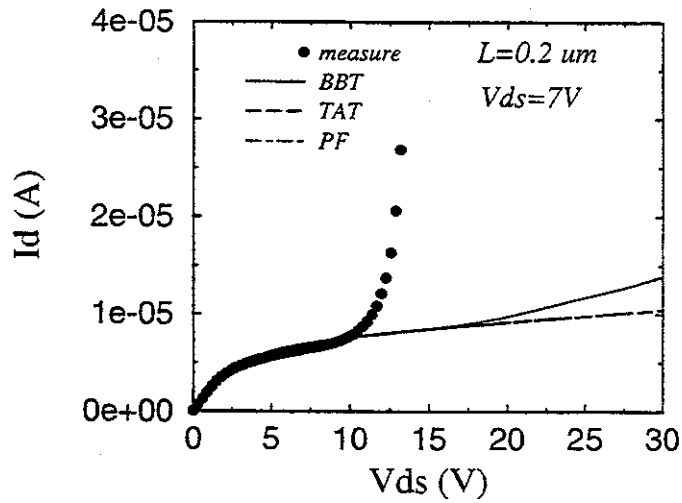

Figure 7: Measured (symbols) and simulated (lines) output characteristics at $V_{gs} = 7$ V, with BBT, TAT and PF generation effects turned on.

Conclusions

The results reported here are part of a research activity aiming at a better understanding of a class of devices that is gaining importance in the field of large-area electronic products. The breakdown in the output characteristics of deep-submicron a-Si:H TFTs was investigated here. The results show that several effects can be ruled

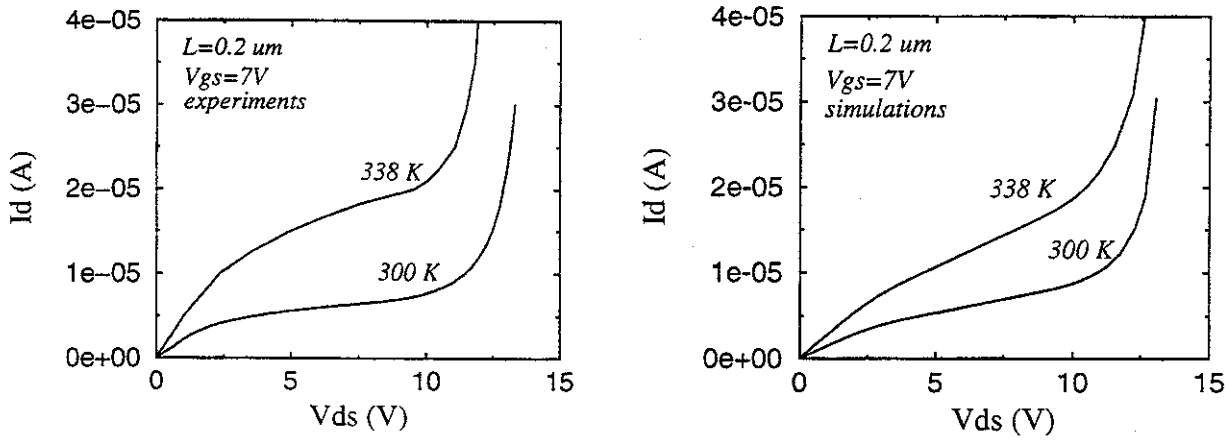

Figure 8: Measured (left) and simulated (right) output characteristics at $V_{gs} = 7$ V, $T = 300$ and $T = 338$ K.

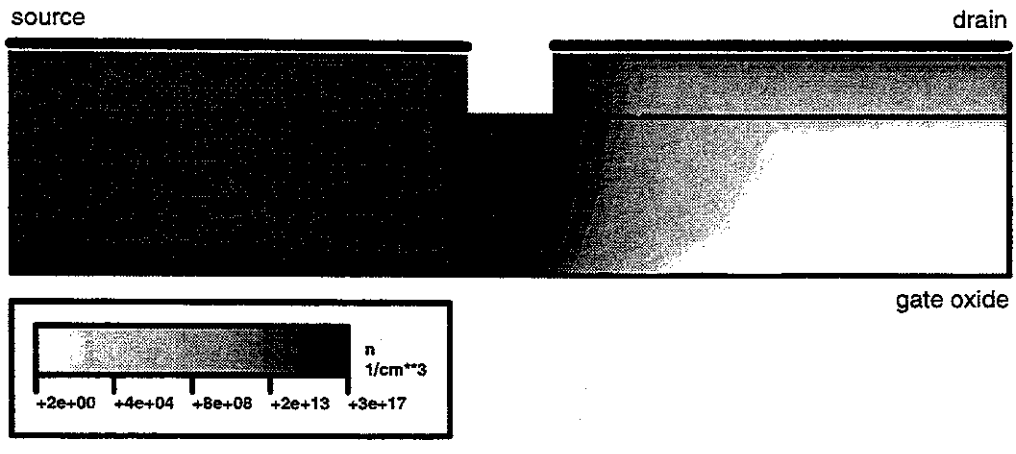

Figure 9: Distribution of the electron concentration within the intrinsic film, at $V_{gs} = 7$ V and $V_{ds} = 13$ V.

Table 1: Simulation parameters

	Value	Unit
Energy gap	1.72	eV
Electron mobility	10	$cm^2V^{-1}s^{-1}$
Hole mobility	0.5	$cm^2V^{-1}s^{-1}$
Conduction band acceptor tail states density	1×10^{22}	$cm^{-3}eV^{-1}$
Conduction band acceptor deep states density	5×10^{19}	$cm^{-3}eV^{-1}$
Acceptor tail states characteristic energy	20	meV
Acceptor deep states characteristic energy	70	meV
Valence band donor tail states density	1×10^{21}	$cm^{-3}eV^{-1}$
Valence band donor deep states density	5×10^{19}	$cm^{-3}eV^{-1}$
Donor tail states characteristic energy	30	meV
Donor deep states characteristic energy	100	meV
Acceptor (donor) states electron (hole) capture cross-section	1×10^{-17}	cm^2
Acceptor (donor) states hole (electron) capture cross-section	1×10^{-15}	cm^2
Electron i.i. coefficient	5.0×10^7	cm^{-1}
Electron i.i. characteristic field	4.0×10^6	$V\ cm^{-1}$

out as the origin of the anomalous current increase at large drain voltages, namely the Poole-Frenkel effect, the trap-assisted tunneling and the band-to-band tunneling, as well as the occurrence of punch-through. On the contrary, impact ionization occurring in the high-field region near the drain and source regions can not be ruled out. Simulations with impact-ionization turned on show indeed a fair agreement with experimental output curves. Further, the anomalous temperature dependence of the breakdown voltage, with respect to crystalline silicon, is also well reproduced.

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