Simulation of Narrow-Width Effects in Sub-Half-Micron n-MOSFETs with LOCOS Isolation

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ABSTRACT

The anomalous threshold voltage behavior of sub-half-micron LOCOS-isolated n-MOSFETs is explained by the segregation of boron and narrow-mask effect of local oxidation. A novel approach to simulating narrow-width effects is proposed. It combines 2-D process and device simulations and analytical calculations of the threshold voltage shift.

Keywords: LOCOS isolation, field oxide, narrow-width effect, boron segregation, pad oxide punchthrough.

INTRODUCTION

Threshold voltage (*Vt*) variation of narrow-channel transistors (narrow-width effect) is one of major drawbacks of sub-half-micron CMOS ULSI with LOCOS isolation. It is well known that the threshold voltage of a narrow n-channel transistor continuously increases with the channel width reduction. Isolation structure and the encroachment of the channel stop dopant are the two factors responsible for this conventional narrow-width effect for the channel wider than 1 μm [1]-[2]. However, the reduction of the device dimensions below 1 μm results in new phenomena influencing the threshold voltage. With the decrease of the channel width *Vt* slightly drops followed by its dramatic increase. This anomalous threshold voltage behavior can not be explained by the above two factors.

In this paper, we present our experimental results demonstrating the anomalous narrow-width effect in sub-half-micron LOCOS-isolated n-MOSFETs and explain this effect by the segregation of boron and narrow-mask effect of local oxidation. We also propose a method for calculating the threshold voltage of narrow transistors. This method is based on 2-D process and device simulations and analytical calculations of the threshold voltage shift.

EXPERIMENTAL

N-channel transistors with channel width varied from 20 to 0.35 μm were fabricated on 200 mm p-type silicon wafers according to the 0.35-μm CMOS technology with

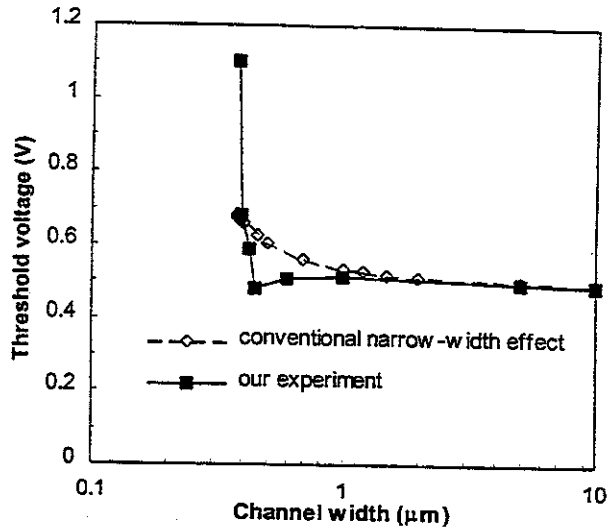

Fig.1. Experimental threshold voltage of n-channel transistors versus the channel width. Conventional narrow-width *Vt* increase is shown for comparison.

LOCOS isolation. Channel length of transistors was 10 μm in order to eliminate short channel effects. The gate oxide thickness, measured by the optical method, was 65 Å and, measured by electrical method, was 71 Å. The field oxide thickness was 4500 Å. The field oxide regions were formed by growing 200 Å pad oxide, depositing 2000 Å nitride, patterning, and further wet oxidizing at 1100 °C. The linear threshold voltage *Vt* variation was analyzed as an indicator of the narrow-width device performance deterioration. Cross-sections of the transistor and isolation structures were studied using scanning electron microscopy.

RESULTS AND DISCUSSION

Fig. 1 shows the experimentally measured threshold voltage of n-channel transistors versus the channel width (*W*). For the values of the *W* above 1 μm, *Vt* slightly increases with the *W* decrease due to the conventional narrow-width effect. However, when *W* becomes less than 1 μm, the threshold voltage demonstrates the anomalous behavior. *Vt* decreases for *W* changing from 1 to about 0.4 μm (inverse narrow-width effect) and sharply increases for *W* below 0.4 μm. The conventional narrow-channel *Vt* increase is shown in Fig. 1 for comparison.

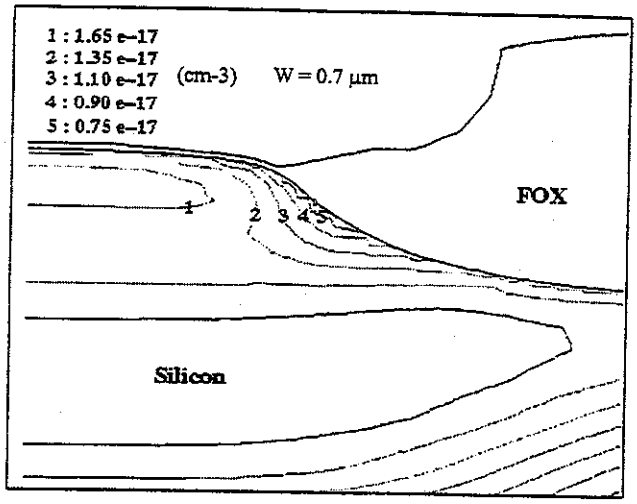

Fig. 2. Simulated final field oxide shape and boron concentration. The doping is lower under the field oxide edge.

Boron segregation

The inverse narrow-width effect, observed previously, has been explained by the segregation of boron to the field oxide [3], compressive stress in the field oxide [4], or transient enhanced diffusion [5]. To investigate the cause of the *Vt* decrease, we performed 2-D process simulations, using TSUPREM-4. The results have confirmed that the segregation of boron is the main factor responsible for the inverse narrow-width effect. The segregation reduces the average concentration of boron in the channel region, decreasing the transistor threshold voltage. This effect becomes more significant as the channel width decreases. Fig. 2 shows the simulated field oxide and active area for the transistor width of 0.7 μm. The calculated net doping levels demonstrate that the concentration of boron is lower under the edge of the field oxide and next to it than in the channel region. The following parameters of the boron segregation model were used in simulations [3]: *seg.0* = 34.7, *seg.e* = 0.66 eV.

Narrow-mask effect

However, we found it impossible to calculate the threshold voltage drop correctly accounting only for boron segregation, especially for the channel width around 0.5 μm. Also, the segregation can not explain steep *Vt* rise for *W* below 0.4 μm. Our investigations have shown that these phenomena are caused by the narrow-mask effect of local oxidation. The conventional CMOS process with LOCOS isolation comprises the following steps: pad oxide growth; silicon nitride layer deposition and patterning; thermal oxidation; nitride layer removal; oxide strip to open active regions; sacrificial oxide growth; different ion implantation

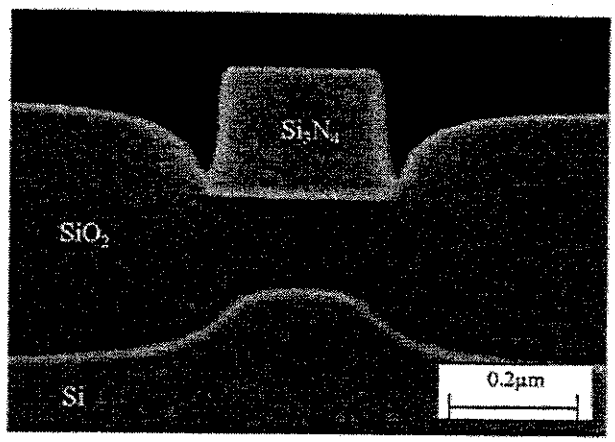

Fig. 3. SEM photograph of field oxide showing severe pad oxide punchthrough under 0.3-μm nitride mask.

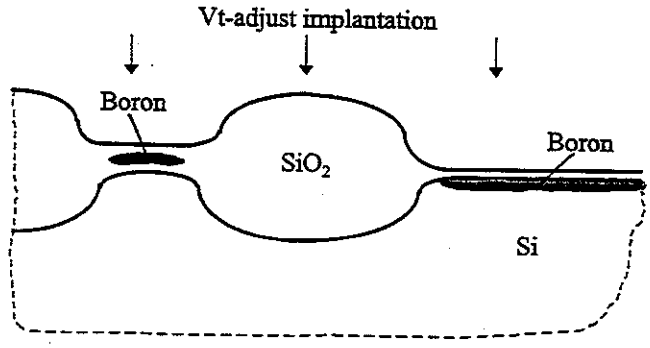

Fig. 4. Narrow-channel self-masking effect. Channel doping is lower under the punchthrough oxide.

steps to form active device elements; sacrificial oxide removal; gate oxide growth; gate formation, etc. The main drawback of LOCOS is the encroachment of the field oxide under the nitride mask during field oxidation. If the mask is narrow, the oxidation profiles from its both sides merge, and the thickness of the pad oxide under the nitride increases. This effect is known as the narrow-mask effect of local oxidation, or the pad oxide punchthrough [6]. Fig. 3 shows a SEM photograph of the field oxide with severe pad oxide punchthrough under the narrow nitride mask.

Our experimental results clearly demonstrate that if the pad oxide grows thick enough, it can not be completely etched away in the fluorine acid after the nitride removal and becomes an additional mask for the following channel implantations. Fig. 4 shows schematically this narrow-channel self-masking effect. As a result, the concentration of boron in the channel region decreases, and the transistor threshold voltage drops. However, if the resulting pre-implantation oxide layer is not totally removed before gate oxidation, the gate oxide thickness increases with the reduction of the channel width, and *Vt* rises drastically, causing transistor degradation. Fig. 5 presents the simulated

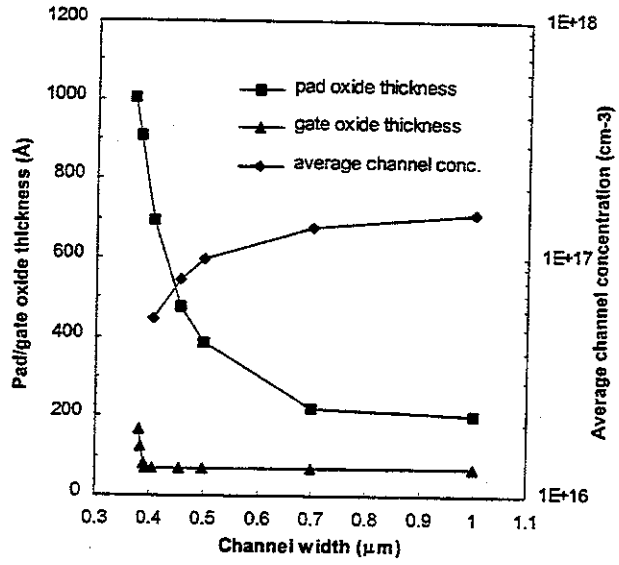

Fig. 5. Simulated pad/gate oxide thickness and average channel dopant concentration versus channel width.

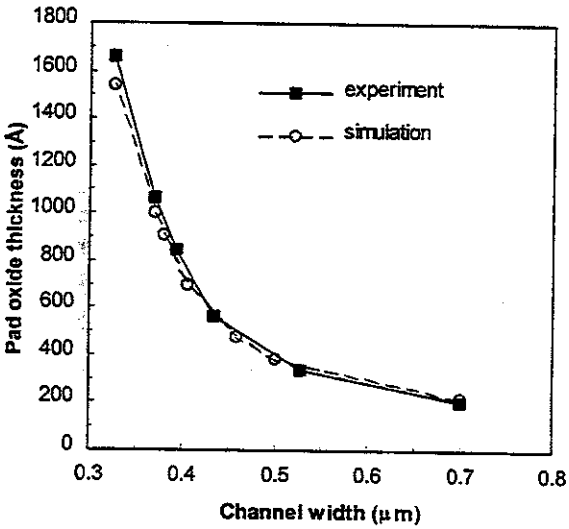

Fig.6. Comparison of experimental and simulated pad oxide thickness versus channel width.

dependence of the pad/gate oxide thickness and average channel dopant concentration on the channel width. When W changes from 1 to 0.5 μm, the average concentration slightly decreases due to the boron segregation phenomenon. If the width is less than 0.5 μm, the pad oxide punchthrough significantly reduces the concentration. For W below 0.4 μm, the gate oxide thickness increases rapidly, while the average channel dopant concentration drops gradually. This explains the dramatic rise of the threshold voltage for the channel width below 0.4 μm.

Simulation of pad oxide punchthrough

The following approach is proposed to taking into consideration the boron segregation and pad oxide punchthrough influence on the threshold voltage. The first step is the 2-D process simulation of a transistor structure across the channel. As a result, the values of the pad and gate oxide thickness are extracted, and the average dopant concentrations in the channel region, under the bird's beak, and under the field oxide are calculated.

Accurate extraction of the punchthrough oxide thickness required the calibration of stress-dependent oxidation models in TSUPREM-4. In our simulations we used the viscoelastic model. The values of low-stress oxide and nitride viscosities, the activation volumes *VC*, *VD*, *VR*, and the *VDLIM* parameter were obtained from the comparison of simulated field oxide shapes with cross-sectional SEM pictures. Fig. 6 presents the dependence of the pad oxide thickness on the channel width. The 2-D simulation matches the measured data quite well.

Calculation of threshold voltage

The next step is the simulation of a wide transistor structure along the channel for a desired channel length and calculation of the threshold voltage *Vt0*. MEDICI was used as a device simulator. The last step is the analytical calculation of the difference between the threshold voltage of a narrow and wide transistor ΔVt (the change of the transistor threshold voltage due to the narrow-width effects). We modified the approach of Akers *et al.* [1] and expressed ΔVt in terms of the gate oxide thickness and the depletion charge (average dopant concentration) under the bird's beak and the field oxide:

$$\Delta Vt = \Delta\left(2\phi_B + \frac{qt_{ox}}{\varepsilon} N_a W_{ox} + \frac{qt_{ox}}{\varepsilon W}(2aN_{th}W_{th} + bN_b(W_{ox} + W_{th}))\right)$$

where ϕ_B is the Fermi potential in the channel region, q is the electron charge, ε is the oxide dielectric constant, a is the gate overlap, b is the final bird's beak length, N_a, N_{th}, and N_b are the average dopant concentrations in the channel region, under the field oxide, and under the bird's beak, respectively, t_{ox} is the gate oxide thickness, W_{ox} and W_{th} are the values of the depletion width in the channel region [8] and under the field oxide [1], Δ refers to the difference of the corresponding expressions for the narrow and wide channel. These parameters are shown schematically in Fig. 7. We assume that the depletion width under the bird's beak changes gradually from W_{ox} to W_{th}. Since the above equation accounts for the increase of the gate oxide thickness due to the pad oxide punchthrough and the decrease of the average channel concentration due to the boron segregation to the field oxide, both conventional and submicron narrow-width effects are taken into consideration. Finally, the narrow-channel Vt is found as the sum of $Vt0$ and ΔVt.

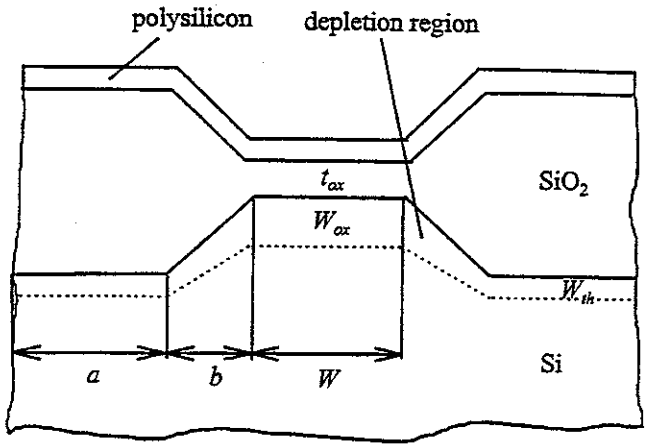

Fig. 7. Schematic width cross-section of MOSFET.

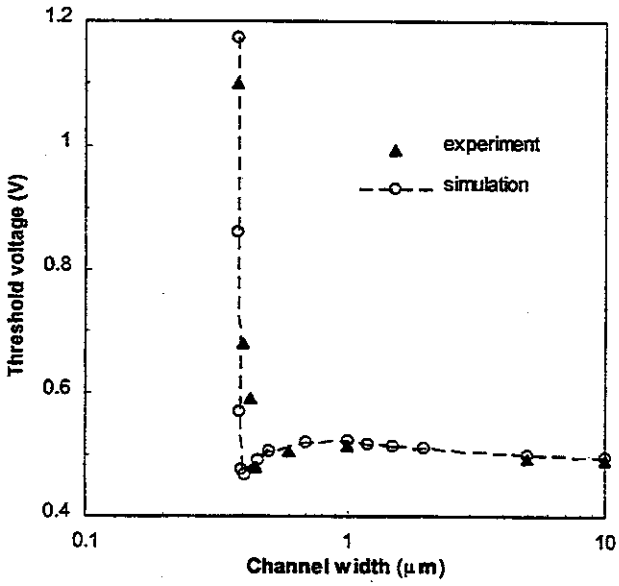

Fig. 8. Experimental and calculated values of the threshold voltage of n-MOSFET versus the channel width.

Fig. 8 shows the results of the *Vt* calculations for the n-channel transistor, compared with the experimental data. When the channel is wider than 1 μm, the conventional narrow-channel effect dominates, and *Vt* increases with the reduction of *W*. While the channel width is reduced from 1 to 0.5 μm, the decrease of boron concentration in the channel region due to the segregation compensates this increase of *Vt*. For *W* below 0.5 μm, the threshold voltage precipitously drops because of the presence of the masking punchthrough oxide layer. The increase of the gate oxide thickness for the channel narrower than 0.4 μm results in the steep *Vt* rise.

CONCLUSION

In this paper, we described the anomalous narrow-width effects in sub-half-micron LOCOS-isolated n-MOSFETs, explained these effects by the segregation of boron and narrow-mask effect of local oxidation, and proposed a novel method for their consideration. This method, based on combining 2-D process and device simulations and analytical calculations, makes it possible to calculate the threshold voltage of narrow transistors with reasonable speed and accuracy.

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