Drain and gate voltage influences on MAGFET offset and sensitivity: modeling and experiment

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ABSTRACT

In this paper both offset and absolute/relative sensitivities of MAGFET (MAGnetic Field Effect Transistor) are investigated as functions of the drain and gate voltages. Accurate physical and analytical models are developed allowing the identification of optimum operation criteria, in terms of offset reduction and/or sensitivity maximization.

Keywords: MAGFET, silicon, offset, sensitivity, analytical models

INTRODUCTION

The silicon Hall MOS magnetic sensor (MAGFET) stands as a good candidate for intelligent microsystems because of its full compatibility with IC CMOS process. Main previous studies dedicated to MAGFETs focused on the sensor design and related performances (sensitivity, noise, etc.), compared to classical Hall plates [1-3]. More recently, other works concerned the investigation of the MAGFET sensitivity in the linear and saturation regions [4-6] and the related static modeling. This paper investigates the influence and the modeling of gate and drain biases on MAGFET offset and sensitivity. A short comparison between the offset and the sensitivity of conventional Hall plates and MAGFETs fabricated with the same technology is also presented.

MAGFET PRINCIPLE AND OPERATION

The structure of the investigated Hall-type magnetic sensor (see Figure 1) is based on a conventional MOS transistor with lateral Hall contacts (p-type substrate, n-channel enhancement-mode associated MOSFET). When the inversion layer is formed it stands as a Hall plate, the main differences being that its thickness is very low (i.e. inversion channel thickness, d<50Å) and the carrier mobility is lower than in bulk silicon because of the interface defects and transverse electric field [1,6]. If the device is placed in magnetic field perpendicular to its surface, a corresponding Hall voltage, V_{Hdiff}, is sensed between the two Hall contacts:

$$V_{Hdiff} = k_g \mu_n B W E_x = \frac{k_g I B}{Q_{inv}} \qquad (1)$$

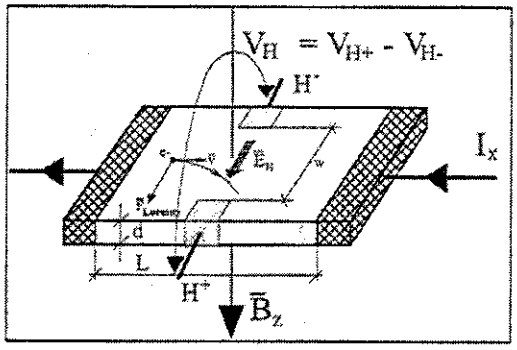
where k_g coefficient accounts for sensor geometry and carrier scattering effects, I (=I_D) is the injected current and B the magnetic induction. Taking into account that the MOS inversion channel charge, Q_{inv}, is given by:

$$Q_{inv} = -\int_0^d qn(z)dz \qquad (2)$$

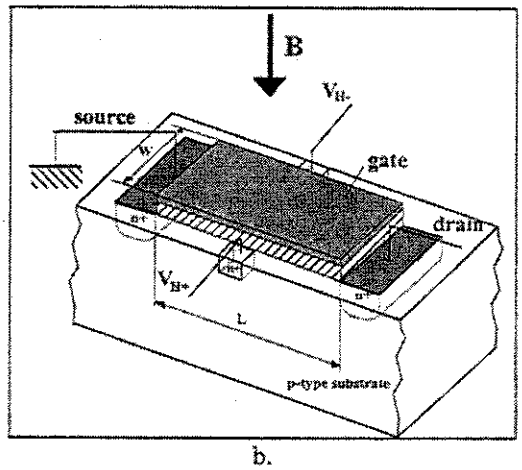
where n(z) is the channel electron concentration at coordinate z (normal to the channel surface), it is obvious that the electrical behavior of this kind of sensor is controlled by the device biases which determinate the relation between the drain current and the channel inversion charge:

$$I_D = \frac{W}{L}\mu_n C_{ox} \int_{V_D}^{V_S} \frac{Q_{inv}(V_G, V_D)}{C_{ox}} dV \qquad (3)$$

where W and L are the transistor width and length, respectively, μ_n the electron mobility in the inversion channel, C_{ox} the oxide capacitance (/surface unit) and V_S and V_D, the source and drain voltages, respectively.



a.



b.

Figure 1 a. Hall plate principle, b. Silicon MAGFET cross section and principle.

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MOSFET MODELS FOR SENSITIVITY ACCURATE EXPRESSIONS

Types of sensitivities

Sensor sensitivity is the very first parameter which characterizes the performance achieved by the sensing principle. The MAGFET absolute (S) and 'relative' (S_{VD} and S_{ID}) sensitivities are defined via the following expressions:

$$S = \partial V_{Hdiff} / \partial B \quad (4a)$$

$$S_{VD} = S / V_D \quad (4b)$$

$$S_{ID} = S / I_D \quad (4c)$$

The interest in investigating all the three types of sensitivities is related to the MAGFET specific double bias (V_G and V_D) and to the selection of the operation mode (voltage, current) according to the application type.

Linear region: unified 'ENSERG' model

An original point of this paper is that in the *linear region* the following sensitivity expressions are developed based on a recent advanced unified MOSFET model [6,7] - called the ENSERG model [8]- which stands for *weak, moderate and strong inversions* (thus allowing MAGFET accurate modeling even at low V_G). In this simple unified model, in the linear region, the drain current is expressed by:

$$I_D = \frac{W}{L}\mu_n V_D Q_{inv} = \eta \frac{kT}{q} g_0 \frac{\mu_n}{\mu_{n0}} \ln\left\{\exp\left[\frac{q(V_G - V_T)}{\eta kT}\right] + 1\right\} \quad (5)$$

where η, V_T and g_0 are model parameters [6,7], and the transverse field dependence of the carrier mobility is modeled as:

$$\frac{\mu_n}{\mu_{n0}} = \frac{1}{1 + \alpha \ln[\exp(\theta_G (V_G - V_T)/\alpha) + 1]} \quad (6)$$

where θ_G is the mobility reduction coefficient with the transverse field and α is an empirical parameter of the model. This unified model is generally valid for all V_G: weak, moderate and strong inversion. In strong inversion, the classical equations are found as a particular cases.

Taking advantage of this unified expression, the MAGFET sensitivity is calculated in all inversion regions with:

$$S = \left|\frac{\partial V_{Hdiff}}{\partial B}\right| = k_g \frac{I_D}{Q_{inv}} = k_g \frac{g_0}{C_{ox}} \frac{1}{1 + \alpha \ln[\exp(\theta_G (V_G - V_T)/\alpha) + 1]} \quad (7)$$

where $g_0 / C_{ox} = (W/L)\mu_{n0} V_D$.

It follows that, in the linear region, S decreases with V_G as the carrier mobility does. Note that the extraction of the model parameters is very simple [6]: (i) the threshold voltage, V_T, from the intercept with the horizontal axis of the linear extrapolation of the $I_D/g_m^{1/2}$ vs. V_G plot, (ii) g_0 as $2g_m(V_T)$, (iii) θ_G from the slope of $(g_0/g_m)^{1/2}$ vs. V_G plot and $\alpha = \eta.(kT/q)g_0/I_D(V_T) - 1/\ln 2$. It means that for all these parameters no information about transistor geometry and dimension is needed which is extremely useful in case of MAGFETs, for which non-conventional geometries (minimizing sensor offset) are often utilized. It is clear that, after MOSFET parameter extraction and using eq. (7) the geometric coefficient k_g can be plotted as a function of device biases. Its value at $V_G = V_T$ is given by:

$$k_g(V_G = V_T) = \frac{2S(V_G = V_T)C_{ox}(1 + \alpha \ln 2)}{g_0} \quad (8)$$

Typical simulation plots of the normalized MAGFET sensitivity, $S_{norm} = S/(k_g g_0/C_{ox})$, based on eq. (7) and illustrating the absolute sensitivity decrease with the gate voltage in the linear region, are given in Figure 2. This results are in good agreement with other previous reported measurements and calculations of S [3].

Similarly, using equations (4b), (4c), (5) and (6), the expressions of S_{ID} and S_{VD} sensitivities can be deduced.

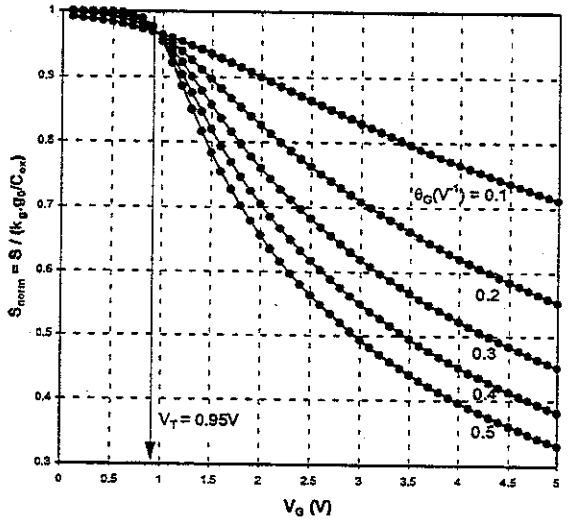

Figure 2 Simulation of the normalized MAGFET absolute sensitivity, S_{norm}, as a function of the gate voltage, V_G, according to eq. (7), with α=0.05.

Saturation region: 'conventional' model

The saturation region is investigated in this paper using the conventional modeling of the drain current, in strong inversion ($V_G > V_T, V_D > V_{Dsat} \cong V_G - V_T$)):

$$I_D \cong \frac{1}{2}\frac{W}{L}\frac{\mu_{n0}}{1 + \theta_G(V_G - V_T) + \theta_D V_{Dsat}} C_{ox}(V_G - V_T)^2 \quad (9)$$

where θ_D is the reduction coefficient of the mobility with the longitudinal field and V_{Dsat} is the saturation voltage. A unified detailed investigation of the saturation region can be performed with the 'EKV' model [9]. For simplicity, we present here a conventional analysis based on eq. (9). Using

eqs. (9), (1), (4a), (4b) and (4c), the following simple analytical expressions corresponding to the absolute and the relative sensitivities are deduced for Hall contacts placed in the first half of the channel (source side):

$$S = \frac{k_g}{2}\frac{W}{L}\frac{\mu_{n0}(V_G - V_T)}{1+\theta_G(V_G - V_T)+\theta_D V_{Dsat}} \quad (10)$$

$$S_{VD} = \frac{k_g}{2}\frac{W}{L}\frac{\mu_{n0}}{1+\theta_G(V_G - V_T)+\theta_D V_{Dsat}}\frac{V_G - V_T}{V_D} \quad (11)$$

$$S_{ID} = \frac{k_g}{C_{ox}}\frac{1}{V_G - V_T} \quad (12)$$

where all model parameters are already specified.

Note that since these model parameters can be extracted directly from the transistor output characteristics, I_D-V_D, possibly combined with the analysis of I_D-V_G curves, the evolution of the geometric coefficient, k_g, with gate and drain biases can be deduced.

EXPERIMENT

Sensitivity

CMOS MAGFETs with geometries which minimize sensor offset were characterized using a HP4155A parameter analyzer (1μV resolution in V_{Hdiff} measurement). Fig. 3 presents typical dependencies of Hall voltages, V_{Hdiff} as functions of V_D with V_G as a parameter, for different magnetic fields (up to 400mT). The calculated sensitivities using definitions (4a), (4b) and (4c) are presented in Fig. 4. It appears that the proposed analytical modeling of MAGFET sensitivity is well validated by the experiment (note that in these figures all data are in strong inversion):

- in the linear region (*low V_D*):

(i) S increases linearly with V_D (g_0 in eq. (7) is a linear function of V_D) and is slightly lower for V_G=5V compared to V_G=2.5V (as predicted by equation (7), in terms of V_G influence),
(ii) S_{VD} is slightly higher for V_G=2.5V compared to 5V because the transverse electric field is lower (i.e. the channel electron mobility is higher),
(iii) S_{ID} depends on V_G as: $k_g/Q_{inv} \sim k_g/(V_G - V_T)$, the dependence on the transverse field being canceled. The linear increase of S_{ID} with V_D (~30%) can be related to an equivalent increase of k_g (Hall angle 'rotation' increases with V_D).

- in the saturation region ($V_D > V_{Dsat}$):

(i) S appears to be not dependent on V_D, like eq. (10) shows. Its dependence on (V_G-V_T) is also well verified,
(ii) S_{VD} well tracks eq. (11) in terms of both V_D and V_G,
(iii) As eq. (12) predicts, S_{ID} is not dependent on V_D and is proportional to $1/(V_G - V_T)$: nearly 3 times higher in case of V_G=2.5V compared to 5V (according to V_T=0.95V).

The previous simple analysis, based on analytical models validated by experiment, shows that, in case of strong inversion (i.e. $V_G > V_T$), the maximum of MAGFET sensitivity can be obtained:
(i) for S - in *saturation for maximum V_G and V_D* (both 5V in Fig. 4),
(ii) for S_{VD} - in the *linear region for low V_G*, and
(iii) for S_{ID} - in *saturation for low V_G*.

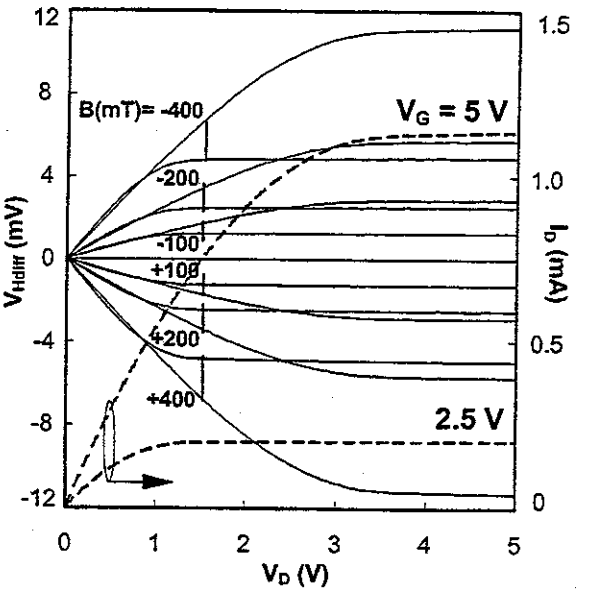

Figure 3 Hall voltage, V_{Hdiff}, and drain current, I_D (doted line), against the drain voltage V_D with the gate voltage, V_G, as a parameter, for different magnetic fields, B (data measured at room temperature).

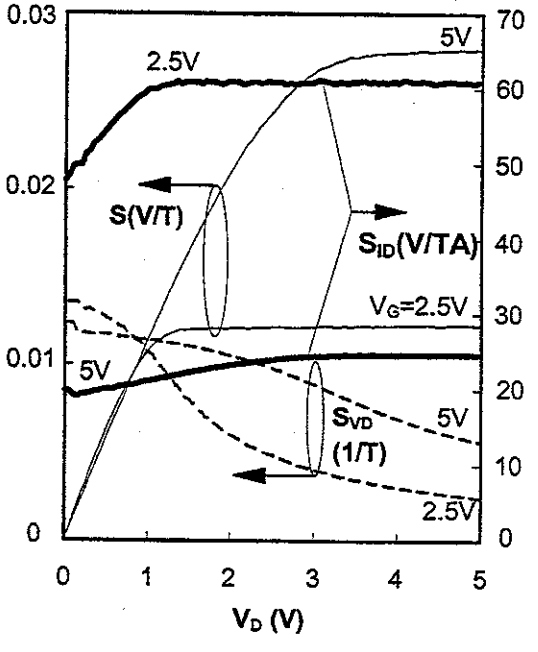

Figure 4 MAGFET absolute and relative sensitivities: S, S_{VD}, S_{ID}, against the drain voltage, V_D, with the gate voltage, V_G, as a parameter, calculated with experimental data from Figure 3 (the transistor threshold voltage is V_T=0.95V).

Offset

Offset stands as an important sensor performance parameter illustrating the non-ideally of a given fabricated geometry. A large number of design techniques are now available in order to reduce Hall sensor offsets. It is well known that Hall plate and MAGFET offsets are usually related to the device geometry and to the inherent non-alignment between the lateral Hall contacts ('R_{off} effect'). In the following, it will be shown that in case of silicon MAGFET, the gate and drain biases can influence substantially the offset amplitude.

In Figs. 5 and 6 are illustrated typical dependencies of the offset voltage (i.e. $V_{off}=V_{Hdiff}(B=0)$) on drain and gate voltages, in linear and saturation regions.

First, note that, in strong inversion and linear region of operation (low V_D), the offset remains proportional to the drain voltage, V_D (see Fig. 5 and Fig. 6).

Systematic measurements show that offset curves look like the output MOSFET I_D-V_D characteristics, (see Figure 5) with the main difference that in the linear region (i.e. low V_D), the V_G influence seems to be canceled. This result is confirmed by Fig. 6 where V_{off} is plotted as a function of V_G together with the drain current and transconductance ($g_m=dI_D/dV_G|_{VD=const}$): below threshold, V_{off} rises with V_G and, in strong inversion, V_{off} increases very slightly with V_G. For low positive values of V_G (i.e. weak inversion or depletion) the offset voltage is high (as shown in Fig. 6) because of the low conductivity of the inversion channel (not yet 'formed').

In order to explain the offset dependence on V_G, in the linear region, correlations with different MOS electrical parameters are analyzed. The correlation plot between the MAGFET transresistance, $R_m=1/g_m$, shows that, on the contrary to [5], there is no clear linear correlation region (see inset Fig. 7) between this parameter and the offset voltage. Another possible explanation of the offset behavior in the linear region (weak, moderate and strong inversions) is that there is an offset contribution which mirrors the value of the Si/SiO_2 surface potential, ψ_S, which strongly depends on V_G in weak and moderate inversion and is pinned up near $2\phi_F$ in strong inversion along the channel, according to [10]:

$$V_G = \psi_S + \frac{\sqrt{2\varepsilon_{Si} q N_A}}{C_{ox}} \sqrt{\psi_S + \frac{kT}{q} e^{\frac{\psi_s - 2\phi_F}{(kT/q)}}} \qquad (13)$$

where N_A is the substrate doping, ε_{Si} is the silicon permittivity and ϕ_F is the Fermi potential. This late influence (surface potential) can dominate near threshold the current one, associated with the offset contribution due to contact non-alignment (R_{off}). Fig. 8 presents typical plots of the MOS surface potential as a function of the gate voltage, in the linear region of operation (low V_D), based on eq. (13). It is clear that near threshold ($0.75V<V_G<1.3V$) the offset dependence on V_G looks like the surface potential one. Further interesting application of this remark could concern the extraction of the threshold voltage of the associated MOSFET based on offset measurement and on the most 'physical' definition of V_T (i.e. $V_T=V_G(\psi_S=2\phi_F)$).

It is obvious that the offset dependence on the gate voltage changes in saturation (increased drain voltage), where ψ_S depends both on V_G and on the position along the inversion channel ('x' axis). In this case, the much higher value of the drain current can make the contact misalignment to be the dominant contribution in the offset voltage.

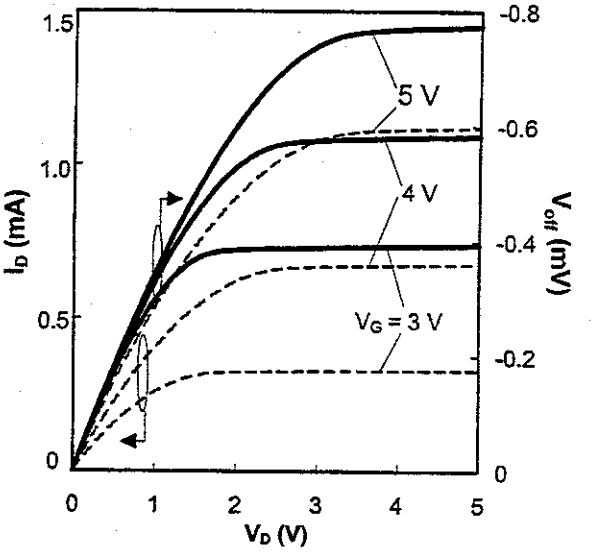

Figure 5 Offset voltage, V_{off}, and drain current, I_D (doted line), versus drain voltage, V_D, with V_G voltage as a parameter, for a silicon n-channel MAGFET.

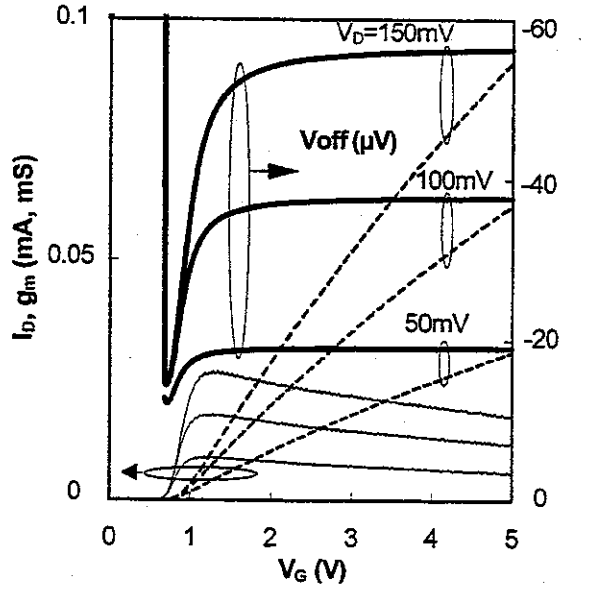

Figure 6 Offset voltage, V_{off} (thick line), drain current, I_D (doted line), and transconductance, g_m (thin line), versus gate voltage, V_G, with drain voltage, V_D, as a parameter (same device as in Figures 3 and 5).

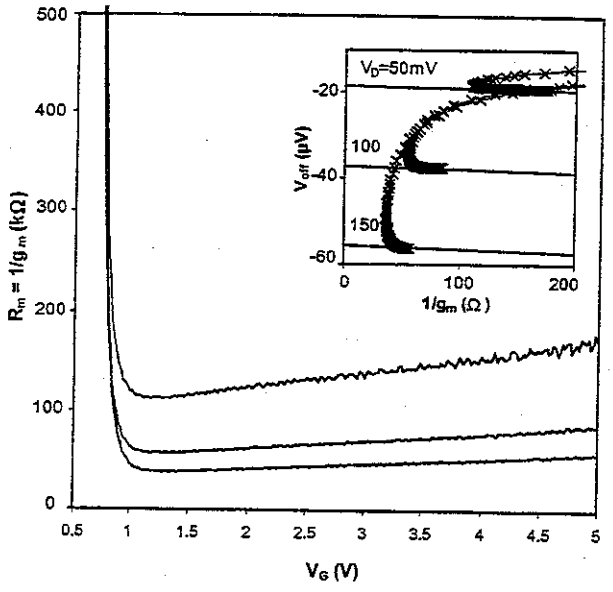

Figure 7 Transresistance, $R_m=1/g_m$ versus gate voltage, V_G and (inset) correlation between offset voltage, V_{off}, and R_m, corresponding to characteristics given in Fig. 6.

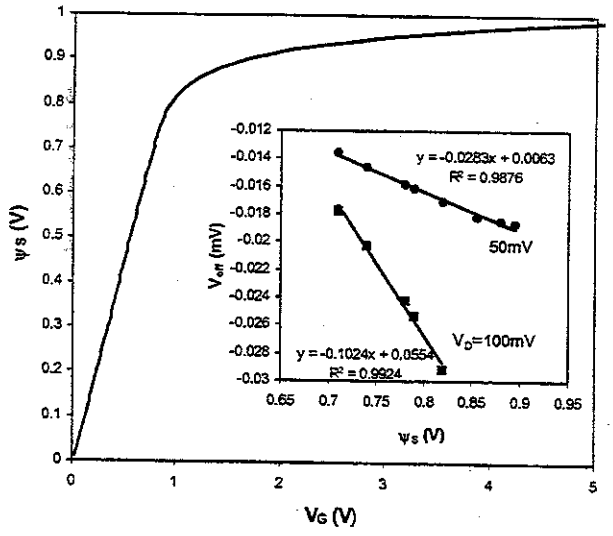

Figure 8 Surface potential, ψ_S, as function of gate voltage, V_G according to conventional analytical modeling, eq. (13) and (inset) experimental correlation between V_{off} and calculated ψ_S.

COMPARISON BETWEEN MAGFET AND CONVENTIONAL HALL PLATES

Conventional Hall plates (Fig. 9) with various geometries have been fabricated on the same wafer using the same CMOS technology as for the previously investigated MAGFETs.

Table 1 presents a short comparison between few parameters of typical Hall plate sensors and the MAGFET ones. It is clear that, in terms of offset voltage and absolute/relative sensitivity, the MAGFET solution can easily compete (if optimal gate and drain biases are selected, based on the presented analysis) with the conventional Hall plate. As already mentioned in other previous works [1,3], the main drawback of MAGFETs, compared to Hall plates, remains its higher noise. Typically, the noise spectral power density, S_{VH}, corresponding to our silicon MAGFETs has been found to be 5 to 10 times higher compared to Hall plates operated in similar bias conditions.

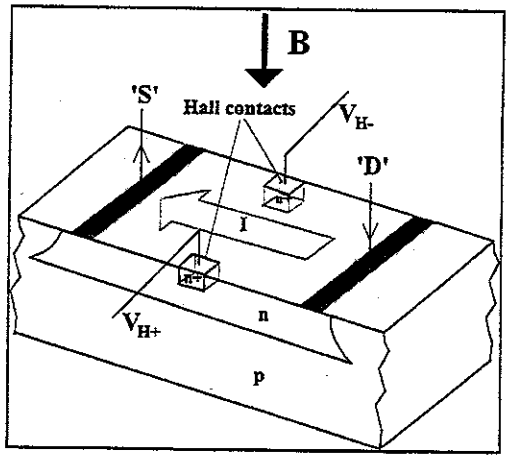

Figure 9 Schematics of a conventional silicon Hall plate placed in a magnetic normal field, B ('S' and 'D' are the contacts equivalent to MAGFET source and drain).

Table 1 Comparison between silicon MAGFET and Hall plate typical electrical parameters, measured at room temperature

Parameter	MAGFET	Hall plate
V_{off}(μV) V_D=5V	780 (V_G=5V)	160
I_D(mA) V_D=5V	1.18 (V_G=5V)	3.88
V_{Hdiff}-V_{off}(mV) B=500mT	14.8 (V_G=5V)	96
$S_I=(V_{Hdiff}-V_{off})/BI_D$ (mV/TmA) V_D=5V,B=500mT	25 (V_G=5V)	49.4
$R=V_D/I_D$(kΩ) (V_D=2.5V)	2.5 (V_G=5V)	1.28
$(S_{VH})^{1/2}$ (nV/Hz$^{1/2}$) V_D=2.5V, f=1kHz	14 (V_G=5V)	6

CONCLUSION

A thorough physical and experimental study with an analytical modeling of MAGFET offset and sensitivities as functions of device biases (gate and drain voltages), in the linear region of operation as well as in saturation, is presented. It is shown how drain current unified models allow the extension of the modeling from strong inversion to moderate and weak inversions.

Operation in saturation with maximum allowed gate and drain voltages maximizes the S and S_{ID} MAGFET sensitivities. Contrarily, in order to maximize S_{VD}, the linear region (a low drain voltage) combined with a low gate voltage is required.

It is found that in the offset dependence on the gate voltage there is a contribution which is not due to the R_{off} effect and which probably mirrors the value of the surface potential.

The main impact of this study is on the simulation and the optimal operation conditions for MOSFET-based Hall silicon sensors.

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