A Floating Random-Walk Method for Efficient RC Extraction of Complex IC-Interconnect Structures

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ABSTRACT

The floating random-walk method has been used to efficiently extract interconnect capacitance in complex, multilevel integrated circuits. We present here an overview of the floating random-walk method in the context of capacitance extraction. The method implements a series of 3D random walks to statistically estimate elements of the capacitance matrix. Because the floating random-walk method requires no numerical mesh, excellent computational efficiency is achieved. The method is well suited for parallel implementation in possible full-chip applications. We describe, as well, a related methodology for extracting *RC*-interconnect parameters. Our methodology consists of conversion of the IC layout data into 3D structures, recognition of interconnects and devices, identification of interconnects requiring *RC* modeling, creation and simplification of *RC* models, and generation of a interconnect netlist.

Keywords: capacitance extraction, floating random-walk method, network reduction, *RC* extraction.

INTRODUCTION

The floating random-walk method has been used to accurately and efficiently extract capacitance of complex 3D interconnects for digital ICs [1–3]. This meshless, stochastic numerical method has proven itself a worthy alternative to deterministic finite-element, boundary-integral, and spectral methods. The random-walk method may also prove useful in application areas requiring solution of 3D linear partial-differential equations with complicated problem geometry. Ideal application areas include: (1) heat conduction, electrostatics, and magnetostatics (Laplace equation); (2) time-harmonic electromagnetics (Helmholtz equation); and (3) mechanical deformation (linear elasticity equations).

We present here an overview of the floating random-walk method for IC interconnect-capacitance extraction. We present, as well, a related methodology for extracting and reducing distributed *RC* models for distributed interconnect parasitics. Our focus is the analysis of complex, 3D IC-interconnect structures.

FLOATING RANDOM-WALK METHOD

The floating random-walk method can be used to evaluate an integral representation of capacitance with no numerical discretization error. Its performance characteristics are quite different from those of other extractors.

Theory

Our floating random-walk method is based on the solution of Laplace's equation for a scaleable cube domain, over which are applied arbitrary Dirichlet conditions. A resulting boundary-integral solution permits us to compute electric potential and electric field at the cube center. Nesting these boundary integrals yields complete integral expressions for capacitance-matrix elements as a function of the full 3D IC-interconnect geometry. Monte Carlo evaluation of these integrals defines the floating random-walk method.

To find, for example, the capacitance C_{AB} between two of several electrical conductors, we evaluate by Monte Carlo integration the following surface integrals that combine to form an infinitely deep nested-integral expression for capacitance:

$$C_{AB} = \oint\!\!\oint d^2 r_1 \; \varepsilon(r_1) E(r_1) \Big/ V_B,$$
$$E(r_1) = \oint\!\!\oint d^2 r_2 \, f(r_2 - r_1) V(r_2),$$
$$V(r_k) = \oint\!\!\oint d^2 r_{k+1} \, g(r_{k+1} - r_k) V(r_{k+1}), \; k=2,3,\ldots \tag{1}$$

Here, E is the component of electric field normal to the surface of integration for the conductor of interest; and, f and g are known functions, independent of conductor geometry. The domain of the integral for C_{AB} is a surface enclosing conductor A. The domain of the integral for $E(r_1)$ is a surface enclosing r_1 and containing no electrodes. The domain of the integral for $V(r_k)$ is a surface enclosing r_k and containing no electrodes as well. When r_k is on the surface of an electrode, however, $V(r_k)$ is either V_B (on electrode B) or 0 (on any other electrode). Because Eq. (1) contains no approximations, the principal source of computational error associated with Monte Carlo integration of Eqs. (1) is statistical sampling error.

Each random walk begins on an integration surface enclosing the conductor from which coupling capacitance is to be determined. A walk consists of a series of steps onto maximal cube boundaries, as shown in Fig. 1. A walk terminates upon encountering a conductor. The statistical estimate for capacitance between electrode A and B in this example is a single mathematical weight factor consistent with Eqs. (1). The series of points associated with a single Monte Carlo estimate of the capacitance integral can be described as a floating random walk—floating, because the size of a walk step is limited only by the distance to the nearest conductor. To obtain an accurate estimate for this capacitance, weight factors are averaged over a series of walks. The statistical error in this estimate decreases as $1/\sqrt{N_w}$, where N_w is the number of walks.

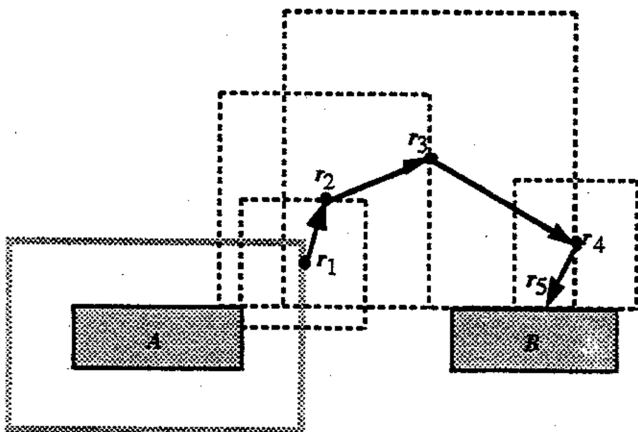

Fig. 1. Sample random walk starting on an integration surface around conductor A and terminating on a conductor B.

Performance

The computational performance of this floating random-walk method is markedly different from other types of physically based extractors relying on conventional finite-element analysis [3]:

- No numerical mesh is required, so memory requirements are low, allowing analysis of large layouts.
- Computational error of a given interconnect structure depends on run time, only.
- The convergence time for self-capacitance depends *weakly* on the size and number of conductors.
- Due to statistical error cancellation, values of small coupling capacitors need not be found very accurately. No individual small capacitor will have a significant effect. A significant capacitance consisting of a combination of small coupling capacitors, however, will have an improved accuracy due to statistical error cancellation.
- The random-walk method is readily parallelizable because of the statistical independence of individual walks. Dramatic computational acceleration is achievable in massively parallel-processor (MPP) or network-of-workstation (NOW) implementations. Since little inter-processor communication is required, we expect nearly 100% efficiency with respect to speed improvement for perhaps as many as thousands parallel computational nodes.

RC EXTRACTION

To extract RC interconnect data from 2D IC layout information, our steps include: (1) conversion of the layout to 3D structures, (2) recognition of interconnects and devices, (3) identification of interconnects requiring RC modeling, (4) creation and simplification of RC representations of interconnects, and (5) generation of a netlist, an electrical description of the layout.

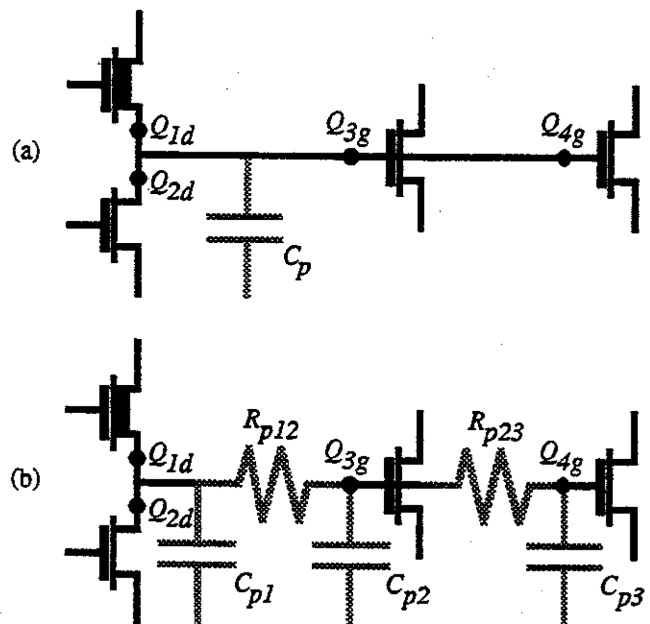

Fig. 2. (a) Modeling an interconnect as a parasitic capacitance involves the addition of a capacitor (gray) to the netlist, but does not affect relationships between pins (Q_{1d}, etc.) on the interconnect. (b) RC modeling requires that the netlist be regenerated—resistors added between devices affect relationships between pins.

Generating an RC model of an interconnect is complicated by the requirement that the resulting model must itself be incorporated into a netlist representing the entire circuit. As shown in Fig. 2, adding a parasitic capacitor to the model of an otherwise ideal interconnect can be performed

without consideration of pins (device terminals). However, adding a parasitic resistor to the model will change the relationship between pins that were formerly shorted together by a conductor considered ideal.

Geometry Input

Our first step in *RC* modeling is to identify interconnects and device pins from 2D layout data while generating a 3D representation. This can involve several operations, some of which are shown in Fig. 3. Pin recognition, especially, can be complex, depending on whether pins are defined by device geometry (a MOSFET) or by layout hierarchy (a macro cell).

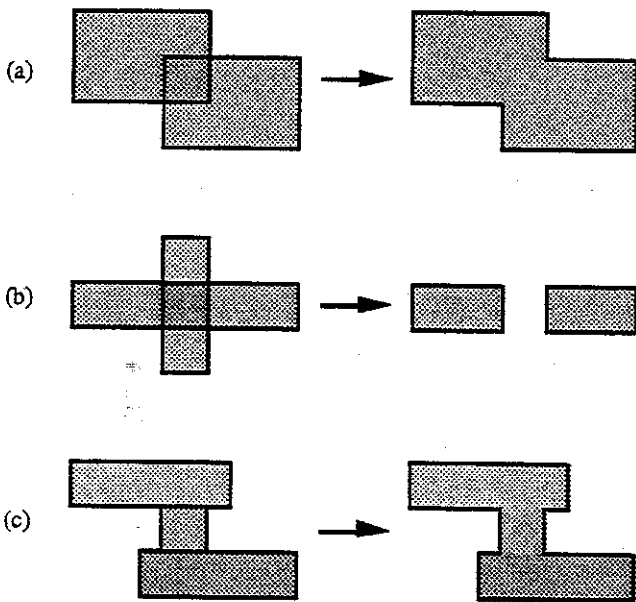

Fig. 3. Some operations required to convert 2D layout data to a 3D representation: (a) simplification of polygons on a layer; (b) derivation of layers; (c) side view showing a via connecting two interconnect layers.

RC-Critical Interconnects

In typical designs, only a small fraction of the interconnects will be "*RC* critical", requiring an *RC* representation. We use some simple, approximate formulas for resistance, capacitance, and delay time to distinguish between less important interconnects in a design and *RC*-critical interconnects. We control *RC* model generation and network simplification with a user-defined *RC* resolution parameter τ_{err} (units of time). Each node in the final network must have an accumulated "time" error of no more than τ_{err}.

When available, the resistance of drivers (output pins) and the capacitance of both receivers (input pins) and drivers are included in the *RC*-interconnect model. This information, along with an estimate of the total interconnect capacitance C_{est} and an upper limit to the resistance R_{max} of the interconnect, establishes an upper limit to the delay time. LPE (layout-parameter extraction) values for C_{est} and R_{max} are found by summing the capacitance and resistance contribution of each element of an interconnect. These contributions are determined with user-supplied layout-parameter coefficients. R_{max} is usually overestimated in our procedure, though it will be reasonably accurate for interconnects containing a driver at one end, a single current path, and a receiver at the other end. C_{est}, R_{max}, driver resistance, and pin capacitance determine a worst-case Elmore[4] delay time τ_{max} for a particular interconnect. If τ_{max} is less than τ_{err}, the interconnect may be modeled as an ideal conductor, possibly with a single lumped parasitic capacitance.

For present-day high-end digital chip designs with reasonable values of τ_{err}, only a small fraction of interconnect interconnects are expected to have τ_{max} values necessitating *RC* modeling.

RC Network Reduction

For *RC*-critical interconnects, a detailed *RC* network representation is generated based on user-supplied LPE coefficients. The network includes connections to pins on the interconnect. The network is then reduced by various transformations that generally preserve resistance, capacitance, and Elmore delay time in *RC* trees. Figure 4 shows two such transformations: π–T and T–π. Second-order effects are controlled by user-defined parameters. When a transformation eliminates a node containing a pin, the pin is moved to a nearby node as long as the accumulated Elmore-time error is less than the user-defined parameter τ_{err}. Thus, two pins with Elmore delay times within $2\tau_{err}$ of each other may reduce to a single node. We recognize that LPE capacitance estimates are generally inaccurate. However, these estimates do not play a significant role in the structure of the simplified *RC* network.

With respect to Elmore delay time in an *RC* tree, equivalence of the two structures in Fig. 4 is easily shown. The contribution of a capacitor of value C to the Elmore delay time in an *RC* tree is $R_{uphill}C$, where R_{uphill} is an "uphill" resistance, resistance between the capacitor and the driver. Since the resistance of the two structures in Fig. 4 is identical, the resistance between any pair of external nodes is unchanged, so the contribution of any external capacitor to the Elmore delay time is unaffected. For the internal capacitor(s), "uphill" is either to the left or to the right. When the driver is to the left, the contribution of the internal capacitors to the Elmore delay time is $(R_{uphill}+R_1)C_{12}$ in either structure. (R_{uphill}, here, is the uphill resistance from the node *nearest* the driver.) When the driver is to the right, the contribution of the internal capacitors to the Elmore delay time is $(R_{uphill}+R_2)C_{12}$ in either structure.

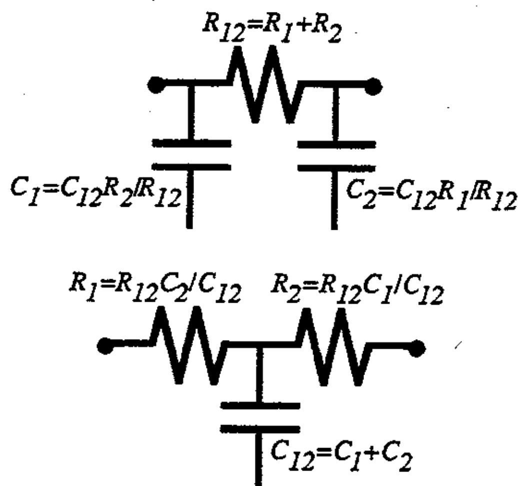

Fig. 4. Transforming between a π structure (top) and a T structure (bottom) preserves resistance, capacitance, and Elmore delay time in an RC tree.

Netlist Generation with 1st-Order Correction

The netlist is generated and then modified. First, a netlist is produced containing the layout-parameter-based capacitance values. Also produced is a file containing the 3D representation of all interconnects in the layout. The floating random-walk method is then used to replace the capacitance values in the netlist with accurate values based on the 3D representation. For an interconnect described by a lumped-element RC model, capacitor values are uniformly scaled so the total interconnect capacitance agrees with the random-walk result. This provides a first-order correction to the model.

2nd-Order Correction

We are currently attempting to improve accuracy by using the random-walk method to find individual distributed node-capacitor values, rather than apportioning a total single interconnect capacitance across distributed nodes in proportion to the corresponding LPE capacitance values.

Each node in the RC model is already associated with resistors, device pins, and a capacitor with an LPE value. We will also associate with each node a section of the physical interconnect from which the LPE capacitance value was calculated. Network generation and reduction will still be based on LPE capacitance values, but reduction will not use some transformations, such as the T–π, which effectively splits an existing capacitor.

In the reduced RC network, each LPE capacitor is associated with a section of the physical interconnect. The random-walk method can then be used to extract an accurate value for each node capacitance.

While the original RC network might include a direct correspondence with the physical interconnect, the degree of correspondence, by necessity, diminishes as the network is reduced. The methodology we propose here will maintain a correspondence between the capacitors in the model and the physical interconnect. Direct correspondence between the resistors and the physical interconnect will be lost. But, this correspondence is not required as long as the initial RC network accurately represents resistance. In Fig. 5, for example, capacitors associated with nodes $p1$, $p2$, and $p3$ correspond to physical sections of the interconnect. The resistors, on the other hand, do not have this direct relationship to the interconnect.

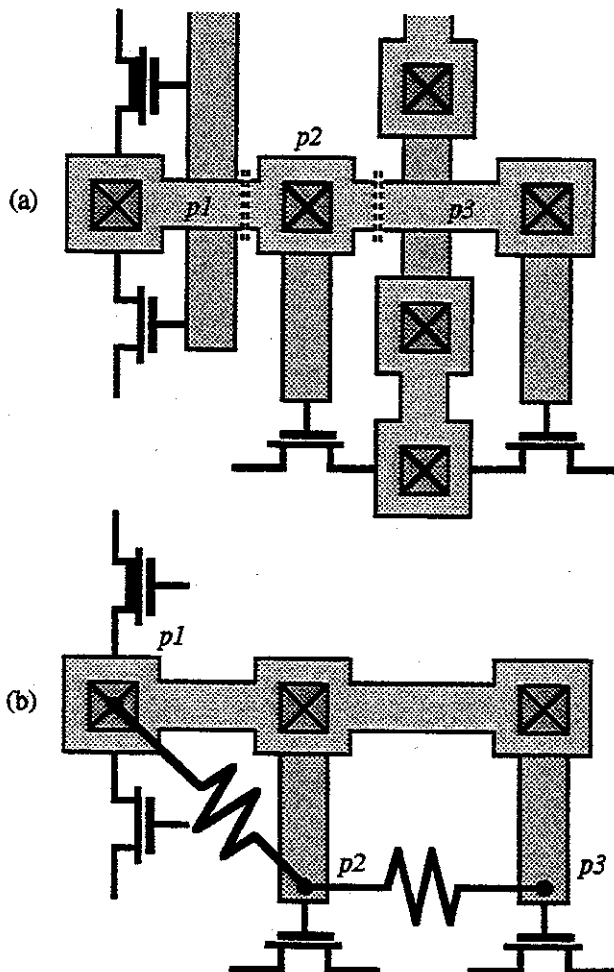

Fig. 5. (a) Reduction of an RC model while maintaining a correspondence between capacitors in the model and the physical interconnect. (b) Correspondence between the resistors and the physical interconnect may be lost.

SUMMARY

We have presented an overview of the floating random-walk method for extracting interconnect capacitance in complex, multilevel IC structures. We have presented, as well, a general methodology for extracting *RC*-interconnect data, starting with a 2D layout geometry. The methodology employs an existing floating random-walk capacitance extractor. Total interconnect capacitance is accurately calculated with the extractor to normalize otherwise inaccurate LPE values. We have outlined, as well, a procedure to further refine our proposed *RC* extraction methodology. During the generation and reduction of *RC*-interconnect networks, correspondence must be maintained between the physical circuit structure and the capacitors in the *RC* model. The procedure entails a direct calculation of distributed capacitance values within the interconnect of interest.

ACKNOWLEDGMENT

The work of the authors is supported in part by the SRC Center for Advanced Interconnect Science and Technology at Rensselaer, Contract ID: 448.023.

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