Spice-like Simulation Using Real Devices Instead of their Mathematical Models

V. V. Denisenko, Ph.D.

Research Laboratory of Design Automation, den@rlda.rnd.su

ABSTRACT - Modern Spice-like circuit simulators use increasingly accurate and sophisticated analytical models of components. But the validity of models, that is the probability that the procedure of the model verification is true, still remains very poor. The reason is that the mathematical models cannot be created without some simplifying assumptions. To solve this problem we suggest the use of real transistors instead of their mathematical models. It is shown that semi-natural models built on the basic of real transistors allow to control the transistor length and width with an error of a fraction of percent. Besides, they have an admissible speed and can be embedded into Spice-like simulators. The preferred way of the model use is a forecast of the radiation and temperature influence on the circuit to be designed and solution of some simulation problems that require high validity and accuracy.

Spice, simulation, circuit, analog, radiation, aerospace

INTRODUCTION

Current circuit simulators like Spice use increasingly accurate and sophisticated analytical models of components. But the validity of models, that is the probability that the procedure of the model verification is true, still remains very poor. In [1] several examples are given that despite the apparent "excellent accuracy" of drain-source current characteristics of MOS-transistor model the simulation results can be found unacceptable in practice.

The models designed for traditional MOS-transistor structure produce large error while simulating LDD, SOI, SPI, LATID-structure [1-3] and transistors with extremely short or narrow channel. As the model complexity increases, the parameter extraction procedure becomes labor intensive and there is a growing uncertainty that the model is really valid for your purpose. It can be found by fully chance that various "kinks and glitches" exist in the model behavior [1] and even model authors do not know it. The most CAD models today cannot pass all the benchmark tests given in [1].

This is because the high complexity of a model development and verification causes an emergence of human's errors. These errors come about as a result of a large number of simplifications whose applicability depends on the specific transistor structure. Besides, the model verification is carried out on a finite set of tests and technologies, on a finite set of transistor geometry and on a finite interval of voltage and current values. So, the transistor models may contain even obvious errors in equations that have not been detected during the testing process.

The said problems grow under simulation of military and aerospace products that must operate in a wide interval of temperature (including cryogenic), under influence of radiation, light, vibration, sound and electromagnetic field. It is most difficult to take into account the transistor self-heating, that is important for SOI-structure, or the volt-ampere characteristic degradation generated by semiconductor atoms offset as a result of radiation. That is why the full-scale test of the product is necessary before the serial fabrication.

The table look-up models [4-6], originally designed to improve simulation validity and decrease of CPU time consuming, met with several difficulties among which are the table dimension bound, poor small-signal accuracy and convergence of Newton-Raphson method for Spice-like simulation programs [4-6]. To weaken the problems they use the interpolation formulae and simplifying assumptions that allow to decrease the number of storage points up to 1000-3000 [4] or even 432 [5] under the error of 4-5%. But, the table grows very fast in size when it is necessary to enhance the precise of dc curve simulation or to take into account the substrate and the gate current, the model dependence on channel length and width, the external influences.

For drastically solution of stated problems one can use the real (natural) transistor itself. A similar approach has been used by Advanced Linear Devices [7], which offers to engineers first to breadboard the future device on the base of a special breadboarding set of real components, then to simulate it with Spice and only after that to implement it in silicon.

In this paper we suggest a new simulation method integrating mathematical simulation and breadboarding. This method allows very high simulation validity.

BASIC IDEA

The main idea is based on the possibility to divide the traditional mathematical model into two parts: the dc behavior model and the transistor's capacitance model (fig.1). This allows us instead of the dc model to use real transistor connected to a computer via analog-digital and digital-analog converters, and to substitute the dynamic part for any conventional mathematical model (fig.2, 3).

To be simulated, the circuit then has to be divided into two subcircuits. The first one is the whole circuit with an exception of the dc models to be substituted with

real transistors. The second subcircuit combines these "real" transistors.

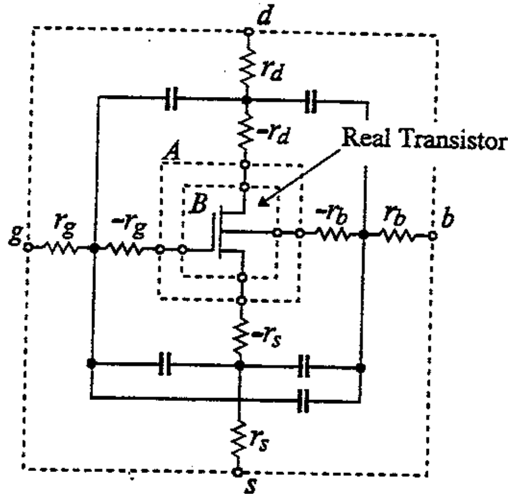

Fig.1. Complete MOS-transistor model

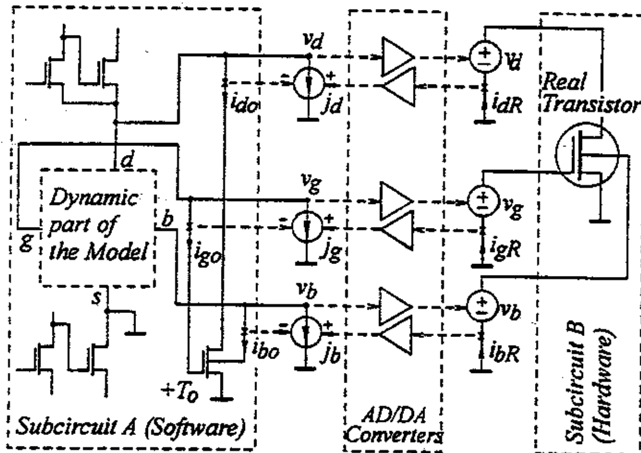

Fig. 2. "Connecting" of the real transistor to the mathematical model. Controlling circuits of controllable sources are shown with dashed line

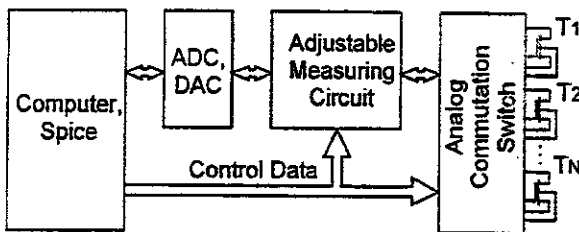

Fig.3. Hardware architecture

The simulation program treats the real transistor as a library model and allows to use only one transistor to simulate circuit containing any number of similar transistors.

The hardware part of semi-natural model (SN-model) contains computer, analog-digital I/O card, measuring circuit with adjustable circuit configuration and analog commutation switch that selects the required at this moment transistor (fig.3).

SEMI-NATURAL MOS-TRANSISTOR MODEL

A parameter control of long-channel MOS-transistor SN-model can be easily realized by means of similarity theory. But this method is not practically possible for short or narrow channel MOS-transistor. The problem is that the nonlinear similarity criteria are very cumbersome. Furthermore, their accuracy is limited by the accuracy of the mathematical model used to get these criteria.

The channel length control

The most precise method of parameter control, that fully inherits all advantages of a real transistor, requires to fabricate the set of transistors with channel lengths L varying from $L_{\min}$ to $L_{\max}$, where $L_{\max}$ is the boundary between short and long channel behavior of a MOS transistor, $L_{\min}$ is the minimal channel length. As follows from the experimental dependencies of the threshold voltage, body-effect factor and subthreshold slope on the channel length, given in [3,8] for LDD, LATID, SPI-LDD, SPI-LATID technologies, their values do not depend on L when $L > 1...3\mu m$. So, for simulation purpose it is enough to fabricate a semiconductor chip containing about 4-7 (see below) short-channel and 1 long-channel transistor.

The semi-natural MOS-transistor model is shown in fig.4. Here, we use the conventional designations. The controllable voltage and current sources in fig.4 simulate the following relations:

$$e_{ds} = V_{ds} \qquad e_{gs} = V_{gs} \qquad e_{bs} = V_{bs}$$
$$j_d = \mathbf{P}(i_{di}) \qquad j_g = \mathbf{P}(i_{gi}) \qquad j_b = \mathbf{P}(i_{bi})$$

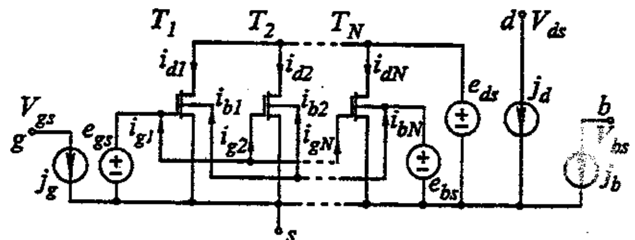

Fig.4. Semi-Natural static MOS transistor model

The operator $\mathbf{P}(\bullet)$ is realized by the program and will be defined below.

To combine the possibility of a channel length control with high accuracy of real transistors, the operator $\mathbf{P}(\bullet)$ must change to an identity: $\mathbf{P}(i_{di}) = i_{di}$ if $L = L_i$, where i is the transistor index in fig.4. Then, under condition that $L = L_i$, the SN-model will reproduce the characteristics of one of the transistors $T_1 \ldots T_N$ with zero methodical error. These requirements are satisfied by some interpolation operator. We use the cubic spline interpolation.

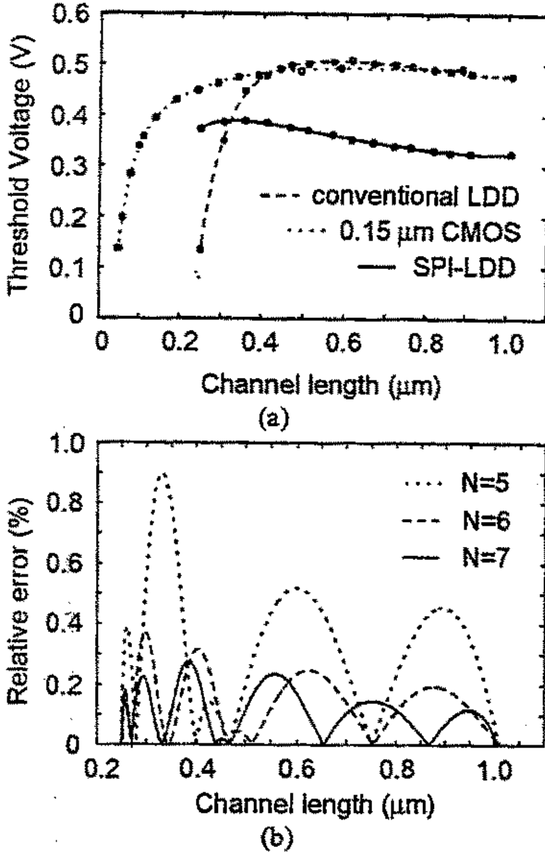

Fig.5. Subthreshold voltage (a) [2, 8] and model error (b) versus channel length for three types of technologies; N is the number of transistors in the model. Experimental data are marked by boxes

To estimate the SN-model error, we have used experimental curves for threshold voltage as a function of a channel length for n-channel MOS transistor, given in [2, 8] (fig.5(a)). It is the threshold voltage that ought to use to find the channel lengths $L_1 \ldots L_N$ and for error analysis because it exhibits the most effect upon MOS-transistor characteristics.

From the curves of fig.5 we can see that if the number of real transistors is increased from N=5 to N=7, the error decreases from 0.9% to 0.3%. At the supporting points $L = L_i$ the error is zero.

Notice, that in case of SN-model interpolation is made for L, not for (V_{ds}, V_{gs}, V_{bs}) as is the case of table look-up models [4-6]. Therefore, the dc characteristics of SN-model are defined by real transistors only, hence, the model allows valid representation of their dependencies on voltage, temperature and external influences. That is why the surprises in model behavior are fully excluded.

Channel width control

For channel width control we suggest using the model, shown in fig.6.

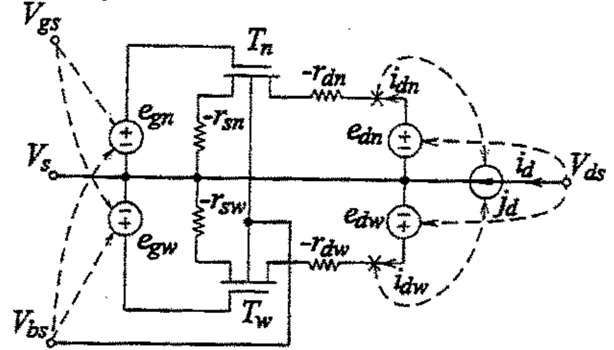

Fig.6. Electrical circuit for channel width control

Here, the controlled sources simulate the following dependencies:

$$e_{gn} = V_{gs} - \frac{\pi\varepsilon_{si}}{4C_{ox}}\left(\frac{\delta_w}{W_w} - \frac{1}{\Delta W}\right)(2\varphi_F - V_{bs})$$

$$e_{gw} = V_{gs} - \frac{\pi\varepsilon_{si}}{4C_{ox}}\left(\frac{\delta_n}{W_n} - \frac{1}{\Delta W}\right)(2\varphi_F - V_{bs})$$

$$J_d = M_n i_{dn} + M_w i_{dw}; \quad e_{dn} = e_{dw} = V_{ds}$$

where δ_w, δ_n are parameters to represent the narrow-channel effect in transistors T_w and T_n; ε_{si}, C_{ox}, φ_F are respectively the permittivity of semiconductor, oxide capacitance and a Fermi level; W_n and W_w are the channel widths of transistor T_n and T_w respectively, $W_n < W_w$. The scale factors M_n, M_w and the parameter ΔW are calculated as

$$M_n = \frac{W - W_w}{W_n - W_W}, \; M_w = 1 - M_n, \; \frac{1}{\Delta W} = \frac{1}{W_n} + \frac{1}{W_w} - \frac{1}{W}$$

where W is the channel width of the transistor to be simulated. The meaning of other designations can be seen from fig.6.

Source and drain resistance control

When using the SN-model the MOS-transistor capacitances must be connected between the channel and resistances of source and drain (fig1). To realize such a connection it is necessary to extract the parameters of r_d, r_s, r_g, r_b and to compensate them by equal in value

negative resistances, then to introduce the required positive resistances into the simulating circuit (fig.1).

SIMULATION ALGORITHM

The suggested iterative coupling method is based on exploiting "the negative transistor" [10]. The negative transistor may be realized by software and is characterized by negative input, output and transfer resistance.

Let us introduce vector variables:

$$\mathbf{I}=\mathbf{I}(t)=\begin{bmatrix} i_d(t) \\ i_g(t) \\ i_b(t) \end{bmatrix},\ \mathbf{V}=\mathbf{V}(t)=\begin{bmatrix} v_d(t) \\ v_g(t) \\ v_b(t) \end{bmatrix},\ t\in[0,T],$$

where $i=i(t)$, $v=v(t)$ are currents and voltages measured at the subcircuit terminals (fig.7); their subscripts are explained by fig.7; t - time; $[0,T]$ - simulation interval.

To couple the subcircuits A and B we shall use the iteration method:

$$\mathbf{I}^{k+1}(t)=\mathbf{Y}\left(\mathbf{V}^k(t)\right),\quad \mathbf{V}^k(t)=\mathbf{F}\left(\mathbf{I}^k(t)\right),$$

where $\mathbf{Y}$ is some nonlinear algebraic operator describing the subcircuit B, $\mathbf{F}$ is a nonlinear dynamic operator with some initial conditions for subcircuit A (fig.7).

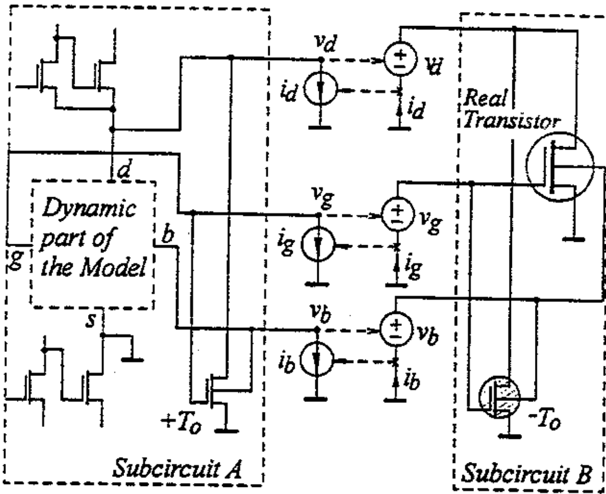

Fig.7. Application of a negative transistor to improve the convergence; T_0 is the negative transistor

A speciality of the above iterative process is that it is executed by functions of time, similarly to the WR-method [11]. Transform (1) to

$$\mathbf{I}^{k+1}(t)=\mathbf{Y}\left(\mathbf{F}\left(\mathbf{I}^k(t)\right)\right),$$

where $\mathbf{Y}(\mathbf{F}(\bullet))$ is the superposition of operators $\mathbf{Y}$ and $\mathbf{F}$. We shall define the norm $\|\bullet\|$ of vectors $\mathbf{V}$, $\mathbf{I}$ as:

$$\|\mathbf{X}\|=\max_{i\in[1,3]}\left\{\max_{t\in[0,T]}|x_i(t)|\right\}.$$

A general convergence criterion for a considered iterative process has been investigated in details. To evaluate how the parameters of the transistor T_0 and the simulated circuit influence the convergence, consider the system linearized in some small neighborhood of the exact solution. Let also the vector iterates $\mathbf{I}^k(t)$ and $\mathbf{I}^{k+1}(t)$ are close enough to the solution. Then, if the operators $\mathbf{Y}$ and $\mathbf{F}$ are differentiable, $[\mathbf{Y}(\mathbf{F}(\mathbf{I}))]' = \mathbf{Y}'_{\mathbf{F}}\mathbf{F}'_{\mathbf{I}}$, where $\mathbf{Y}'_{\mathbf{F}}$ and $\mathbf{F}'_{\mathbf{I}}$ are the Frechet derivatives and the norm of errors satisfies the following relation:

$$\left\|\mathbf{I}^{k+1}-\mathbf{I}^k\right\|\le\left\|\mathbf{Y}'_{\mathbf{F}}\mathbf{F}'_{\mathbf{I}}\right\|\left\|\mathbf{I}^k-\mathbf{I}^{k-1}\right\|.$$

Hence, we can write the convergence condition of the iterative process as:

$$\left\|\mathbf{Y}'_{\mathbf{F}}\mathbf{F}'_{\mathbf{I}}\right\|<1.$$

One can show that to ensure the convergence of iterations for conventional MOS-transistor inverter in the worst case, it is enough to specify the parameters of a simulated transistor with a tolerance the 300% [10].

EXPERIMENTAL RESULTS: EMBEDDING INTO SPICE-LIKE SIMULATION SYSTEM

Based on the proposed idea we have developed and examined the simulating system that uses the MicroSim® DesignLab™ 8.0 commercial program for circuit description and simulation. On the stage of a graphical (schematic) input of the circuit we assign to a field "Model attribute" the mark "Real" and indicate the number of the corresponding AD/DA channel, to which the real transistor is connected. A specially written software translates this marks into the input language of PSpice®A/D [12] and the additional supervisory program, which organizes iterations coupling SN-model with PSpice®A/D.

When simulating test circuit (fig.8) we have used the real transistors (M1Real-M3Real) in combination with the mathematical model of transistors M1-M6. Despite the fact that negative transistor characteristic is very different from real transistor characteristics (fig.9) the coupling process converges rather fast (fig.10).

Speedup and hardware error

The model access time is composed from AD and DA conversion time, I/O instruction runtime and time of interpolation algorithm execution. We have purpose-built an experimental equipment using simple 12-bit AD-

converters with conversion time of 80 μs and the 10-μs DA-converter. The total SN-model access time is about 300 μs. The corresponding computation time for one point of dc curve for BSIM3 [3] model, built in PSpice®AD Version 8.0 of MicroSim® Corp. and Pentium-166, is 600 μs. However, to realize the waveform algorithm to couple SN-model and PSpice® we need some extra time, that results in the total slow-up factor of 1.5-5 depending on the required precision and particularities of circuit to be simulated.

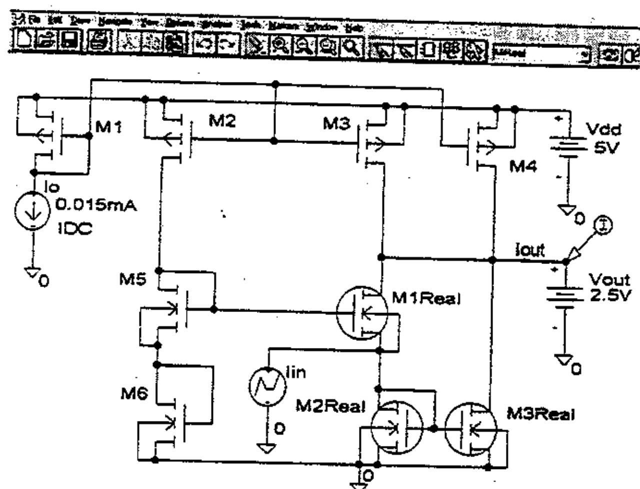

Fig.8. Test circuit - current squarer/divider [13] described with MicroSim® DesignLab™ user interface

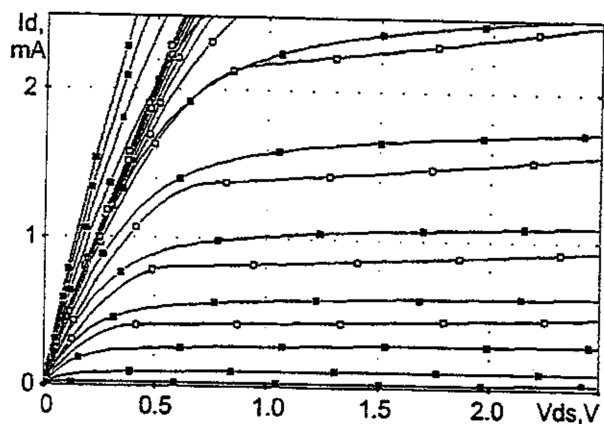

Fig.9. Volt-ampere characteristics of the real (□) and negative (■) transistor

The hardware error is easily estimated by automatic testing of the AD/DA channel. To achieve a multiplicative error of 0.1% and an additive error of 1mV is easy, but the achievement of 0.01% and 0.01mV error is the problem for technical and, maybe, economical reasons. If the error exceeds predefined value or the simulated value overruns its dynamic range, the computer outputs an error message.

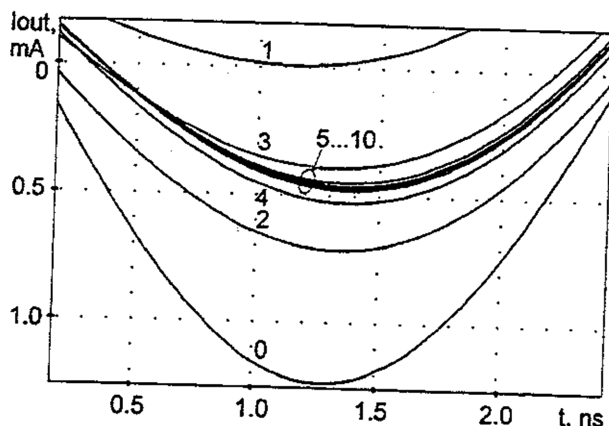

Fig.10. Output current Iout versus time for input Iin (ramp function of time, fig.8) simulated in 10 iteration steps

ADVANTAGES AND LIMITATIONS

The suggested simulation method has built-in limitations in digit capacity, dynamic range and possibilities to control the technology depending parameters.

A basic limitation is an impossibility to predict the circuit behavior for future technologies before we produce the set of real transistors for SN-model. Further, we cannot control the model parameters (except channel length and width), such as doping concentration, junction depth, gate oxide thickness and so on. Nevertheless, using the correction table, it is possible to take into account the small variations in technology parameters, caused by technological tolerances.

The second limitation is that a typical AD/DA converter capacity does not exceed 14-16 bit, that is not enough to simulate supersensitive analog circuits. Consequently, we have to combine a real transistor and a mathematical model to smooth the AD-converter's data, that results in the slow-up of simulation process.

The third limitation is a sensitivity threshold of the measuring circuit. The precise measurement in nanoampers range requires a long time and the following data processing by statistic method. Therefore, in this case we need to use a mathematical model. Both models can be adjusted so the first and the second derivatives are continuous in the coupling point.

An advantage of the suggested method is the extremely high simulation validity independent on technology, size, structure's characteristic and operating conditions of a MOS-transistor. It is achieved by removing from SN-model the reasons reducing validity of the mathematical model. First, the SN-model does not use simplifying assumptions about transistor construction and their physical behavior, second, the model error is easily controllable during the simulation process, third, SN-model does not need the parameter extraction.

The SN-model is unique in the ability to store the huge amount of information containing into a real transistor. For typical MOS transistor the amount of information,

contaned in dc curves, is approximately 10^{20} bit. But, using inexpensive 12-bit ADC and 1, 10, 100 and 1000 time scaling amplifier with a mean-square noise voltage of 0.1 mV, we can have an access to $6 \cdot 10^{17}$ bit of data.

AREA AND SPECIALTY OF APPLICATION

From the above advantages and limitations of SN-model it follows that there is no point in using it instead of mathematical MOS-transistor model. It can become one of the models for Spice-like simulation system and be useful in cases described below.

A precise circuit verification. Let us assume that with Spice we have achieved a desirable result, but we want to be sure that after we have embodied the circuit in silicon, the required characteristics are preserved. For this purpose the mathematical models of transistors should be replaced with the SN-models. It is often enough to make such a replacement only for those transistors whose parameters have the highest effect on circuit characteristics. For example, even for a very complicated operational amplifier, its gain, cutoff frequency and common-mode rejection are determined by some transistors in the input stage; the accuracy of an analog multiplier is determined with a few transistors which generate square-law characteristics.

The prediction of external effects upon the circuit to be designed. To investigate radiation effects it is enough to expose the real transistors of some SN-models with various doses, then use them for simulation. In these conditions we can automatically take into account the effects like displacement of semiconductor atoms, lattice disturbance, lifetime and mobility change, etc.

The precise simulation. Simulation with high accuracy and validity can be used to solve many design problems, but the practicability of such an application has to be determined by designer depending on his purpose.

The circuit operation under cryogenic temperature can be investigated if we place the SN-model into a dewar vessel.

Since the thermal processes change slowly compared to a simulation time, the SN-modeling allows us to explore the *self-heating dynamic* of SOI MOSFET or power FET on a heatsink.

In a similar way the SN-modeling allows to simulate the *microphonic effect,* if the sound source is synchronized with a model access time, as well as an *influence of pressure, light and vibration.*

CONCLUSION

To solve the problem of accuracy and validity, inherent in analytical and table look-up models, we suggest the use of a new simulation method based on real transistors applied instead of their mathematical models. The suggested method allows to control channel width, length of MOS-transistor and exhibits a satisfactory performance. The method is destined for prediction the circuit behavior under external influences and solution of various simulation problems for extremely high validation and accuracy. The method can be embedded into existing simulation programs. The SN-models are well combined with hardware accelerator for circuit simulation [14,15].

REFERENCES

1. Y. P. Tsividis, K. Suyama, *IEEE Journal of Solid-State Circuits,* vol.29, March, 1994, pp.210-216.
2. Hori A., Hiroki A., Nakaoka H., Segawa M., Hori T., *IEEE Trans. on Electron Devices*, Vol. 42, No. 1, Janury 1995, p.78-85.
3. Huang J.H., Liu Z.-H., Jeng M.C., Hui K., Chan M., Ko P.K., Hu C. BSIM3 Manual (version 2.0). *Department EECS UC Berkeley*, CA 94720 March 7 1994. - 215 p.
4. Rofougaran A., Adidi A.A., *IEEE Trans. on CAD of ICAS,* Vol. 12, No.2, Febr. 1993, pp. 324 - 335.
5. Allen Ph.E., Yoon K.S., *IEEE Int. Conf. CAD,* Santa Clara, Calif., Nov.7-10, 1988, Dig. Tech. Pap., Washington, 1988, pp.124-127.
6. Yanilmaz M., Eveleigh V., *30th Midwest Symp. Circ. and Syst.*, Syracuse, N.Y., Aug.17-18, 1987, Proc., N.Y., 1988, pp. 1074-1077.
7. Frank Goodenough., *Electron. Design*, pp. 159, 160, 162, 163, NO.14, 1991.
8. Davari B., Dennard R.H., Shahidi G.G., *Proceedings of the IEEE*, vol. 83, NO. 4, April 1995, pp. 595-606.
9. Liu Z.-H., Hu C., Huang J.H. Chan T.J., Jeng M.C., Ko P.K., Cheng Y.C., *IEEE Trans on Electron Devices.*, vol.40, No. 1, January 1993., pp.86-95.
10. Denisenko V.V., *In Proc. 1997 International Symposium on Nonlinear Theory and its Applications* (NOLTA'97), Honolulu, U.S.A., Nov.29-Dec.2, 1997, p.p.345-348.
11. Lelarasmee E., Ruehly A.E., Sangiovanni-Vincentelli A.L., *IEEE Trans. Comput. Aided Design of Integrated Circuits and Syst,* July 1982. pp.131-145.
12. "MicroSim® PSpice®A/D & Basics+", User's Guide, MicroSim Co., 20 Fairbanks, Irvine, California, Version 8.0, June, 1997.
13. Vittoz E.A. Journal of VLSI Signal Processing, vol.8, July 1994, pp. 27-44.
14. Denisenko V.V., *Proc. EURO-DAC'94 with EURO-VHDL'94*, 1994, Grenoble, France, IEEE Comp. Soc. Press, Los Alamos, Calif., pp. 182-186.
15. Denisenko V.V, *In Proc. 1993 International Symposium on Nonlinear Theory and its Applications* (NOLTA'93), Hawaii, U.S.A., Dec. 5-10, 1993, 1.6.4.