Validation and Calibration of Electrothermal Device Models Using Infrared Laser Probing Techniques

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ABSTRACT

As it has recently been demonstrated, the internal distribution of carrier concentration and temperature is accessible to accurate measurements by various infrared laser probing techniques. In this work we present an advanced method for the validation and calibration of electrothermal device models which is based on experimental results obtained by these methods. As an example, numerical investigation of a pin power diode and an insulated gate bipolar transistor reveals Joule and recombination heat to be the most significant effects on the temperature profile. The very sensitive Internal Laser Deflection method enables the experimental detection of the Peltier heat at metal contacts, thus verifying the thermal boundary conditions in the simulation. As it can be seen from Backside Laser Probing, the strong rise of temperature during short circuit operation is also accurately reproduced by the calibrated numerical simulation.

Keywords: Validation of electrothermal device models, internal characterization techniques, parameter extraction, power devices.

Introduction

While the measurement of electrical terminal characteristics has become state of the art in device characterization for many years, various infrared laser probing techniques were recently introduced for the experimental analysis of the internal distribution of carrier and heat flow. These probing techniques are based on the dependence of the refractive index on carrier concentrations and lattice temperature. From Internal Laser Deflection measurements [1], the vertical distribution of carrier concentration and temperature can be observed in the interior of devices, provided they are $100\,\mu$m in depth or larger. The Backside Laser Probing technique [2] yields information on the lateral profiles and is also applicable to the investigation of integrated circuits and small structures, e. g. the channel region in MOS devices. The measured data are useful for the validation and calibration of electrothermal device models. As an example, we investigate electrothermal effects in two modern power devices, a pin diode and an insulated gate bipolar transistor (IGBT).

Numerical Modeling

For accurate electrothermal modeling of semiconductor devices, heat generation and conduction in the semiconductor have to be treated consistently with the drift–diffusion model. The electrical behavior of the device is calculated by solving Poisson´s equation

$$\vec{\nabla}\left(\varepsilon\vec{\nabla}\Psi\right) = q\left(n - p + N_A^- - N_D^+\right)$$

and the particle balances for electrons and holes

$$\frac{\partial n}{\partial t} - \frac{1}{q}\vec{\nabla}\vec{J}_n = -R \quad \text{and} \quad \frac{\partial p}{\partial t} + \frac{1}{q}\vec{\nabla}\vec{J}_p = -R$$

where the driving forces of the current densities are the gradients of the state variables Φ_n, Φ_p (electrochemical potentials), and T (temperature):

$$\begin{aligned} \vec{J}_n &= -q\,\mu_n\,n\left(\vec{\nabla}\Phi_n + P_n\vec{\nabla}T\right) \\ \vec{J}_p &= -q\,\mu_p\,p\left(\vec{\nabla}\Phi_p + P_p\vec{\nabla}T\right) \end{aligned}$$

Based on the principles of irreversible thermodynamics the following heat flow equation is derived [3] which accounts for heat generation and conduction in consistence with the drift–diffusion model:

$$c\,\frac{\partial T}{\partial t} - \vec{\nabla}\left(\kappa\vec{\nabla}T\right) = H$$

where the heat generation rate H is given by

$$\begin{aligned} H &= -\vec{\nabla}\left[(\Phi_n + P_nT)\vec{J}_n + (\Phi_p + P_pT)\vec{J}_p\right] \\ &\quad + q\left(\Phi_n - T\frac{\partial\Phi_n}{\partial T}\right)\frac{\partial n}{\partial t} - q\left(\Phi_p - T\frac{\partial\Phi_p}{\partial T}\right)\frac{\partial p}{\partial t} \end{aligned}$$

A familiar interpretation of H is obtained by evaluating the divergence operator in the above equation, revealing well known contributions to the total heat generation rate: First, the Joule heat of holes and electrons,

$$\vec{J}_p^{\,2}/qp\mu_p \quad \text{and} \quad \vec{J}_n^{\,2}/qn\mu_n,$$

respectively. Second, the recombination heat

$$qR\,(\Phi_p + TP_p - \Phi_n - TP_n).$$

Third, the Peltier/Thomson heat

$$-\vec{J}_p T \vec{\nabla} P_p - \vec{J}_n T \vec{\nabla} P_n,$$

and fourth, an additional heat generation rate caused by transient variations of the carrier densities.

This set of equations is implemented in the general purpose device simulator DESSIS^{ISE} [4], which has been used for calculating the results presented in this work.

Internal Laser Deflection measurements

Laser probing techniques exploit the dependence of the silicon refractive index on carrier concentrations and lattice temperature.

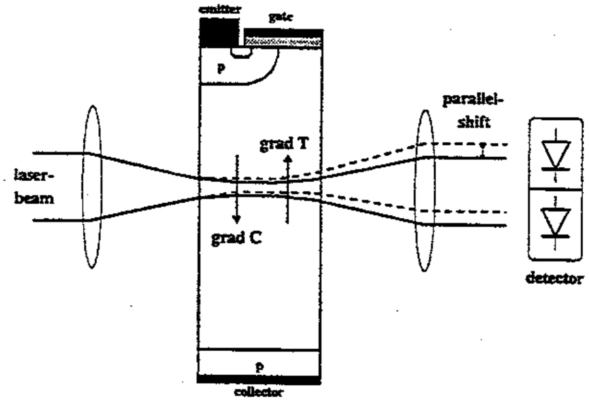

Figure 1: Experimental setup for Internal Laser Deflection measurements.

The Internal Laser Deflection method [1] is based on the deflection of a laser beam (Fig. 1) by local modulations of the refractive index which are caused by the injection (or removal) of carriers and/or local variations of the lattice temperature. A four quadrant photodiode detects the parallel shift and the total transmitted intensity of the laser beam. Measuring these signals, the local carrier concentration and temperature gradient can be extracted. Vertical profiles are obtained by shifting the device along its vertical axis.

The Internal Laser Deflection technique can be applied for the investigation of devices whose depth of the active region is 100 μm or more. Its greatest advantage is the very high sensitivity which enables the detection of a temperature rise within a few Millekelvin. However, the deflection signal saturates if the parallel shift becomes too large so that the laser beam only touches one segment of the detector. Thus, the measurement range is limited to some Kelvin of temperature rise.

Backside Laser Probing

For Backside Laser Probing [2], a laser beam enters at the bottom side of the structure, propagates vertically through the device, and is reflected at the top metallization (Fig. 2). Modulations of the refractive index due to variations of the carrier concentrations or lattice temperature cause a phase shift of the probing beam which is detected by interference with a reference beam:

$$\Delta\varphi = 2\frac{2\pi}{\lambda}\int_0^L \left(\frac{\partial n_{Si}}{\partial T}\Delta T + \frac{\partial n_{Si}}{\partial n}\Delta n + \frac{\partial n_{Si}}{\partial p}\Delta p\right) dz$$

The application to vertical devices requires to open a window in the rear contact metallization which is done by photolithographic structured etching.

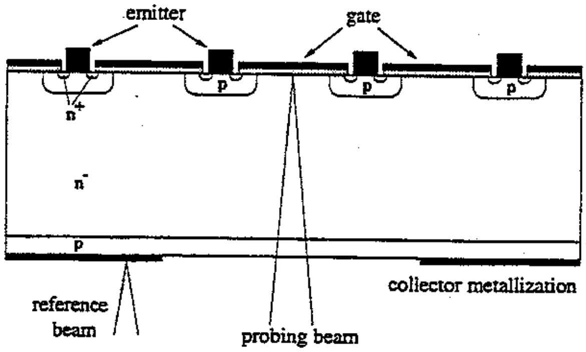

Figure 2: Experimental setup for Backside Laser Probing

The Backside Laser Probing technique allows the detection of a temperature rise of some Millekelvin as well as a very large temperature rise of 100 K or more. It has been successfully employed for the investigation of a large variety of structures, e. g. MOSFETs [5], DRAMs, IGBTs [6], and GaAs power sensors [7].

Results

Designing modern power devices implies a trade-off between turn-off losses and conduction losses: On the one hand, a high carrier injection into the intrinsic region would be desirable in order to achieve a low voltage drop in the forward conducting state. On the other hand, this will increase turn-off losses, as a greater amount of stored carriers needs to be extracted. Therefore, an additional heavy metal diffusion is employed for carrier lifetime control. For an exact treatment of this effect, complicated models for the local lifetime reduction had to be implemented in the simulator. It has been demonstrated that a simplified model (Scharfetter relation), which is preferable for the sake of computational economy, also yields accurate results if the model parameters are appropriately adjusted [8]. For this purpose, internal laser probing techniques provide valuable information for a reliable model calibration.

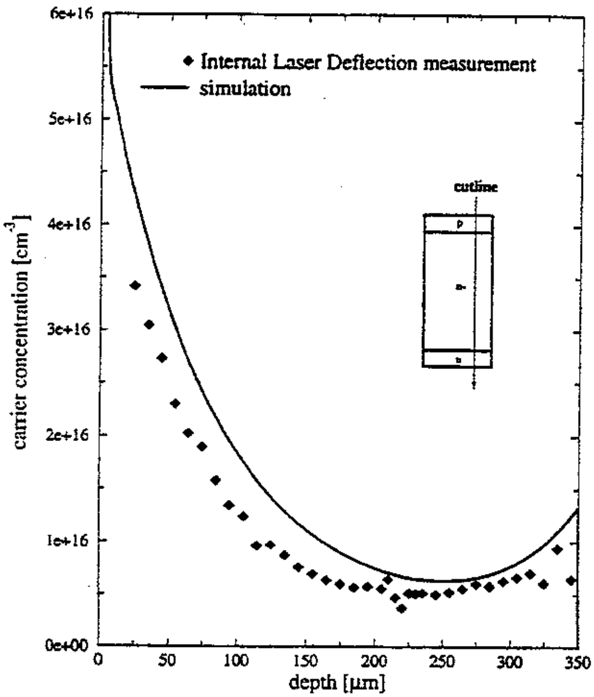

Figure 3: Carrier distribution of a pin diode at a current density of 150 A/cm^2

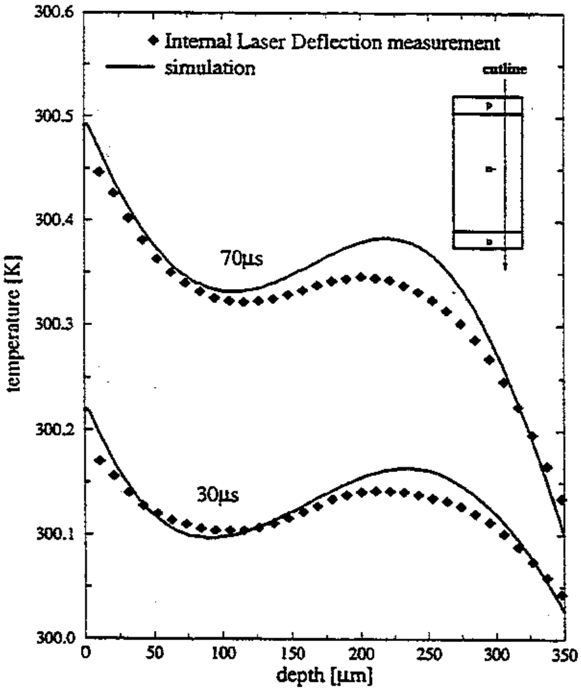

Figure 4: Temperature profile after turn-on of a pin diode

Pin Power Diode

As a first example, a pin power diode is investigated by means of Internal Laser Deflection measurement. Since this method is very sensitive and accurate, the carrier concentration is plotted on a linear scale (Fig. 3). From the carrier distribution in the weakly doped region information on emitter efficiencies and carrier lifetimes can be extracted. For instance, the ambipolar diffusion length and, thereby, the ambipolar carrier lifetime is directly related to the curvature of the carrier concentration profile, since power devices are operated under high injection conditions.

The temperature profile (cf. Fig. 4) after turn-on of a current pulse shows a local maximum in the bulk of the device which arises from Joule heating of electrons and holes in the drift region (cf. Fig. 5). The second temperature peak at the anode side is caused by recombination heat at the p^+n^--junction. Thus, minority carrier lifetime in the p^+-emitter can be extracted from the height of this temperature peak.

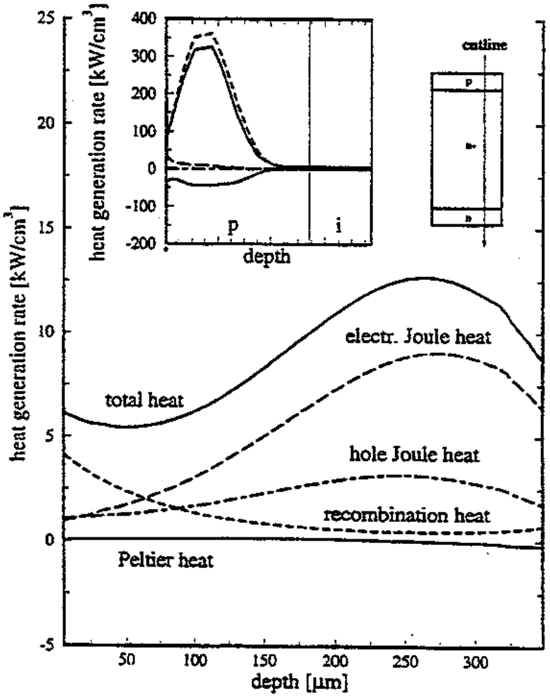

Figure 5: Heat generation in a pin diode. The insert shows a detailed view of the heat generation rate at the p^+/n^--junction.

Insulated Gate Bipolar Transistor (IGBT)

Internal Laser Deflection measurements have also been applied for the internal characterization of an insulated gate bipolar transistor. As it can be seen from the linear carrier concentration profile (Fig. 6), carrier lifetimes are very large. Since the simulation results are not very sensitive to their exact values, they can be easily adjusted within the required accuracy. After lifetime

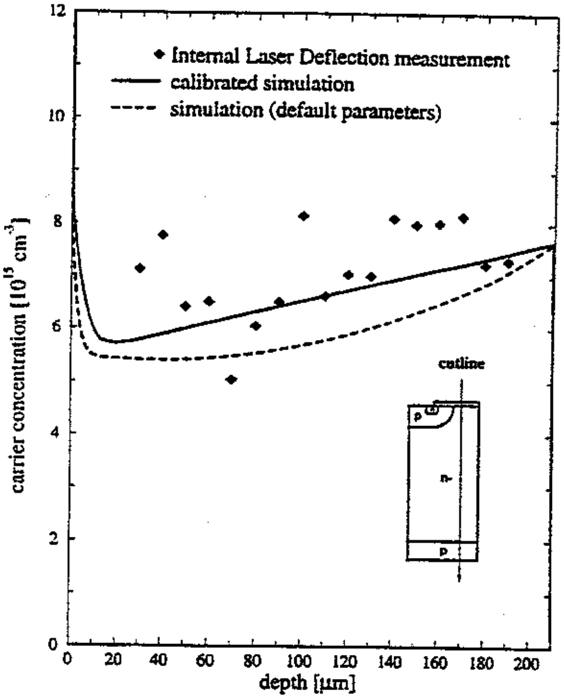

Figure 6: Carrier distribution in an IGBT at a current density of $150\,\mathrm{A/cm^{-2}}$

adjustment, the mobility models are calibrated with reference to the forward characteristics [8].

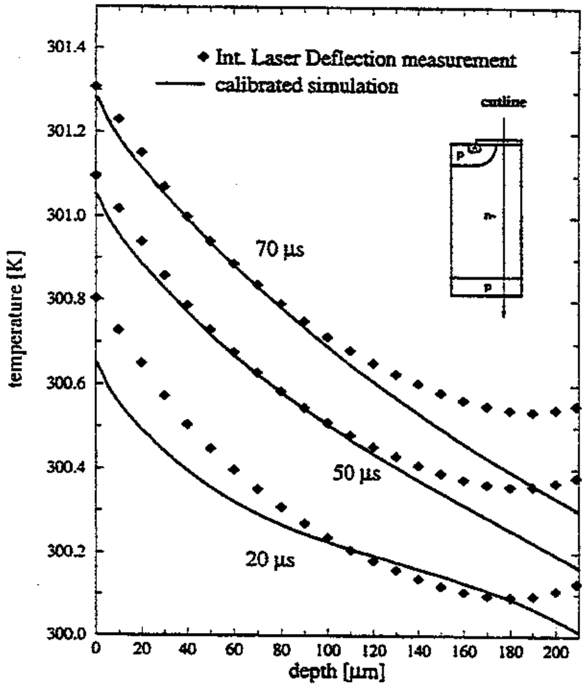

Figure 7: Temperature profiles in an IGBT during transient switching with ohmic load, $150\,\mathrm{A/cm^{-2}}$ current pulse

The most significant effect on the temperature profile arises from heat dissipation in the channel region and in the space charge region of the reverse biased pn–junction at the top. The resulting temperature increase during transient switching with ohmic load (cf. fig. 7) is accurately reproduced by the calibrated simulation, thus confirming and validating the electrothermal model. Note that the slight increase of temperature measured at the bottom side is caused by Peltier heating at the metal contact [9] which is not included in the simulation as a consequence of simplifications made in the thermal boundary conditions (cf. [3] and [4]).

For the internal characterization under short circuit operation (cf. Fig. 8), Backside Laser Probing is employed. Although this technique provides only integral information for vertical devices, it allows the experimental investigation of the device region close to the top side, in particular the channel region. This is of great importance for the detection of critical operating conditions. In addition, the Backside Laser Probing method is capable of detecting enormous temperature rises of 100 K or more, as they typically occur during short circuit operation. In this case, the thermal contribution becomes the dominant effect on the total phase shift which is therefore approximately proportional to the total heat ΔQ dissipated inside the device.

$$\Delta\varphi(t) = \frac{4\pi}{\lambda c A}\frac{\partial n_{Si}}{\partial T}\int\limits_0^L cA\Delta T(z,t)\,dz = \frac{4\pi}{\lambda c A}\frac{\partial n_{Si}}{\partial T}\Delta Q(t)$$

Possible side effects of the sample preparation, in particular the etching of a window in the collector contact metallization, are investigated by simulating multiple IGBT cells. While the integrated carrier concentration in the window region is increased by about 20 %, the influence of the collector window on the temperature profile integrated along the vertical beam propagation path is practically neglegible [6].

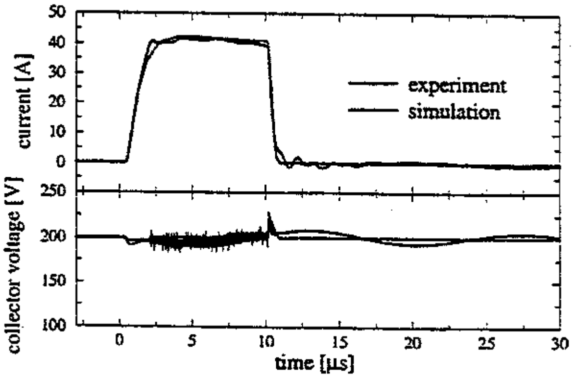

Figure 8: Current and voltage wave forms for short circuit operation at $U_{CE} = 200\,\mathrm{V}$

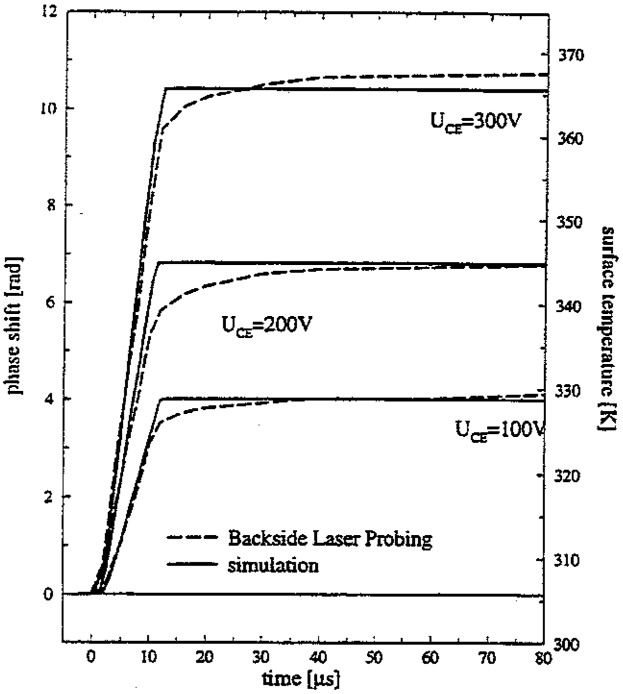

Figure 9: Phase shift for short circuit operation, with a pulse duration of 10 μs, measured by Backside Laser Probing

Since the heat flow through the device surfaces can be neglected on the short–term time scale immediately after turn–on, the constant power dissipation during the current pulse linearly increases the total heat inside the device and, thereby, the measured phase shift (cf. fig. 9). When the measurement signal is monitored for a period of several 100 μs, the cooling of the structure is clearly reflected in an exponential decrease of the phase shift signal. The thermal coupling of the device under test to the substrate can be extracted from the respective time constant. Note the excellent agreement of the simulated and the measured phase shift which validates the model for heat generation and conduction in the semiconductor.

Conclusions

Internal carrier concentration and temperature profiles have been determined by various infrared laser probing techniques. In addition to the measurement of terminal characteristics, these experimental results provide valuable information for the investigation of electrothermal effects in semiconductor devices. Thereby, the self–consistent electrothermal extension of the drift–diffusion model can be validated and calibrated so that the experimental results are reproduced by the calibrated simulation with very high accuracy.

The introduced laser probing techniques are sensitive to changes of the refractive index, either in its real or in its imaginary part. Principally, they can be also employed for the time–resolved investigation of any other internal variable which affects the refractive index, e. g. mechanical stress.

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