Methodology for Calibrating Process and Device Simulators by Extracting Model Parameters from Electrical Data

Hok-Min Ho, Yue Zu, Konstantin V. Loiko, and David H. Y. Lim
Chartered Semiconductor Manufacturing Ltd.
60 Woodlands Industrial Park D, Street 2, Singapore 738406

ABSTRACT

This paper describes a physically based methodology for calibrating 2D semiconductor process and device simulators. The calibration begins with the determination of 1D and 2D doping profiles by means of extracting model parameters from electrical data without SIMS analysis, followed by tuning mobility model parameters to match the device I-V characteristics. The methodology is successfully demonstrated for NMOS and PMOS devices fabricated by 0.25μm salicide retrograde well CMOS process.

Keywords: TCAD calibration, 2D process and device simulation, reverse short channel effect, short channel effect, 0.25μm CMOS.

INTRODUCTION

Since the complexity of IC fabrication processes constantly increases, the use of simulation tools for the development of new technologies is getting more and more important. However, as the device dimensions shrink to 0.25 μm or below, the calibration of process and device simulators becomes more complicated because of the difficulties in characterizing the impurity profiles for shallow junctions and high cost of SIMS analysis. One of possible ways for overcoming these difficulties is to use phenomenological models of dopant profiles [1,2]. Although this approach gives fast and reasonably accurate results, the models are not physically based and the tuned model parameters can not be automatically transferred to new generations of technologies.

It is essential to have the correct 2D doping profile in order to have an accurate simulation of devices over a range of gate lengths. As the device feature size decreases, the impact of interaction between source/drain (S/D) and channel on device performance increases. For example, the channel boron redistribution in NMOS devices is caused by implant damage during S/D formation in which results reverse short channel effect (RSCE) [3]. Commercial 2D process simulator like TSUPREM-4 [4] have the capability to model the interaction between the channel and S/D regions. But, some model parameters need to be fine tuned before being used for accurate simulation.

In this paper, we describe a simple and cost-effective physically based methodology for calibrating 2D process and device simulators based on extracting the model parameters from the electrical data without SIMS analysis. Such approach allows quick fine tuning of model parameters for new CMOS technologies.

EXPERIMENTAL

The NMOS and PMOS devices with channel length varied from 10μm to 0.22μm were fabricated according to the 0.25μm salicide retrograde well CMOS process. Channel width of transistors is 20μm in order to eliminate narrow channel effects. A set of splits is done to demonstrate the RSCE on threshold voltage for different thermal cycle following NLDD implant in NMOS and pocket implant in PMOS, as shown in Tables 1 and 2 respectively.

Table 1. Split data for NMOS.

Wafer no.	1st NLDD anneal	2nd NLDD anneal
1	975°C 15sec	900°C 15min O_2
2	skip	900°C 15min O_2

Table 2. Split data for PMOS.

Wafer no.	pocket implant	PLDD implant
3	skip	BF2 3E14_15_0
4	As 1E13_80_0	BF2 3E14_15_0

METHODOLOGY AND RESULTS

The procedure of calibration is divided into three parts. The 1D doping profile is calibrated first by extracting gate oxide thickness of long channel device from C-V measurement and matching with experimental threshold voltage vs substrate bias (VT-Vb) data through adjusting the poly workfunction. Then, the 2D doping profile of channel and the S/D is determined by matching RSCE and SCE in threshold voltage vs channel length (VT-Lg) curve. Finally, electron and hole mobility model parameters are tuned to fit the measured Id-Vg and Id-Vd curves.

1D doping profile matching

The comparison of experimental and simulated VT-Vb data of long channel (Lg=10μm) NMOS and PMOS devices are shown in Figs. 1 and 2 respectively. Good agreement between experimental and simulated values shows that the gate oxide thickness and the 1D channel doping profile is well calibrated. The gate oxide thickness is obtained by matching the simulated with experimental C-V curve of large MOS capacitor at accumulation region. Poly workfunction is then tuned to match experimental VT at Vb=0.

2D doping profile matching

2D doping profile is calibrated by matching RSCE and SCE of VT-Lg data. In NMOS, RSCE is caused by boron pile-up underneath the gate oxide and near the LDD edge. The damage created during LDD and S/D implants greatly enhance the diffusivity of channel boron in the subsequent thermal steps. The interstitials recombine at the gate oxide surface leaving behind the boron and cause the pile-up near the LDD region. One key factor of simulating such pile-up is the interstitial recombination rate at the silicon/silicon dioxide interface (Ksurf). It is found that the RSCE is strongly depend on Ksurf in NMOS devices. The 2D doping profile is calibrated by tuning Ksurf until the RSCE and SCE are matched with experimental data. Fig. 3 shows the comparison of simulated and experimental VT-Lg data for NMOS. Excellent match between the simulated and experimental VT values shows that the 2D doping profile is well calibrated. The dashed line in Fig. 3 shows that almost no RSCE is simulated with default Ksurf value used in TSUPREM-4. Due to the RSCE, the boron concentration at the centre of the channel is higher for shorter gate length, as shown in Fig. 7. For PMOS devices, experimental data in Fig. 4 shows that they only exhibit a small RSCE. It is found that the RSCE in PMOS is caused by the low temperature, long duration thermal cycle during the formation of spacer. With the inclusion of this low temperature thermal cycle, fine tuning of phosphorus diffusivity at low temperature and boron diffusivity at high concentration, we can simulate the variation of VT with Lg accurately, as shown in Fig. 4. The effect of different thermal cycle following NLDD implant on VT is simulated accurately by using the tuned Ksurf, as shown in Fig. 5. It is expected that wafer 1 exhibits smaller RSCE than wafer 3 because part of the interstitials is recombined at the surface after the first NLDD anneal causing less boron pile up at the surface. The simulated PMOS VT of wafers 3 and 4 are compared with experimental data, as shown in Fig. 6. Simulation matched well with the experimental data and predicted that the PMOS with pocket implant (wafer 4) exhibit larger RSCE.

Mobility tuning

The last step is to match the Id-Vg and Id-Vd curves by tuning mobility model parameters. In this paper, the Lombardi surface mobility model (LSMMOB) and high field mobility model (FLDMOB) used in MEDICI [5] is selected for device simulation. LSMMOB accounts for the vertical field effect on the mobility and is tuned by matching simulated Id-Vg curve at Vd=0.1V of long channel device (Lg=10μm) with experimental data. The results of tuned LSMMOB for NMOS and PMOS devices are shown in Figs. 8 and 9 respectively. FLDMOB accounts for the parallel field effect on the mobility and is tuned by matching simulated Id-Vd curve at Vb=0V of short channel device (Lg=0.25μm) with experimental data, as shown in Figs. 10 and 11. The saturation velocity VSAT and the parameter BETA of FLDMOB are tuned separately for NMOS and PMOS until a good match is obtained.

CONCLUSIONS

In this paper, we present a physical methodology for calibrating 2D process and device simulators based on electrical data. The process simulator is tuned to capably predict RSCE and SCE on VT for different thermal cycle following NLDD implant in NMOS and pocket implant in PMOS. The 2D doping profile of NMOS can be calibrated by the interstitial surface recombination rate. However, the PMOS 2D doping profile needs fine tuning of phosphorus diffusivity at low temperature and boron diffusivity at high concentration. This is because PMOS RSCE is caused by the low temperature, long duration thermal cycle during the formation of spacer. Mobility models of the 2D device simulator is tuned and good agreement between the simulated and measured I-V characteristics of NMOS and PMOS is demonstrated.

REFERENCES

1. K.Vasanth et al, "An Efficient Method for Modeling the Effect of Implant Damage on NMOS Devices Using Effective Profiles and Device Simulation," *IEDM Tech. Dig.*, p.717, 1996.
2. K. Vasanth et al, "A Pocket Implant Model for Sub 0.18 Micron CMOS Process Flows," *Proc. SISPAD*, p.181, 1997.
3. C.S. Rafferty et al, "Explaination of Reverse Short Channel Effect by Defect Gradients," *IEDM Tech. Dig.*, p.311, 1993.
4. Technology Modeling Associates, Inc. TSUPREM-4 Version 6.5.2., Users Manual.
5. Technology Modeling Associates, Inc. MEDICI Version 4.0., Users Manual.

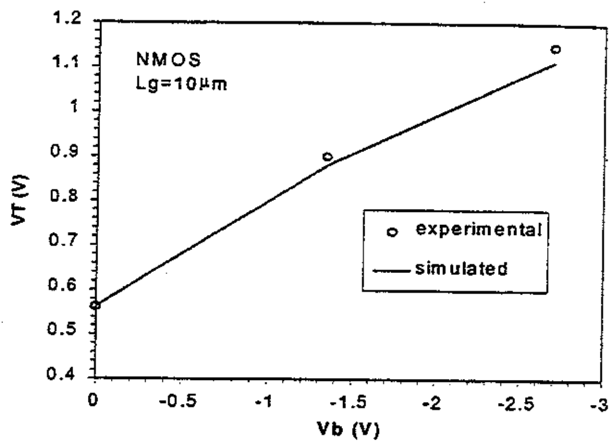

Fig. 1. Threshold voltage vs. substrate bias for long channel NMOS of wafer 1. Poly workfunction of simulated VT at Vb=0 are tuned to match experimental VT at Vb=0.

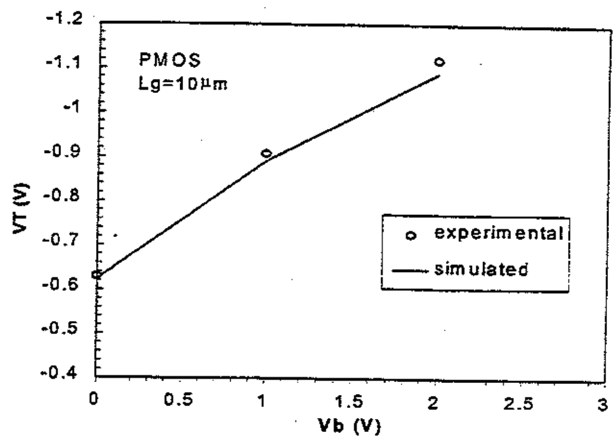

Fig. 2. Threshold voltage vs. substrate bias for long channel PMOS of wafer 3. Poly workfunction of simulated VT at Vb=0 are tuned to match experimental VT at Vb=0.

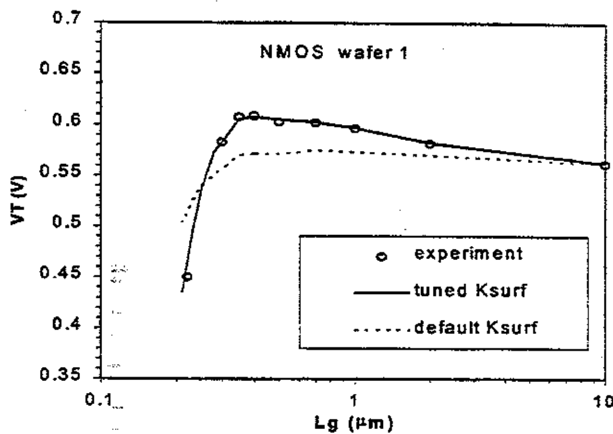

Fig. 3. Comparison of simulated and experimental threshold voltage vs gate length data for NMOS of wafer 1. The poly workfunction is tuned to fit experimental VT of long channel device.

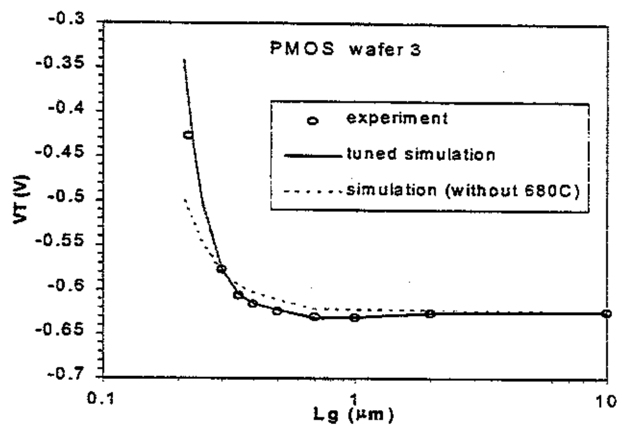

Fig. 4. Comparison of simulated and experimental threshold voltage vs gate length data for PMOS of wafer 3. The poly workfunction is tuned to fit experimental VT of long channel device.

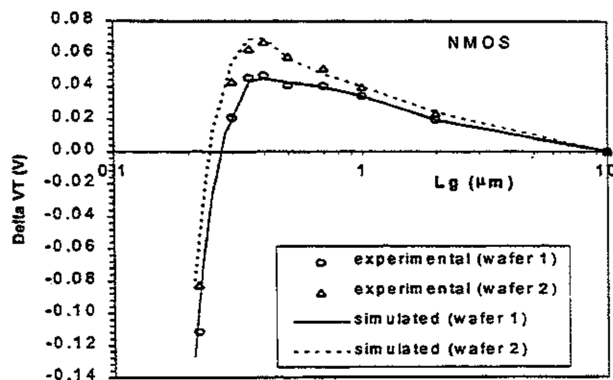

Fig. 5. Delta threshold voltage (=VT(Lg)-VT(10)) vs gate length for NMOS. Same value of Ksurf is used for the simulation of wafer 1 and 2.

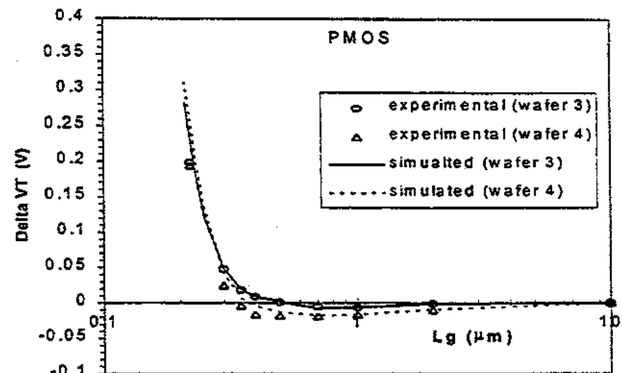

Fig. 6. Delta threshold voltage (=VT(Lg)-VT(10)) vs gate length for PMOS. Same values of model parameters are used for the simulation of wafer 3 and 4.

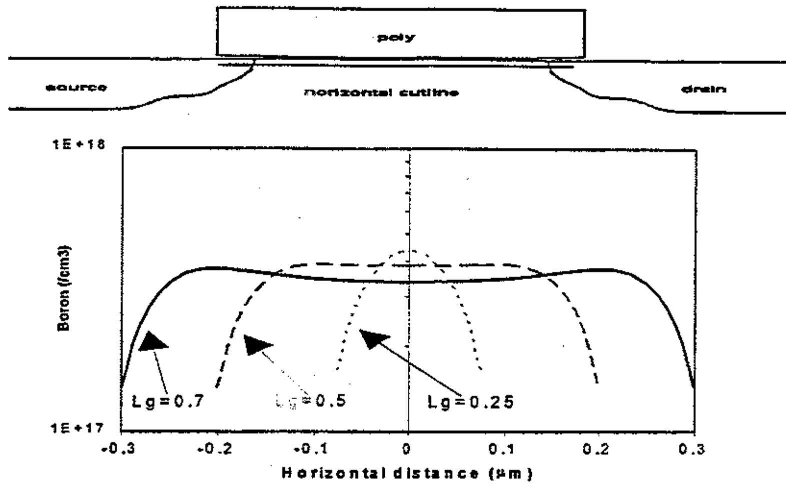

Fig. 7. Cross section of simulated NMOS device (top), and the horizontal boron profile along the cutline underneath the gate oxide for various gate lengths (bottom). The boron concentration at the centre of channel is higher for shorter gate length.

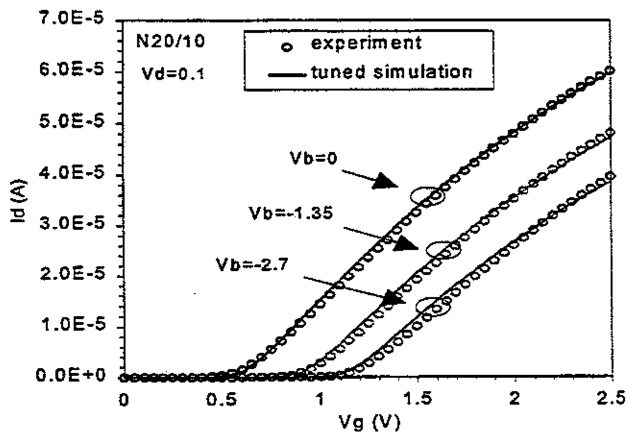

Fig. 8. Comparison of tuned simulation and experimental linear regime gate characteristic for long channel NMOS.

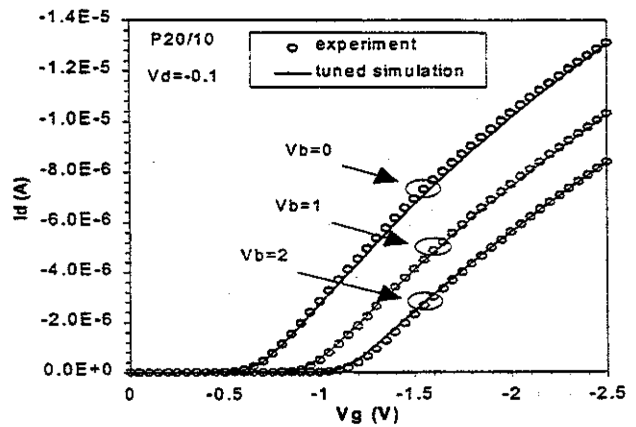

Fig. 9. Comparison of tuned simulation and experimental linear regime gate characteristic for long channel PMOS.

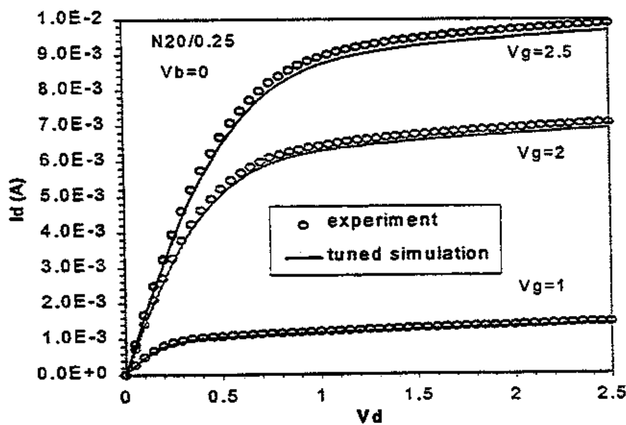

Fig. 10. Comparison of tuned simulation and experimental drain characteristic for short channel NMOS.

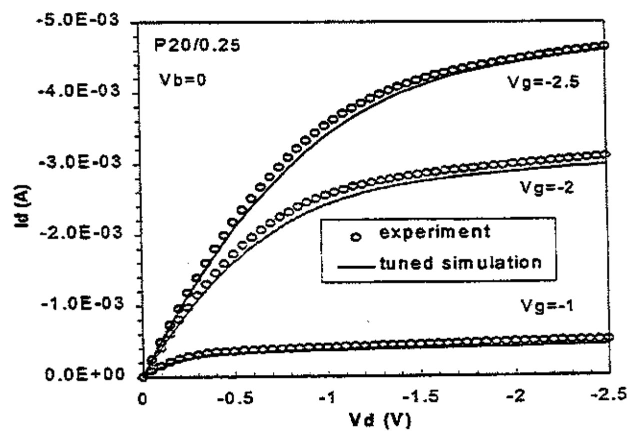

Fig. 11 Comparison of tuned simulation and experimental drain characteristic for short channel PMOS.