Layout Verification Tools for MEMS Physical Design

Kai Hahn*, Rainer Brück** and Bernd Reusch*

*Universität Dortmund, Fachbereich Informatik, LS 1
Otto-Hahn-Str. 16, D-44221 Dortmund, hahn@ls1.cs.uni-dortmund.de
**Universität Gesamthochschule Siegen, Fachbereich Elektrotechnik und Informatik
Hölderlinstr. 3, D-57068 Siegen, brueck@rs.uni-siegen.de

ABSTRACT

The impact of technology related issues in microsystem physical design is of high relevance due to the fact that mask layout and process configuration are strongly interdependant. Performing physical design in this area therefore means designing the layout of mask structures as well as an appropriate process step sequence for fabrication. Unlike in other areas of engineering the design verification task is not sufficiently supported by CAD tools today. This paper describes an approach providing software tools that enable the designer to arrange and to optimize process flows, to derive consistent design rules and to check layout designs for the specific technology intended to be used for fabrication. The tools can be accessed via the Internet. In this manner net based training and design for microsystems is possible, a feature that is especially relevant for SMEs in this field of business.

Keywords: micro system design, design verification, process validation, internet-based design tools

INTRODUCTION

Products fabricated with microsystem technology as one of the most promising key technologies are nowadays used in many innovative applications in medical, IT or automotive sectors. The market share of micromachined sensors and actuactors as interfaces between the real world and microelectronical information is constantly growing.

Unlike in other areas of engineering the physical design process in microstructure techniques is not sufficiently supported. Most CAD tools used in this area were developed either for mechanical engineering or for IC layout design nad therefore often do not meet the requirements of microsystem designers.

This lack of appropriate tools results in an unfortunate delay for the penetration process of these new engineering technologies. In this manner competitive time-to-market compared to other technologies cannot be achieved.

MICOSTRUCTURE PHYSICAL DESIGN

The design of a microstructure and the configuration of the fabrication process to be performed are characterised by strong dependencies. This is due to the fact that two dimensions of the product are defined by geometric structures given on lithographic masks, whereas the third dimension must be structured by selecting appropriate parameters for fabrication steps to be performed. This characterisation is clearly different from the current stage in microelectronics physical design where process sequences are fixed and unchangeable for the circuit designer. The design flows used to describe design stages in microelectronical design, like the well-known Y-chart model of Gajski and Kuhn consequently do not take technology related issues into account [1].

Obviously these approaches are no longer adequate to describe the situation for microstructure design. Up to now no standard devices for microstructures have been detected that turned out to be the analogous counterparts of transistors, diodes or resistors. Most of the designs require a new mask layout combined with the determination of materials and process steps to be performed according to the physical effects to be used for the function of the designed components.

Fig. 1 gives a rough example of two different components fabricated with different process sequences within the same technology family. Although only the major steps are displayed the figure shows very clearly the

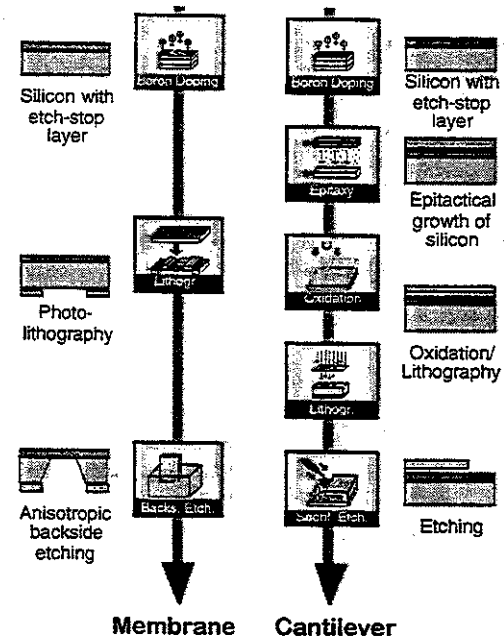

Figure 1. Examples for Design/Process Interdependencies for Microstructures

dependency between layout design and process sequence.

The explicit concurrency of layout design and process configuration is presented in the circle model in Fig. 2. The figure shows a schematic view of the basic steps to be taken during the final stages of microstructure design that leads towards the concrete fabrication data. This design stage is characterised by a cyclic concurrent procedure of designing and redesigning layout and process information. The procedure is influenced by the physical effects and resources as well as by the variety of process steps and materials to be used.

The results of the verification step in the design cycle decide either if the chosen combination of layout and process sequence is correct (i.e. the layout fulfills the design rules derived from the process parameters) or if layout and/or process arrangement have to be modified before verifying the design once again. The grey area within this design model represents the design stages where methods and tools were developed by the authors.

VERIFICATION METHODS

The verification task for microstructure physical design differs strongly from verification approaches used in IC layout design. This is a consequence from the design flow sketched above. Design verification in microelectronics is in use for some 20 years and is restricted to a check for violations of geometrical design rules within the layout.

Most design rule checking systems in this context are based on computational geometry using boolean mask operations to process the layout [2] [3].

The situation in IC layout verification is characterised by several specific conditions that are unfortunately not valid in the area of microstructure design:

- *The nature of the design rules is restricted to simple geometrical relations like spacings, widths, overhangs and overlaps.*
- *The geometrical data to check is restricted to a limited amount of shapes like manhattan style rectangles or octagonal structures.*

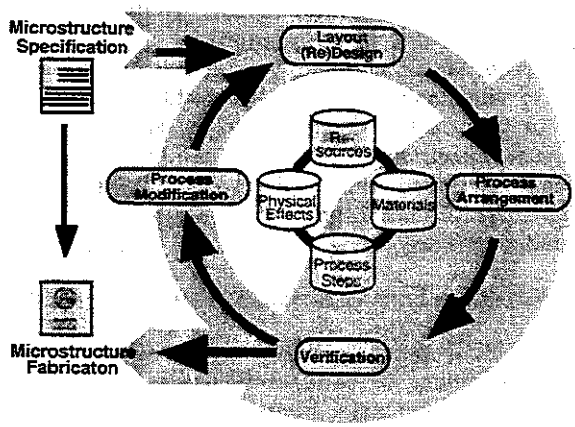

Figure 2. Microstructure Design Model

- *One set of design rules is valid for all designs within the described technology.*

All three assumptions do not hold in the context of microsystem layout design:

- To reduce the risk of bending long, narrow structures should be avoided.
- The ratio of occupied and vacant areas must not differ too strongly in neighboring regions.
- If the area of a block exceeds a certain value, holes must be inserted.
- Silicon bridge orientation not parallel to etching pits
- Convex right angles require compensation structures

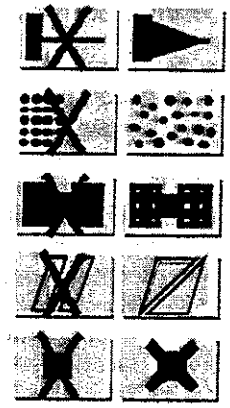

Figure 3. Design Rule Examples for Microsystem Design

Design rules in the area of lithography-based microstructures are still a matter of research. Some investigations in the area of LIGA technology [4] as well as for silicon micromachining [5], however, show that it is possible to derive formal design rules that are often of a more complex nature than simple geometrical relations. Fig. 3 gives some examples of rules to be met in this context. These few informally described rules clearly demonstrate that e.g. angles, distributions of objects and area calculations are subject to verification. Rules of that kind are not covered by classical design rule checking systems up to now.

As far as shapes are concerned microstructure design offers nearly no restrictions. Taking microfluidics or microoptics as an example is becomes clear that these technologies are based on the opportunity to fabricate an enormous spectrum of free shapes driven by the functionality of the desired components.

Verification tasks in the micromachinig area are not only restricted to layout checks. As described for the specific design model, physical design for microstructures consists of the determination of layout data as well as the design of suitable process step sequences combined with all process parameters. In this sense the consistency check for a correct process sequence with no contradictions within the process like unfitting process steps or false material assignments belong to the design verification in the same way as the subsequent layout check with design rules derived from the process description.

Informal descriptions of layout rules as shown in Fig. 3 are not usable as inputs for any computer-based verification tool. The first steps towards a CAD system is therefore the formalisation of these rules followed by the development of suitable checking algorithms. Based on earlier experience with technology description formalisms [6] a process description language called LIDO-PDL has been developed that provides means to describe formally layout rules as

well as process parameters. Descriptions in LIDO-PDL are used as inputs for the design verification system LIDO.

The basic idea for LIDO-PDL is the encapsulation of rules within objects and the configuration of these objects to complete process sequences. This approach reflects the microstructure physical design methodology with design specific process configurations. Different types of objects (as e.g. processes, process steps, materials and resources) can be used.

LIDO-PDL can also be used to optimise process arrangements with regard to cost or effort functions. For this reason work has recently been performed to extend the process description data by time and cost information. As alternative process forks can be represented in LIDO-PDL especially designed optimisation algorithms are capable to find process sequences with minimum time or cost consumption [7].

After the determination of a complete process description the set of valid design rules can easily be extracted. The first task of the verification pocedure at this stage is to check the consistency of the derived design rules.

As an example Fig. 4 shows the detection of homogeneously distributed layout structures on a process area. The even distribution of layout elements is e.g. important for the electroforming process step for LIGA technology. A deviation of the homogeneous distribution would end in an uneven growing of a nickel layer during electroforming which has to be avoided as the metal piece will serve as a moulding form afterwards.

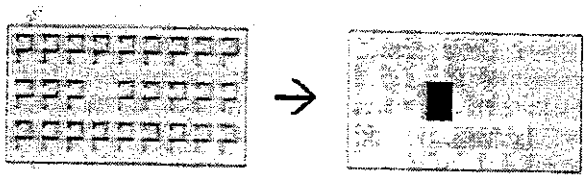

Figure 4. Check for Homogeneous Distribution of Layout Elements

The algorithm is based on the idea that an uneven distribution leads to uncovered remaining areas after an appropriate expansion of all polygons on the process area. These uncovered areas define "lacks" of original microstructured elements. The clue for this algorithm is to determine the expansion factors with regard to the polygon areas in relation to the total process area on the one hand and to the specific polygon shape on the other hand.

LIDO VERIFICATION SYSTEM

Currently there is hardly any CAD support for the design process as described. A prototype approach for design verification based on the recognition of design properties restricted to LIGA technologies is presented in [8]. Except design capture tools (like AutoCAD) there are no dedicated commercial tools for microstructure design. The tools used for microelectronics IC design are based on fixed technology data accessed via design rule interfaces. The user has no opportunity to influence the fabrication process. Correctness with regard to process or layout rules as a result of this tool configuration can only guarantee that the following fabrication of microstructures can be performed without running into problems caused by design errors. All considerations dealing with functional aspects are not within the scope of the research work described in this article.

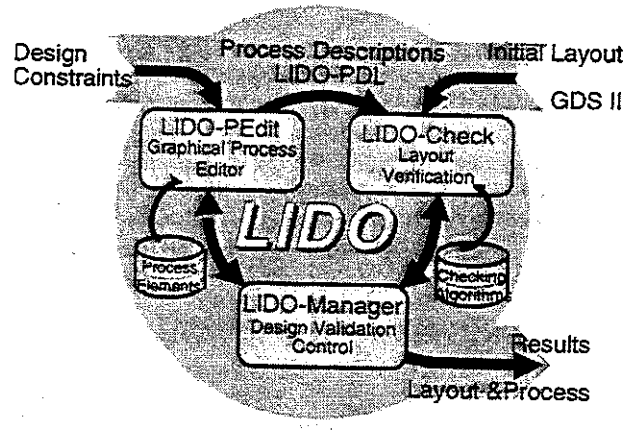

Figure 5. LIDO Design System

The LIDO[1] system takes the requirements of microstructure design into account [9]. On the one hand LIDO provides means to determine the technological process to apply in order to fabricate the designed microstructure in LIGA or silicon techniques. On the other hand the mask layout can be verified with respect to design rules derived from the process configuration.

The system consists of a common user interface and a common technology and geometry database. Fig. 5 shows a system view of the LIDO System. The user interface offers two major applications: *LIDO-PEdit*. the graphical process configuration editor and *LIDO-Check*. the microstructure design rule checker.

The databases for technological and geometrical data have been designed with regard to the specific application as a verification tool. The technological database reflects the object oriented structure of LIDO-PDL. The main feature of this database is an easy interface to access the layout or process related design rules. The geometrical database is concurrently developed with the mask layout checking algorithms. Structures are mainly stored in a polygon-based manner extended by non-polygon structures like circle segments [10].

LIDO-PEdit - The Graphical Process Editor

LIDO-PEdit provides means to configure a process sequence according to the requirements and to the layout design of the intended microstructure. The process arrangement is performed graphically in an editor window.

[1] LIDO is an acronym for Lithography-based Microsystem Design Tools

The user selects design process elements like process steps, materials etc. from libraries based on the sceecific design task he/she is performing. These elements appear as icons that can be placed on the editor window. Icons can graphically be connected to complete process sequences. Materials, layers and resources can be assigned to process steps by using arrows connecting the respective icons. Each icon is related to process or technology information such as design rules or process configuration rules as shown in Fig.6.

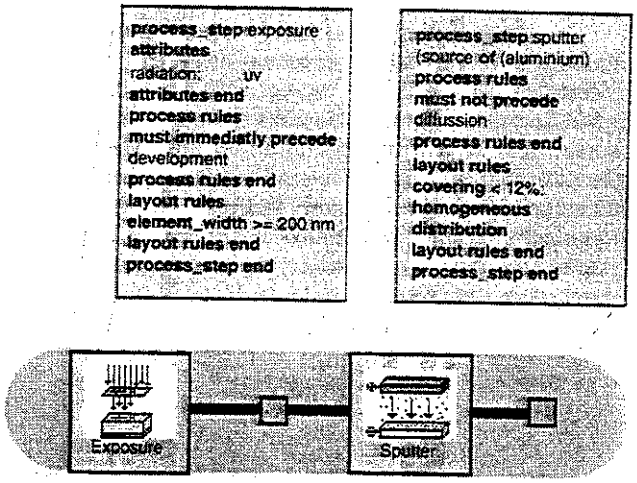

Figure 6. Icon/LIDO-PDL Relation

The technological data of the process elements is created by process experts using the process description language LIDO-PDL. As regular process sequences for silicon micromaching or LIGA consist of several tens of steps a flat graphical representation would suffer from missing clarity. For that reason the possibility to create subprocesses is implemented. Subprocesses can be defined by a simple selection of icons that will afterwards be represented by an automatically generated new icon. In this manner hierarchically structured process description are possible. Vice versa LIDO-PEdit can also arrange icons graphically after reading complete LIDO-PDL descriptions [11].

Process Consistency

LIDO-PEdit provides additionally the option to check the current process configuration for consistency. This check is normally necessary because the designer need not to know internal properties of all process elements. In this way the consistency checker will find inconsistent design rules or not allowed process arrangements.

The consistency check is implemented to verify the defined process configuration before writing the PDL description. In this procedure not only the process rules (compatibility of process steps or materials, sequence rules, assignment rules etc.) are checked but also the consistency of layout rule value ranges. This makes sure that no combination of process elements with layout rules requiring contradictory value ranges can occur. An example of this

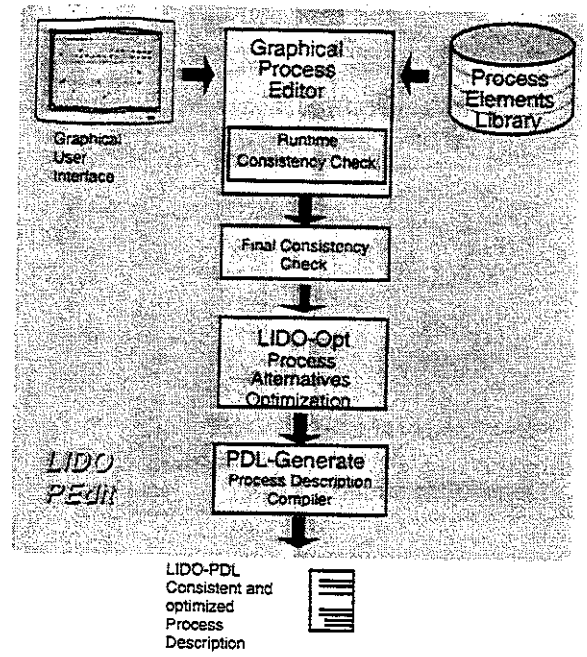

Figure 7. LIDO-PEdit Structure

might be a rule requiring a maximum object extension lower than the minimum object extension required by another rule. It is a considerable computational effort to detect this type of inconsistencies, because they are not always obvious. This problem has been solved by completing a consistency checking module based on constraint logic programming [12]. As a result of the checking procedure inconsistencies are reported to the user who must remove them manually by reediting the process description and reperforming consistency checking.

Process Optimization

As alternative process forks can be represented in LIDO-PDL especially designed optimisation methods are implemented to find process sequences with minimum time or cost consumption [9]. The graphically-based *single-source-shortest-path* algorithm analyses the process network and calculates the process configuration with lowest cost function values. The optimization module LIDO-Opt fulfills the demands of designers who want to learn about the economic implications of a process layout as early as possible. The optimization requires the definition of variable as well as fixed cost within the appropriate PDL objects. PDL offers constructs to declare all resource or process step related costs, time etc.

As a result after several checking/reediting cycles a consistent and optimized technology configuration is obtained. It can then be used to create an input file for LIDO-Check.

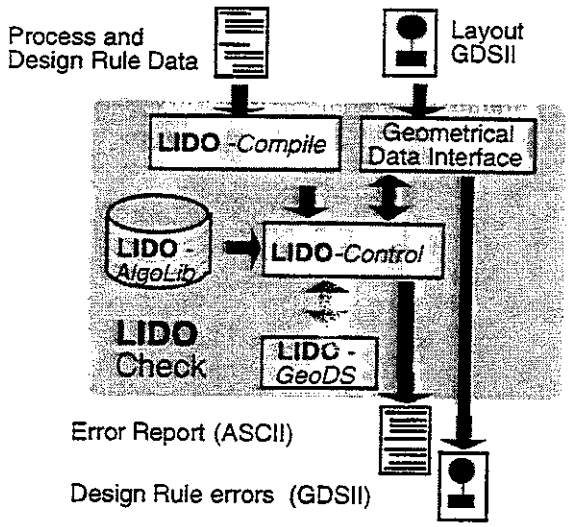

Figure 8. LIDO Check Module Structure

LIDO -Check Design Rule Checker

LIDO-Check is a design rule verification tool especially developed for microsystem mask layouts. Together with the mask design in a standard format like GDSII, the design rules from LIDO-PDL are used to verify the layout design applying especially developed checking algorithms. Because of the nature of design rules for 3-dim microstructures, the complexity of the implemented algorithms is beyond their counterparts known in IC layout verification. Not only simple geometrical distances and widths have to be checked but also arrangement rules that refer to the complete process area or rules dealing with strain or stress of materials are taken into account. For verification of these rules expressed in LIDO-PDL checking algorithms as presented before are provided in LIDO-Check. Fig. 8 shows the structure of LIDO-check. The user can invoke and control the checking procedure by a graphical user interface. The design rule check runs as a batch program. The results are displayed in two windows. The error viewer provides textual information denoting the kind of error, the counted number of errors and the rules that were violated. Additionally links to the mask design are provided by the graphical layout viewer that displays the layout and highlights the errors corresponding to the textual descriptions.

Design rule errors can either be fixed by changing the layout design or by modifying technological parameters in several cycles. The result obtained from the LIDO Microstructure Design System will be a correct layout together with a valid process description. In this way LIDO can guarantee that the physical design can be fabricated with the designed process sequence.

The user has the opportunity to store the checking results or to load already stored designs and error descriptions. The object oriented design of the algorithm library is carried out in a way that makes extensions of the rule base very easy. Fig. 11 shows a screenshot of a LIDO session. The window-oriented user interface allows the slotting in and out of needed system modules.

NETBASED ACCESS

The system presented so far is currently integrated into a training and working environment to be accessed via the Internet. The TRANSTEC project (No. MM1026) funded by the European Commission aims to implement a training course for different kinds of users teaching them how to take advantage and to solve problems using microsystem technologies. One of the main objectives in this context is to gradually change the training and education stage into a system where real-life tasks could be managed using microsystem design software.

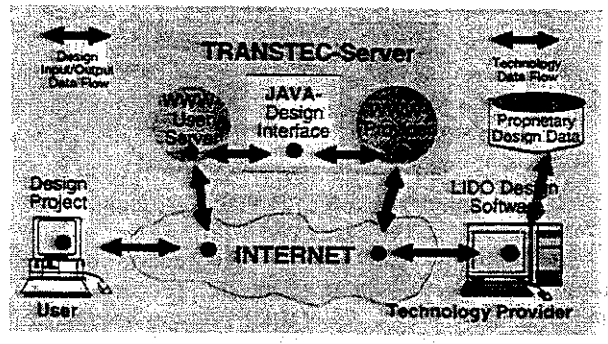

Figure 9. LIDO Netbased Access Scenario

In this sense TRANSTEC courseware will provide access to the LIDO system using JAVA design interfaces. A prototype of LIDO called INTERLIDO supporting the client/server structure of the internet was already developed [13]. The concept of internet-based design software offers several advantages especially for smaller companies:

- *They are able to participate in innovative CAD systems without purchasing the complete system. Accessing and billing mechanisms can the use of the systems at moderate rates.*
- *The installation and maintainance of extensive software systems is no longer necessary.*
- *Access can be granted from any location at any time.*
- *Confidential technology data from providers side can easily be protected.*

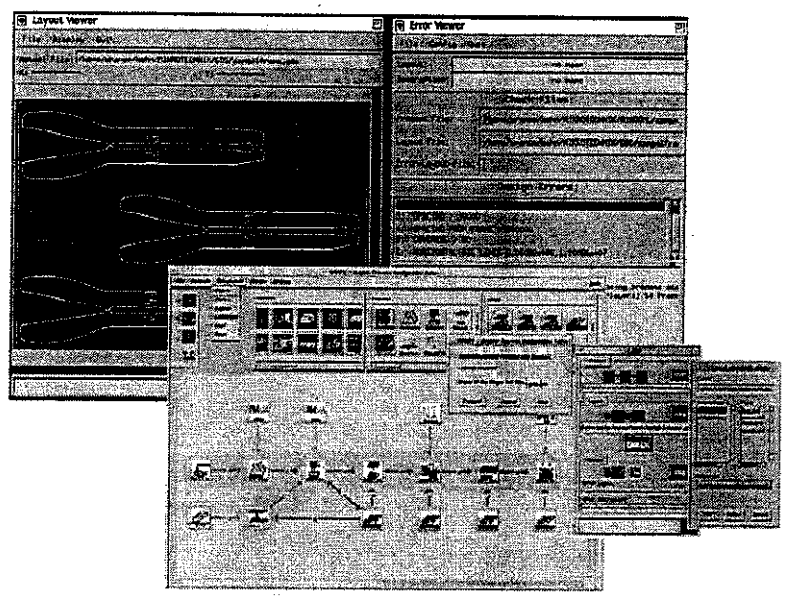

Figure 10. LIDO Session Screenshot

CONCLUSION

The reasons for a different approach to lithography-based microstructure physical design verification were described. The developed model proposing the concurrent design of physical mask layout together with the establishing of a suitable process step sequence necessitate methods and tools that facilitate the consideration of design specific process information. For the task of design verification means to formal process description were presented. Based on these formal rule sets specific checking algorithms were developed as methods known from IC verification were not usable. All considerations were used to create the LIDO verification system consisting of a process configuration part as well as a layout design rule checker.

The LIDO system has been implemented on SUN OS platform using the Motif X-window library. The InterLIDO approach is implemented using JAVA. The system has been applied to several real-life layouts of microstructures designed for LIGA processes that have been provided by the IMM (Institut für Mikotechnik Mainz).

Future work is dedicated towards enhancing the checking algorithms for the complex design rules and to integrate a distributed networking version of the LIDO-system into a european training course for micromaching.

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