3-D Electrothermal Model of Multifinger, High-Power HBTs

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ABSTRACT

We present a 3-D electrothermal model based on the finite difference method and applied to GaAs heterojunction bipolar transistors (HBTs). This non-linear model computes the temperature distribution under static bias conditions for multifinger HBTs, although it can be modified to simulate silicon bipolar devices. The model takes into account emitter ballast resistance, thermal shunt design and the non-linear temperature dependence of substrate thermal conductivity. A simplified analytic electrical model for the HBT can be modified to fit the user's device characteristics. We compute maximum junction temperature and device thermal resistance for three-dimensional HBT structures. We use this model to optimize the thermal design of InGaP/GaAs HBTs employing emitter ballast resistance and thermal shunt, and we compare the parallel topology to the distributed (or "fishbone") topology for power HBT unit cells.

INTRODUCTION

The GaAs-based heterojunction bipolar transistor (HBT) is a promising alternative to the field-effect transistor for power amplifier and mixed-mode applications from L to Ku band. However, the combination of poor GaAs thermal conductivity and positive electrothermal feedback within the device results in a thermal limitation in HBTs which can occur well before the onset of electrical limitations, especially in multifinger designs. Of particular concern in power HBTs is the current collapse phenomenon [1], which results from the negative temperature coefficient of the base-emitter junction. To minimize the impact of these thermal constraints, it is desirable to employ thermal stabilization techniques. Ballast resistors placed on the base [2] or emitter [3] terminals can improve thermal stability, at the expense of reduced microwave gain and efficiency. In addition the thermal resistance of HBTs can be reduced using a variety of techniques, including flip-chip connection and the thermal shunt [4]. The goal of this work is to model, for an arbitrary dc bias point, the thermal resistance and junction temperature of multifinger HBTs having a thermal shunt and/or emitter ballast resistance.

Commercially available, three-dimensional thermal models typically employ constant, independent power sources for the active regions of the device. While this technique may be useful for regarding heat transfer within HBTs, it can not predict the maximum junction temperature attained for a given static bias condition. In addition, these models are often based on the finite elements method, thus requiring substantial computing power and long computation times for complex structures. Therefore we developed a non-linear, finite-difference model which takes into account the electrothermal interaction of temperature and current as well as high current injection effects. We also developed an analytic electrical model for the HBT which can be user-modified to fit the user's device characteristics, and we took into account the non-linear temperature dependence of GaAs thermal conductivity. This 3D electrothermal model calculates the thermal resistance and temperature distribution for an arbitrary dc bias point (base current I_b or base-emitter voltage V_{be}, and collector-emitter voltage V_{ce}). Our model allows for the optimization of numerous topology variables by studying their impact on device thermal resistance. The simplified analytic electrical model coupled with an efficient FD solution of the heat transfer equation provides a good compromise between computation time and accuracy.

MODEL

Thermal Model

The general heat transfer equation governing heat flow in solid materials in steady state is shown in (1).

$$\nabla \bar{k} \nabla \bar{T} + q''' = 0 \qquad (1)$$

where k is thermal conductivity ($Wm^{-1}K^{-1}$), T is temperature and q''' is the volumetric heat generation term (Wm^{-3}). This equation can be non-linear through the thermal conductivity term k and the heat generation term q'''. This equation is solved using a 3D finite difference method with adapted boundary conditions, which are described below.

The HBT topology examined in this study consists of emitter mesas on top of a GaAs substrate. If a thermal shunt is modeled, the pillars of the thermal shunt contact the mesas directly, or the user can define a dielectric layer between the shunt metal and the emitter mesa. A schematic cross-section of a four-finger, thermally-shunted HBT is shown in Figure 1. This simplified topology is sufficient to describe the most important elements involved in the thermal resistance computation. For instance, among the 22 user-definable geometric variables are via hole dimensions, via metal thickness, distance between the outermost fingers and the shunt landing areas, pillar metal height and emitter mesa thickness. The emitter fingers can be arranged in a parallel configuration (as in Figure 1) or in a distributed (a.k.a. "fishbone") arrangement. In a distributed topology, groups of emitter fingers are arranged in two or more rows, each separated by a distance d.

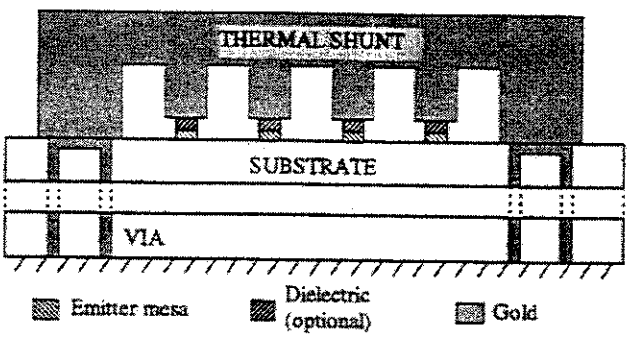

Figure 1. Cross-section of typical simulated structure (not to scale).

Most of the 3D structure is meshed using cubes of constant size, typically 2 μm. However, the cell size is scaled down accordingly for the emitter mesa(s) as well as for the heat generating portions of the structure (i.e. the base-collector junction areas). We will develop the expression for temperature at the center of a cube using the notations in Figure 2, where the central cell is labeled 'a', and the six surrounding cells are labeled b-g. The convention of computing scalar values in the center of an elementary volume and not at each corner leads to a control volume approach. In this method the temperature in each point of the structure is calculated by evaluating the heat transfer through the six sides of the cell. The heat flux f across a surface S is expressed with Fourier's Law:

$$\vec{f}_{\vec{n}} = -k_S \frac{\partial T}{\partial n}\vec{n} \qquad (2)$$

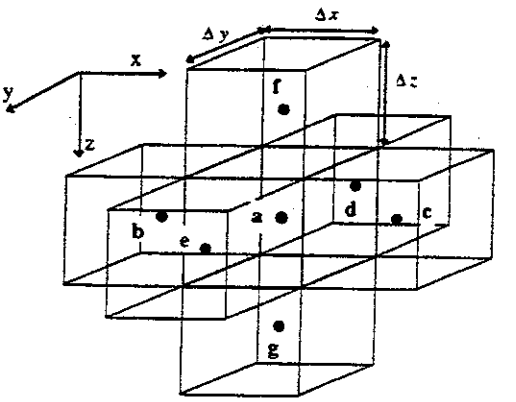

Figure 2. Control volume notation for the finite difference method.

In equation (2) k_s is the thermal conductivity at the surface, and $\vec{n}$ is the normal direction. In an elementary volume of the type shown in Figure 2, the heat flow balance over the six faces (denoted s1-s6) is

$$f_{s1}(\Delta y\Delta z) - f_{s2}(\Delta y\Delta z) + f_{s3}(\Delta x\Delta z) - f_{s4}(\Delta x\Delta z) + f_{s5}(\Delta x\Delta y) - f_{s6}(\Delta x\Delta y) + q'''(\Delta x\Delta y\Delta z) = 0 \qquad (3)$$

To evaluate the thermal conductivity at a surface S, we express the heat transfer in one dimension normal to that surface. Referring to Figure 3, the heat flow across the surface area S is expressed as

$$\frac{f}{S} = \frac{T_B - T_S}{\frac{\Delta x_{BS}}{k_B}} = \frac{T_S - T_A}{\frac{\Delta x_{SA}}{k_A}} \Rightarrow \qquad \frac{f}{S} = \frac{k_B k_A}{k_A \Delta x_{BS} + k_B \Delta x_{SA}}(T_B - T_A) \qquad (4)$$

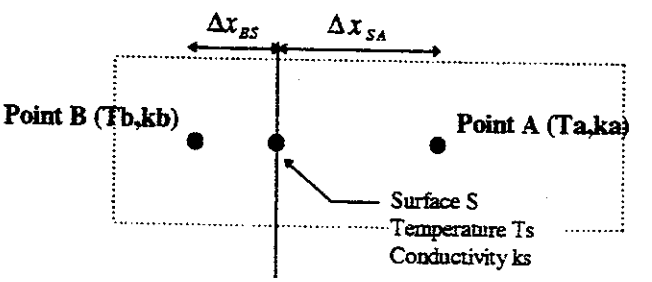

Figure 3. Computation of surface thermal conductivity.

In the case of a constant mesh we obtain:

$$k_s = \frac{2k_A k_B}{k_A + k_B} \qquad (5)$$

$$Ta = \frac{(Tbk_{S1} + Tck_{S2})\frac{\Delta z \Delta y}{\Delta x} + (Tdk_{S3} + Tek_{S4})\frac{\Delta z \Delta x}{\Delta y} + (Tfk_{S5} + Tgk_{S6})\frac{\Delta x \Delta y}{\Delta z}}{(k_{S1} + k_{S2})\frac{\Delta z \Delta y}{\Delta x} + (k_{S3} + k_{S4})\frac{\Delta z \Delta x}{\Delta y} + (k_{S5} + k_{S6})\frac{\Delta x \Delta y}{\Delta z}} \quad (6)$$

With a Taylor series decomposition of (3), we get the temperature for every cell in the structure (equation 6). This expression is in explicit form which is why we compute the temperature with an iterative method. The thermal conductivities of GaAs and gold (in $Wm^{-1}K^{-1}$) are modeled as:

$$k_{GaAs}(T) = 44\left(\frac{T_o}{T}\right)^{1.25} \quad (7)$$

$$k_{Au}(T) = 318.2 - 0.062T \quad (8)$$

where T_o is the ambient temperature. As for boundary conditions, for the backside of the substrate and the sides of the HBT the user can choose between a constant temperature condition and a Dirichlet condition, which approximates continuous heat flow across a boundary. The constant temperature boundary condition is perhaps less physically meaningful than the Dirichlet condition but results in faster convergence; the Dirichlet condition is employed to simulate a substrate dimension (e.g. thickness) of essentially infinite length. For the upper surface of the device, we take into account radiation and convection effects. The convective heat transfer term is expressed as

$$q'' = h(T_s - T_o) \quad (9)$$

where T_s is the temperature of the convective surface, T_o is the ambient temperature and h is the convection coefficient in $Wm^{-2}K^{-1}$. The convection coefficient has a value between 5 and 25 for natural convection but can increase to 1000 for forced convection. The radiative heat transfer term is defined by the Stefan-Boltzmann law of blackbody radiation:

$$q'' = \sigma T_s^4 \quad (10)$$

where σ is the Stefan-Boltzmann constant (5.67×10^{-8} $Wm^{-2}K^{-4}$) and T_s is the temperature of the emissive surface. In the calculation for heat flux at the surface of the device, this radiation term results in a fourth-order polynomial which is solved with a Newton-Raphson algorithm.

Electrical Model

Heat generation in the device is modeled as Joule heating in the base-collector junction regions. We refine the mesh in these regions using a scale factor which divides each emitter finger area into cubes much smaller than the surrounding mesh. For each point i,j,k in the "active" region of the structure, we calculate power dissipation using the following relation:

$$q_{i,j,k} = (Vce - \mathrm{Re}(ib_n + ic_n)) \times Jb_{i,j,k} \times \beta_{i,j,k} \times \Delta x \times \Delta y \quad (11)$$

where V_{ce} is collector-emitter voltage, R_e is emitter resistance, ib_n and ic_n are total base and collector current for finger n, $Jb_{i,j,k}$ and $\beta_{i,j,k}$ are the base current density and current gain at mesh point i,j,k, and Δx and Δy are mesh units in the x,y plane. We use a thermionic injection relation to model the base current density as a function of applied base-emitter voltage and temperature:

$$\begin{cases} Jb(T,Vb) = Jo\left(1 - \frac{Vb}{Vbi}\right)\left[\exp\left(\frac{Vb}{V_T}\right) - 1\right] \\ Jo = \xi A^* T^2 \frac{Vbi}{V_T}\exp\left(\frac{-Vbi}{V_T}\right) \end{cases} \quad (12)$$

where V_b is applied base-emitter voltage, V_{bi} is junction built-in voltage, A^* is Richardson's constant (1.2×10^6 $Am^{-2}K^{-2}$), V_T is the thermal voltage (kT/q) and ξ is a fitting parameter. Figure 4 shows the computed and simulated base current characteristics for an elementary transistor with a 7 ohm emitter resistance. For the modeled characteristics, the voltage V_b is applied across the emitter base junction with a series resistance of 7 ohms. The mismatch of the curves for low injection levels is due mostly to surface recombination current.

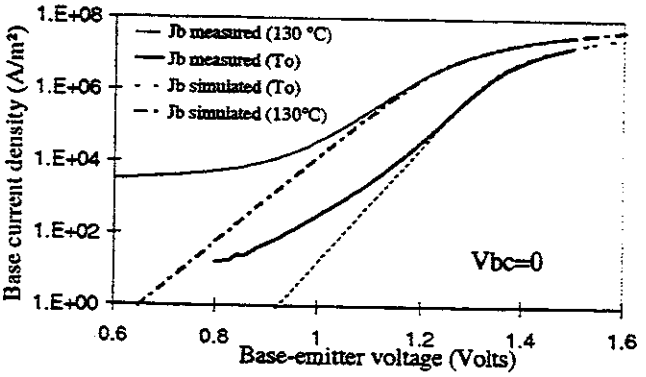

Figure 4. Simulated versus measured base current.

The dc current gain (β) is expressed as an idealized function of temperature and base current density. To accomplish this, we first defined an ideal function $\beta = f(J_c)$, and we measured gain as a function of temperature. Gain is assumed to be independent of collector current density between two current densities, J_{lin} to J_{crit}, although β_o does vary with temperature. Below J_{lin}, current gain varies linearly with current. High current injection effects are modeled as a linear decrease of gain between the collector current densities J_{crit} and J_{end}. Using this analytic expression for β as a function of J_c and the relation $J_c = \beta J_b$, we derive the following for β as a function of J_b.

$$\beta = \begin{cases} Jb\dfrac{\beta o^2}{J_{lin}} & \text{for } Jb < \dfrac{J_{lin}}{\beta o} \\ \beta o & \text{for } \dfrac{J_{lin}}{\beta o} \le Jb \le \dfrac{J_{crit}}{\beta o} \\ -\dfrac{\beta o J_{end}}{J_{crit} - J_{end} - \beta o Jb} & \text{for } Jb \ge \dfrac{J_{crit}}{\beta o} \end{cases} \quad (13)$$

The influence of temperature on current gain was measured for our InGaP/GaAs HBTs and was found to be:

$$\beta o = \beta_{To} - 0.025T \quad (14)$$

where T is the temperature in °C and β_{To} is the dc gain at ambient temperature. It should be noted that we neglect avalanche breakdown in the HBT. This is because the typical operating voltage V_{ce} of our devices is around 10 V, well below the common emitter breakdown voltage BV_{ceo} of 18-22 V.

Resolution

Temperature in every cell of the mesh is computed iteratively from equations 6 to 14 using a Gauss-Seidel algorithm. One iteration consists of computing temperature in the whole structure. After one iteration the thermal conductivity is adjusted using the laws in (7) and (8), and the dissipated power is computed. The number of iterations necessary to achieve a stable solution depends on the bias conditions, since either the base-emitter voltage or base current is augmented to its final value in a stepwise manner so as to avoid divergence. In general, convergence is attained after 3000 - 5000 iterations.

VALIDATION

This model has been validated with thermally-shunted, four-finger HBTs having 7 ohms per finger emitter ballast resistance. However, direct comparison of computed and measured thermal resistance is not used to validate the model. In general, our model predicted thermal resistance values that were 20-30% higher than our measured values. This is because measurement methods for thermal resistance are based on the coincidence of isothermal measurements (e.g., pulsed I-V or gummel characteristics) with non-isothermal measurements (e.g. output characteristics I_c-V_{be}) [5,6]. This results in an estimation of junction temperature that is a pseudo-average temperature and not the true maximal junction temperature for a given bias condition. For validation purposes, we compare the measured and simulated output characteristics (I_c vs. V_{ce}). In Figure 5, the solid lines are the measured output characteristics of the 4-finger device, and the dots are the simulated collector currents for a range of base currents and collector-emitter voltages. There is good agreement between the measured and simulated results, including in the region of negative differential resistance. For these ballasted, thermally-shunted devices, no current collapse phenomenon was visible in the dc measurement.

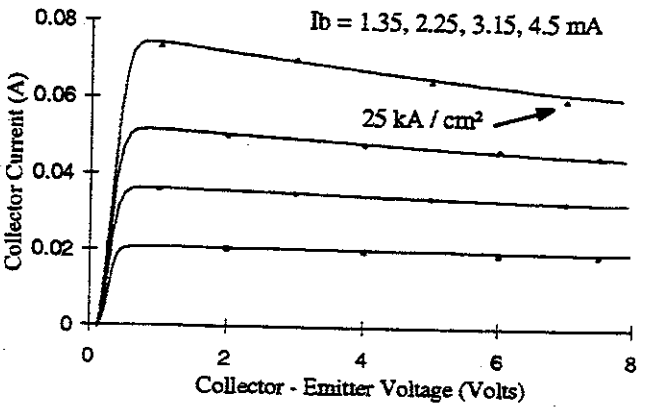

Figure 5. Simulated and measured collector current versus collector-emitter voltage.

RESULTS

In Figure 6, we present the variation of maximum junction temperature as a function of dissipated power for two values of emitter resistance. The device simulated is a four-finger HBT without thermal shunt. We held base current constant at 3 mA and varied collector-emitter voltage. Note the increase in the threshold of thermal instability (i.e. current collapse) from about 300 mW to nearly 340 mW as emitter resistance is doubled from 3.5 to 7 ohms. It is also interesting to note that both curves are initially linear but become non-linear as the current (and thus temperature) distribution among the four fingers becomes non-uniform.

Figure 7 depicts the evolution of thermal resistance and maximum junction temperature as a function of thermal shunt thickness for a four-finger device

at a power dissipation of 270 mW. There is a rapid decrease in thermal resistance between 2 and 6 micron shunt thickness, after which the decrease is less pronounced. We performed similar studies in order to optimize substrate thickness, emitter mesa thickness, emitter finger spacing and shunt pillar thickness. In terms of thermal resistance reduction, the variables having the largest impact are shunt thickness, mesa thickness and finger spacing. For designs in which emitter ballast resistance is integrated as a lightly doped emitter layer on the order of 500 nm thick, it should be noted that this increases the thermal resistance of a 4-finger HBT by about 23%. We note also that thinning the GaAs substrate from 100 μm to 30 μm results in just an 8% decrease in thermal resistance.

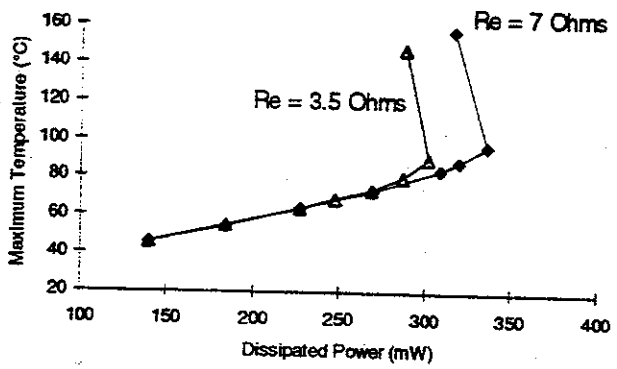

Figure 6. Maximum temperature versus dissipated power for a 4-finger HBT without thermal shunt, R_e = 3.5 ohms (triangles), R_e=7 ohms (diamonds).

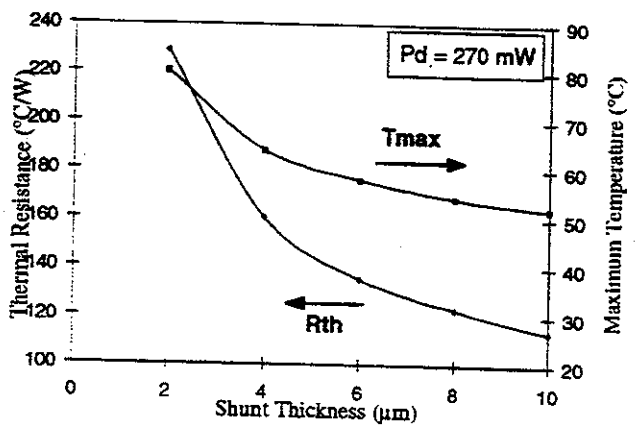

Figure 7. Thermal resistance and maximum temperature versus shunt thickness for a 4-finger HBT.

A 2D depiction of current collapse is seen in Figure 8 for a 4-finger thermally-shunted device. Note the formation of a hot spot (as V_{ce} increases) and the reduction in temperature of the surrounding fingers (Figure 8b) as compared to the pre-collapse condition in Figure 8a.

Finally, we present in figure 9 a comparison between the parallel and distributed topologies. Two-dimensional temperature distributions are shown for two 6-finger, thermally-shunted devices, each biased at I_b = 3 mA and V_{ce} = 7 V. Note the thermal coupling between the two rows of emitter fingers (distributed topology). For values of d smaller than 150 μm, the maximum temperature obtained for the distributed device is higher than that of the parallel device. Although a compact design, the distributed topology results in higher thermal resistance.

CONCLUSION

We have presented a 3D electrothermal model for HBTs. This model is based on a numerical resolution of the heat flow equation, coupled with a heterojunction injection relation, an analytical current gain expression, the GaAs non-linear thermal conductivity and high current density effects. We incorporated a meshing routine which models parallel or distributed emitter-finger, thermally-shunted HBTs with or without emitter ballast resistance. In addition it can be easily modified to simulate arbitrary device topologies as well as bipolar transistors based on silicon or indium phosphide substrates. It is a useful tool for optimizing the thermal design of multifinger power HBTs without the need for costly design prototyping.

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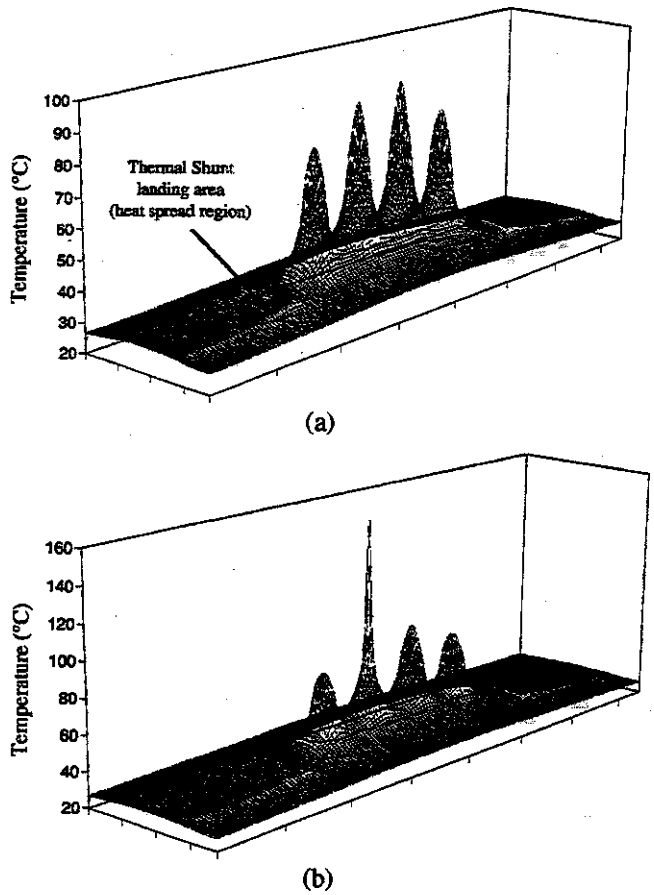

Figure 8. 2D temperature distributions (active region) for 4-finger thermally-shunted HBT with (a) I_b= 3.5 mA, V_{ce}= 7.5 V and (b) I_b= 3.5 mA, V_{ce}= **8.0 V**.

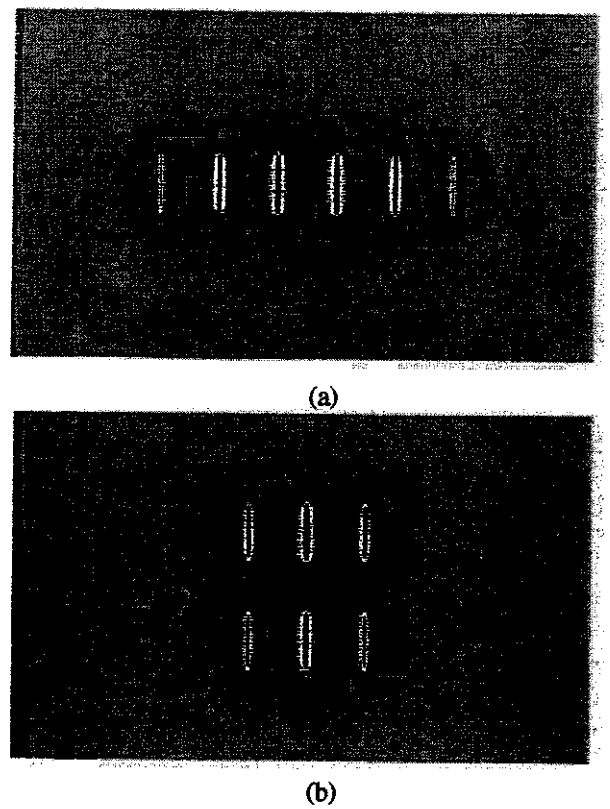

Figure 9. 2D temperature distributions (active region) for 6-finger, thermally-shunted HBTs with (a) parallel and (b) distributed topologies.