A multi-disciplinary design flow for designing embedded systems on silicon

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Abstract

Integrating systems on silicon implies more and more concurrent design by multi-disciplinary teams that combine expertise in different technology disciplines. Future systems on silicon will consist of multi-processor architectures with high bandwidth embedded memory architectures and executing complex but extremely efficient real-time embedded software. Via high speed AD/DA convertors, the digital functions will interact with e.g. the integrated Radio Frequency (RF) front-end, operating at several Ghz. During the process of designing such systems, low power and EMC problems have to be studied. Design technology for building such systems on silicon will have to support the analysis of the interactions and the trade-offs between these very different components. Moreover, during all phases of the design process, the overall view of the system implementation and progress has to remain available.
Designing an optimised system requires a design flow that deals concurrently with system design at a high abstraction level, with component design at a very detailed level and with packaging and interconnect technologies. Many of the CAD tools in the design flow will be developed by expert designers that formalise and encapsulate their knowledge into application specific software and generators. Obviously CAD is important for alleviating the above design problems. However, the systematic formalisation of the design activity and the creation of multi-disciplinary design teams will be of utmost importance to deal with the above challenges.

Introduction

Systems on silicon have become possible as a result of the fast evolution of VLSI technology. Modern (BI)CMOS technology allows complete systems to be integrated on a single chip while new packaging technologies allow the use of micropattern techniques also on multichip carriers. The same micropattern techniques can also be used for designing micromechanical structures as well as silicon sensors possibly with inclusion of signal conditioning, conversion and interpretation circuitry.

Although in principle all these microsystems are technologically feasible, it is clear that designing them may be the true bottleneck for the exploitation of their potential.

CAD can obviously be of help to shorten the design cost of these complex systems.
It is this authors opinion that the design of microsystems goes far beyond the capabilities of actual CAD systems. Therefore we have to ponder in what direction future CAD must be developed in order to cope with this important new challenge.
It will be discussed how the new CAD required will be much more multi-disciplinary design knowledge oriented than today's tool oriented CAD.
Therefore such *CAD* systems will have *to be developed by designers themselves* and although this sounds exciting, designers are usually *not the best software people* and that may be one of the biggest obstacles to the future of design. Traditional CAD may only be restricted to the delivery of the framework into which tools and methodologies are to be embedded. The successfulness of future CAD systems will be measured on their friendly openness to creative designers.

The software heaven and the physics hell

The specifications of systems on silicon are generated by systems engineers thinking in terms of JAVA, C++ or other high level, object oriented formalisms. These high level, executable models allow to increase the productivity of the systems engineers dramatically. However, at the back-end of the design cycle the complexity of the physical problems, due to continuous scaling of technology, disturbs the nice abstraction between bits, voltages and transistors. It requires new circuit, layout and clocking strategies as well as low power techniques. The widening of this gap, between a software centric system level description and its implementation in a silicon architecture is a major challenge of future design technology.
Moreover, the future microsystems will be complex, multi-paradigm devices that combine, on one single substrate, RF front-end functions, massive amounts of DRAMS and many communicating processors, running real time embedded software. In order to reduce the NRE cost of these systems, the application of IP (Intellectual Property) blocks will be essential. However, designing microsystems will involve much more than composing a silicon board out of a database of IP building blocks. The creation of silicon boards will require a design team that brings together software experts, analog designers, DSP specialists and packaging people to execute a synergetic design.
Bridging the gap between system level concepts and their implementation in a heterogeneous silicon architecture requires a multi-disciplinary design environment that supports the global co-design of system architectures and packages, analog and digital functions as well as hardware and software.

Global design of packaged systems

In order to fully exploit the capabilities of the emerging micro-machining technology, it can no longer be true to look at packages as a simple mechanical space transformer to interconnect chips.
The rapid growth of chip compatible micro-machining technologies that yield

micro-scale, high Q components may result in micro-machined novel devices that will e.g. replace the off-chip, discrete components such as oscillators and filters in wireless transceivers. Once these miniaturised filters and oscillators become available, the fundamental basis upon which communication systems are developed may also evolve and will give rise to new system architectures with possible cost, power and bandwidth efficiency advantages. For example, figure 1 (a) shows a traditional wireless receiver architecture whereby the RF front-end functions are integrated in GaAs or BiCMOS components combined with MCM integrated passives. The IF functions still require discrete, off-chip devices due to the highly selective filtering for channel selection and due to the extremely noise free oscillators for frequency translation (not possible in current MCM due to the low Q values). Finally, the digital functions are implemented in CMOS.

As a consequence, the overall receiver size and cost is dominated by the numerous discrete components. Re-organizing the architecture of the receiver as shown in figure 1 (b) by applying a direct frequency downconversion can, in some cases, result in a fully integrated system using integrated passives in the MCM technology and (Bi)CMOS for the other functions. This will happen at the cost of more stringent requirements for the AD Convertor.

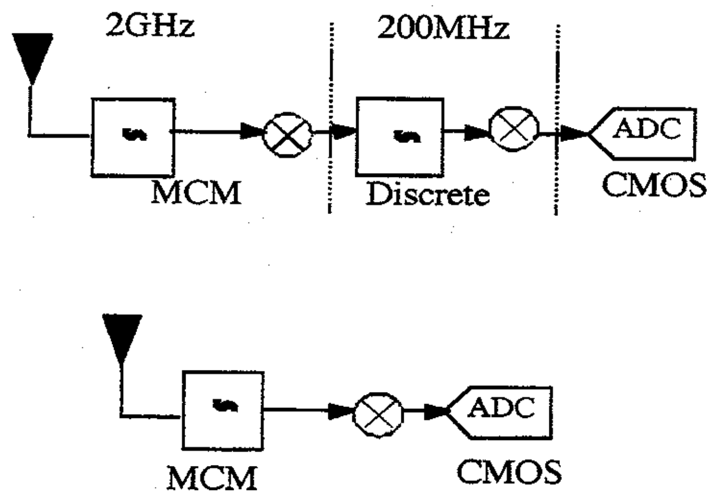

Figure 1
(a)
(b)

Next, it is very questionable whether the future giant chips of 3x3cm, using a 0.18um technology, that combine good logic devices with embedded DRAM and analog functions, together with up to 8 metal layers, will always make economic sense for future embedded systems. Especially in low power digital communication systems that are characterised by an architecture of loosely connected, complex DSP functions, it is the author's belief that an MCM technology, connecting several smaller chips on a silicon substrate can give rise to better results in terms of performance, power and cost. The above implies the disribution of system level functions between the ICs and the package, at an early phase of the design process. This partitioning has to be guided by accurate estimators in terms of routing complexity, performance gain and total system cost.

In the future more functionality will be provided in the micromachining

technology such as higher quality integrated passives, antenna's as well as higher line densities. This will lead to major enhancements in future transceiver architectures.

The creation of an integrated design environment that supports hierarchical on/off chip routing and that gives support for distributing system functions between chip and package, using accurate cost functions, will be a prerequisite for the efficient design of system architectures that optimally exploit all available implementation technologies. Only then, the synergism between the chips and the package will be fully appreciated by the design community.

Analog/digital co-design

Design technology for analog subsystem design is still far behind the digital counterpart. In daily practice, the most intensively used tool set consists of polygon pushers, SPICE like circuit simulation and DRC. Recently, some switched capacitor simulation and filter synthesis tools have emerged. Catching, managing, transferring and validating the specifications of mixed analog/digital systems is still a real bottleneck for microsystem design. Currently, the acceptance is growing for analog module generators. The latter are based on fixed topologies of analog functional building blocks such as op-amps, comparators, flash converters etc.... Analog design will make use of partly parametrisable libraries. In this way, more and more design knowledge will be captured by the CAD system, allowing the designer to focus on the analog system level rather than the analog building block level.

For example, for the optimal design of a complete transceiver, the design of the digital part should take into account the signal degradation caused by the analog front-end. This requires the analog front-end to be modelled at a high level , such that the signal degradation can be quantified at the architecture level.

Nowadays the boundary between the analog and the digital parts in a transceiver shifts in the direction of the antenna. Operations such as up- and downconversion and filtering are more and more performed in the digital domain. However, this may pose tighter requirements on the remaining analog circuits, leading to a high power consumption in the analog blocks. Intelligent decisions on the boundary between analog and digital parts may result in order-of-magnitude power savings. Trade-offs between analog or digital implementation of functionality are still performed manually by experienced system designers. However, a rapid assessment of the performance of the different options requires a high level simulation of mixed analog digital transceiver front-ends.

Hardware/software co-design

The digital parts of an integrated system contain a mixture of embedded software and hardware functions. Essential hereby is the design automation of the communication between the hardware and the software. Hardware/software interface synthesis aims at implementing the communication between the software processes and the hardware processes,

which is specified in an abstract way at the system level, on a particular architecture that makes use of embedded processors. During the whole design refinement process both the hardware and the software designers must be able to verify their design in the global HW/SW context, as such guaranteeing correct behaviour as shown in figure 2 (b). Issues such as guaranteeing real time behaviour of embedded HW/SW systems are still left to be solved.

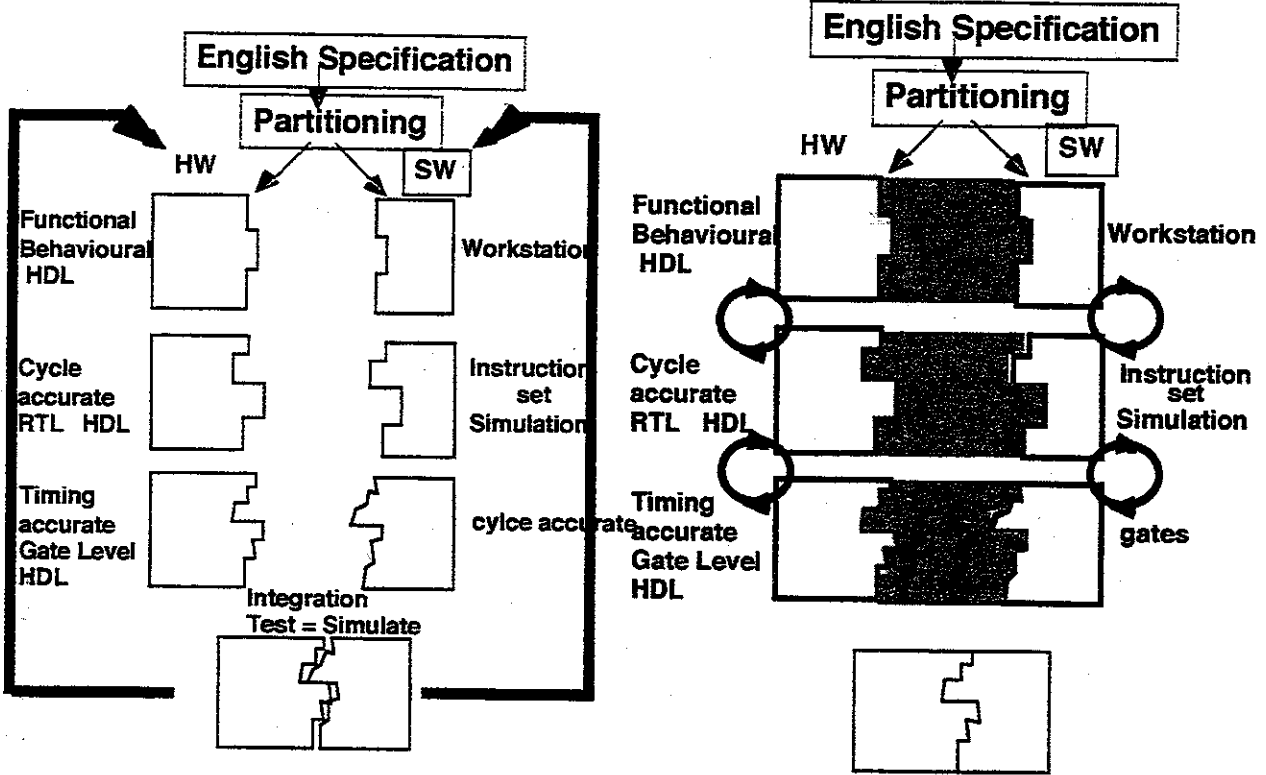

Figure 2 (a) (b)

Conclusions

The evolution of processing technology will result in the implementation of systems on 'silicon boards'. In order to optimally exploit the capabilities of this technology, a multi-paradigm design environment must be created. Such environment must allow a multi-disciplinary design team to work together according to a formal and

systematic design methodology. The CAD tools that support such a design flow must allow for evaluating technology choices at the system level. System design must include the global optimisation of architectures, implementation technologies and packaging. Co-design of packaging and architectures, hardware and software as well as analog and digital functions is essential to globally optimize the architectures of embedded systems. MCM is an important technology that offers a good alternative for the ever faster and larger 'SIA roadmap' chips, especially, in the context of low power, low cost digital communication systems.

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